Low Power VLSI Circuits and Systems
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Lecture No. # 21

Leakage Power Dissipation

Hello and welcome to today's lecture on Leakage Power Dissipation. We are discussing various sources of power dissipation in CMOS circuits. In the last two lectures, we have discussed the switching power dissipation, short circuit power dissipation. And today, we shall primarily focus on leakage power dissipation.

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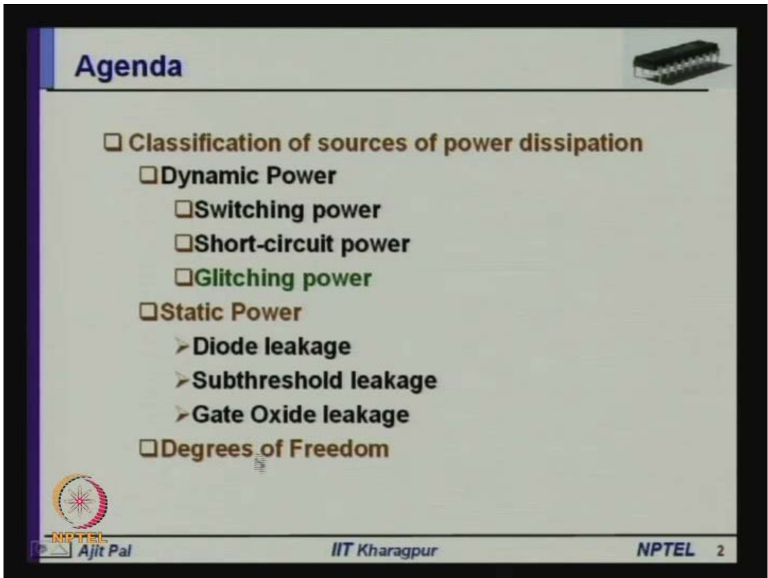

And here is the agenda of today's lecture, as I mentioned, we have discussed about switching power dissipation or short circuit power dissipation. And as part of the dynamic power dissipation, there is another component which is known as glitching power, so that was left out. So, today I shall discussed about this glitching power dissipation after that we shall focus on static power, which are essentially leakage power, different types of leakage currents that flow within the geometry of the CMOS transistors.

And the this leakage power can be broadly divided into three types, diode leakage, sub threshold leakage and gate oxide leakage. So, I shall discuss about these three types of leakage power dissipations, one after the other after that we shall conclude our lecture; conclude this lecture after discussing degrees of freedom.

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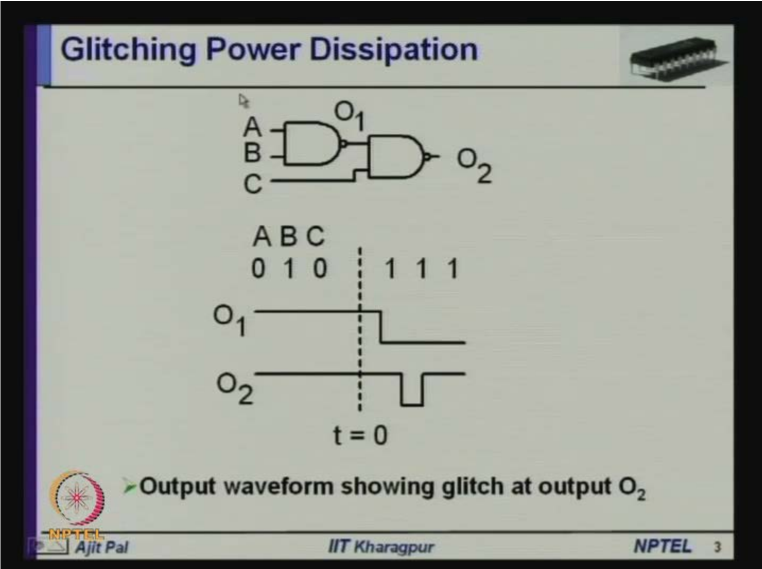

So, let us start with glitching power dissipation, earlier I have mentioned about the occurrence of glitch in CMOS circuits. As I mentioned, the glitch occurs in a CMOS circuit, because of finite delay of the gates, let me take up an example.

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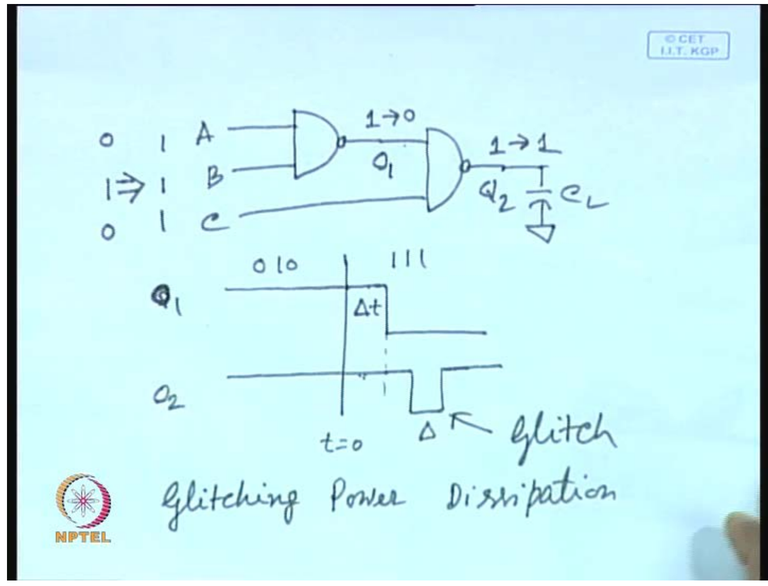

Let us consider a very simple circuit, we have two NAND gates let us assume, here is one NAND gate and this output is fate to another NAND gate to input NAND gate. Here, you are applying A and B as input and another inputs C is applied to the third gate. Now suppose, the initially the value of A, B and C is say 0 1 and 0, that is being applied and so how it will be the output at output 1 and output 2, since as you know in case of a NAND gate if any of the inputs is 0 output will be 1.

So, this output is 1 and so this will be 1 and since this input is also 0, one of the inputs is 0; output will be 1. Now, as it changes from 0 1 0 to let us assume, it is changing from 0 1 0 to 1 1 1; and what will happen, if it changes from 0 1 0 to 1 1 1 then you can see these two inputs are 1 1. So, output will switch to 0 and this input is however 1 but, since one of the input is 0, output is supposed to be 1.

So, we find that for both the inputs 0 1 0 and 1 1 1 for both the inputs, output at Q 2 is 1 but, will it be 1 throughout the time. Let us take a, I mean let us consider with respect to time how it changes, suppose, this is O 1, O 1 output is 1 and at time t 0 your input is switching from 0 1 0 1 0 1 0 to 1 1 1, so this is time t is equal to 0. And since the signal will reach after a brief period of time that means, this will switch to 0 after sometime not immediately that means let us assume, this is time the gate will require to switch from 1 to 0.

So, this is your delta, delta t or delta whatever you write. So, it will switch to 0, then of course, it will remain 0 that means here the input is 0 1 0 and here the input is 1 1 1 and it has changed from 0 1 0 to 1 1 1.

Now, what will be the output at O 2, at O 2 as you can see, this input is switching to 1 to 0 after sometime, delta t and here, what will happen at this output. So, initially it was 1, it will remain 1 up to this period but, after a gate delay of delta I mean another delta, it will become 0 for a very brief duration that is again delta, and then it will become 1.

Why this is becoming low, because for this in during this period delta t you can see, 1 both the inputs are 1 1, this input is 1 and this input is 1. Because of the delay of this gate as a consequence both the inputs are 1 1 after a delay time of this gate, it will be low for the delta amount of time. That means output is becoming 0 for a brief duration and this is typically known as glitch, and this kind of glitch very frequently occurs in CMOS circuits, because of the finite delay of the gates.

Now, as you know whenever the output switches from 0 to 1 or 1 to 0 there is some power dissipation; obviously there will be some load capacitance at the output. And this capacitor will charge and discharge; and this will lead to what is known as glitching power dissipation. So, this glitching power dissipation will is occurring, because of finite delay of the gates.

And you know momentarily the outputs are switching to, when this particular case we have seen it is switching to 0 for a few brief duration and at some point it may switch to 1 for brief duration and these are known as glitches. And this will lead to some power dissipation known as glitching power dissipation. Question arises how do you really reduce the glitching power dissipation, how can it be reduced, is there any way by which this glitching power dissipation can be minimized or reduced?

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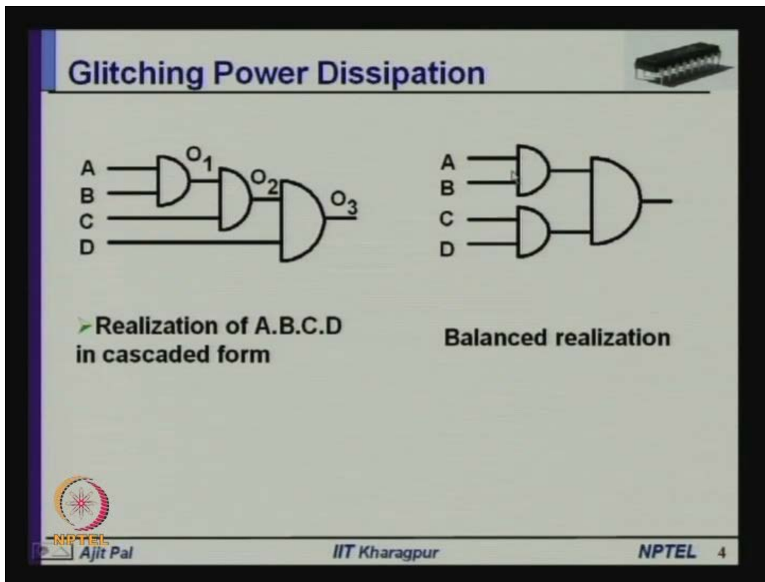

Let us have a look at this particular example, so in this case, what you to do you have to realize a n function of A B C and D. So, here at the output f is equal to A. B.C.D so, it is a AND the four variables A B C and D. So, what has been done three AND gates, two input AND gates have been cascaded to realize the function f. Now, in this particular case obviously there will some glitch at the output of Q 2, O 2 as well as at the output of O 3.

As I have only this explained, how there can be some glitch at this output and because, of the delay of this gate again, because of the delay of this gate. There will some glitch at this point that means at O 3 and O 2 there will be glitches and that will lead to power dissipation. And this is typically known as cascaded form of realization of boolean functions.

Now instead of that, we may realize the same function using, what is known as balanced realization. So, you can see, here A and B are applied to one AND gate and C and D are applied to another AND gate and then these two outputs are applied to a third AND gate. So, in this particular case we noticed that the output is actually same for both the cases, number of gates is remaining same for both the cases but, what we have achieved is I mean reduction in glitching power dissipation, why? The reason for there it is you can see at this point the signal will reach at the same time, at this point.

So, there is no delay I mean difference in delay between the two signals that will be reaching here, and as a consequence the because, of this balance realization the glitching power

dissipation is reduced. And of course another secondary advantage of this that critical path delay also you will lower in this particular case compared to this, because here the critical path is through three AND gates, here the critical path is through the two AND gates.

So, apart from reducing the critical path delay, it is reducing the glitching power dissipation. So, we may conclude by saying that, we can reduce the glitching power dissipation by realizing circuits in a balanced form. So, instead of cascaded form we shall try to realize in the balanced form, that will realize the reduce the glitching power dissipation. So with this, we have come to the end of our discussion on dynamic power dissipation.

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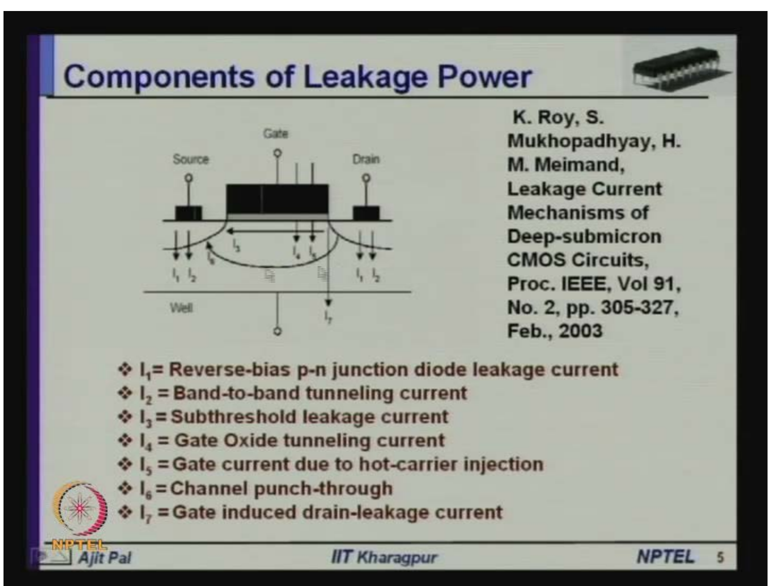

Now, we shall focus on leakage power dissipation and first, we shall discuss about the different components of leakage power. I have already told, that the leakage essentially can be divided into three types of leakage, gate leakage and that diode leakage, gate leakage and the leakage through the channel. So, there will be sub threshold leakage you can say, there will take different types of leakage currents.

Now, here we have drawn a transistor A, it can be; it may be NMOS or PMOS and does not really matter a CMOS transistor; it may be NMOS or PMOS does not matter. And here, are the different leakage currents that flow in a CMOS transistor and particularly, I have taken this from this paper by Kaushik Roy and his group published in proceedings of IEEE back in February 2003.

So, discussion on this component of leakage power is taken from this particular paper. So, here we find there are seven different leakage currents that are flowing in this transistor, so first two Reverse-bias p-n junction diode leakage current and Band-to-band tunnelling current. These two are essentially diode leakage currents I 1 and I 2 are diode leakage currents, I 1 and I 2. And I 3 which is passing through the channel which is essentially sub threshold leakage current which I mentioned earlier.

And then, there are gate leakage currents I 4 and I 5 these two are gate leakage currents gate oxide tunnelling current and gate current due to hot-carrier injection so, these two are gate leakage currents. In addition to that, there are two more leakage currents, which is known as channel punch-through, so that is, this is I 6 channel punch-through, which will flow between the source and drain. And forth the last is gate induced drain-leakage current, that passes through from the you know to the goes to the substrate.

So, through the from the channel so, here these are the different currents but, the first five are most dominant and channel punch-through occasionally occurs. And if it, if the design is not proper and gate induced drain gate-leakage current of course is present here; and I shall discuss about, these leakage currents one after the other.

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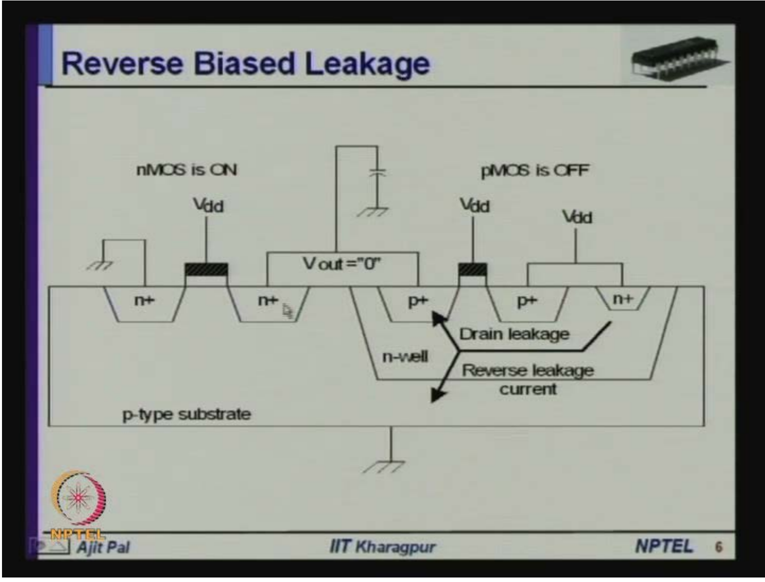

First let us focus on reverse biased leakage current, first from this reverse biased leakage current occurs, here we have got a CMOS inverter shown here. So, you can see this is the

nMOS transistor and here is the pMOS transistors realized in a n-well. So, n in an n-well the pMOS transistor has been realized and the on the p-type substrate there is a nMOS transistor.

So, you have pMOS transistor and nMOS transistor and you can see this is one gate, this is another gate, where we have applied voltage V d d to the gate inputs. And this is the output, so gates are input and this is the output and the source, and drain of the nMOS and pMOS transistors are tied together to get the output.

Now, we can see within the geometry of the device we have got junction diodes, this is the P plus type region heavily doped P plus region and this is n-well. So, you have got p-n diode, junction diode is here, also p plus region and this is n-well so, there is a diode here similarly, this is a n plus region, which is the drain of the nMOS transistor and this is a p-type substrate so, you have got n p diode. And here also there is another diode so n p diode.

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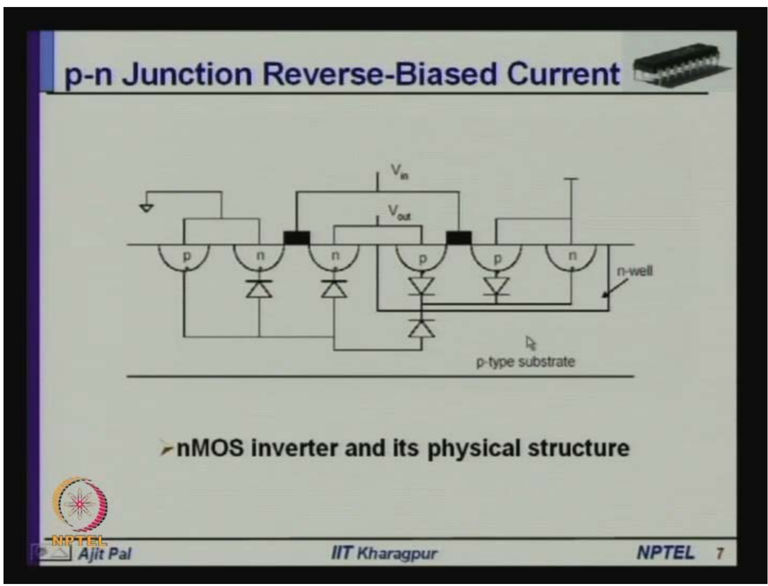

So, we can draw the diodes as you can see all the diodes are shown here, so this is the within the geometry of the device, there are some junction diodes, which are present; because, of the way the nMOS transistors are realized. And during normal mode of operation, these diodes are reversed biased, that is why it is called reversed biased leakage current.

As you know when a diode is reversed biased, some current will flow. And that reverse biased current you may call it leakage current, but usually it is known as reverse biased diode current

junction diode current. And that is essentially a leakage current in this particular context of nMOS transistors.

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And the expression for p-n junction reverse-biased leakage current is shown here, i D into I s into e to the power minus q v by k t minus 1. For I s is the reverse saturation current density, V is the diode voltage applied across the diode, q is the charge of the electron, K is a Boltzmann constant and T is the temperature in Kelvin, absolute temperature. So, you can see q v by k t and like that.

So, the current is in the range of 0.1 nano Ampere to 0.5 nano Ampere, you see this the amount of current will be dependent on the size of the junction area. So, junction area is dependent, I is actually is dependent on the junction area and that is why as the size is reducing this current will obviously reduce. But, the number of transistors will increase and because of this factor, you know that temperature the current doubles for every 10 degree increase in temperature.

So, this is a temperature dependent current now, although this current is quite small for a single diode, the since you have got millions of transistors in a single nMOS circuit. Now-a-day's, it is you have got say 100 million transistors in a single nMOS circuit, and obviously total sum total of the leakage current due to reverse biased diodes cannot be very small. Here some example is given, say total static power dissipation due to diode leakage current of 1 million

transistors is given by p is equal to V d d into summation of this i D that is 1 to 10 to the power 6, 1 million.

So, that comes to be 0.0 1 microwatt, so 0.0 1 microwatt may appear to be small but, whenever we are realizing circuits for embedded applications, which will be used as sense in sensor network where the life of the system depends on the life of the battery. In such situations even microampere of current is not more, it has to be much lower, so it cannot be neglected, when we are considering that type of applications. However as we shall see this component is low smaller than other components.

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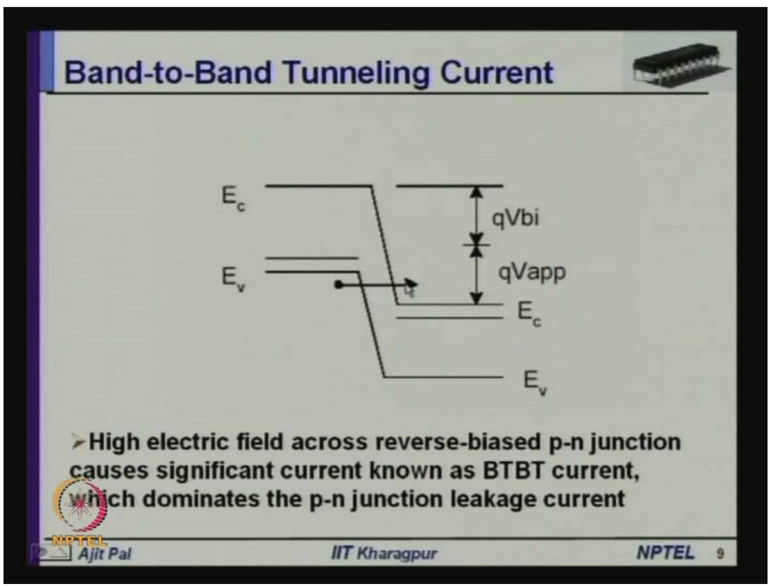

For example, there are two types of diode currents this is 1, another one is known as band-to-band tunnelling current. In fact, in deep sub-micron technologies, this band-to-band tunnelling current is becoming higher than the reverse biased diode leakage current. What is band-to-band tunnelling current? You know those diodes we are, we have told those are reverse biased and because, of reverse biased diodes a voltage is developed across those diodes.

And high electric field is across this reverse biased p-n junction diodes causes significant current known as band-to-band tunnelling current. Why you calling is band-to-band tunnelling current, here as you can see electrons are moving from the substrate to the gate, that is your polysilicon band-to-band no. So here diode is from substrate to the source or drain not really the gate, so here we have seen (Refer Slide Time: 18:36) here, diode is there.

So, across this so from the substrate to the source or drain and depending on whatever is your, so what is happening, because of the voltage drop you can see, the electrical barrier is lowered and as a result the electrons, will move from the valence band to the conduction band and as a result this there will be a flow of current.

So, because of this it is electrons are moving from one band to another band equivalency band to electron band, on the other side of the junction. This is, this will lead to a flow of current and so you can see the band gap is overcome, because of the electric field that is being applied. And these electrons will move, because of the positive voltage applied on the drain.

And as a consequence, this current is become is not very small as the geometry is gradually reduced, as the geometry is gradually reduced at electric field across the diode, can be substantial. And it has been found that, this current is dominating the p-n junction leakage current, that means in deep sub-micron technology that B T B T current, band-to-band tunnelling current is larger than the leakage currents. So, lot of attention is focused on the, for the reduction of this band-to-band tunnelling current so, this is the band-to-band tunnelling current.

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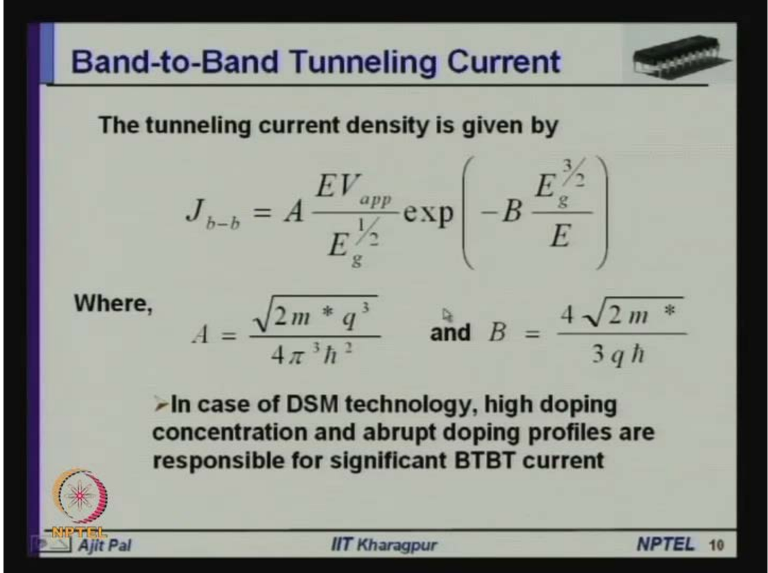

Now, Let us move to the I mean, let us consider the equation, let us not go to the details of this equation, this is a complex equation, derived from the knowledge of synchronised device physics but, from this expression you can find out it is dependence on various parameters.

Obviously, it has dependence on the voltage, it has dependence on the mobility of device, mass of the electronal hole and charge and this is h is Planck is constant.

So, that means this current is predominant, I mean only for holes not for I mean electrons not for holes. So, in case of deep sub-micron technology high doping concentration and abrupt doping profiles are responsible for significant B T B T current. As you know, whenever we are going from one technology to another technology the dimensions are reduced later on I shall discuss about it in more detail. And but to maintain constant field usually the supply voltage is also reduced but, to maintain the electric field; you have to increase the doping concentration.

So, doping concentration is being increased gradually and also the doping profile is not very smooth abrupt doping profile, because of you know, fabrication of less smaller dimension devices. And this is responsible for significant band-to-band tunnelling current. So, this is in brief discussion about the band-to-band tunnelling current.

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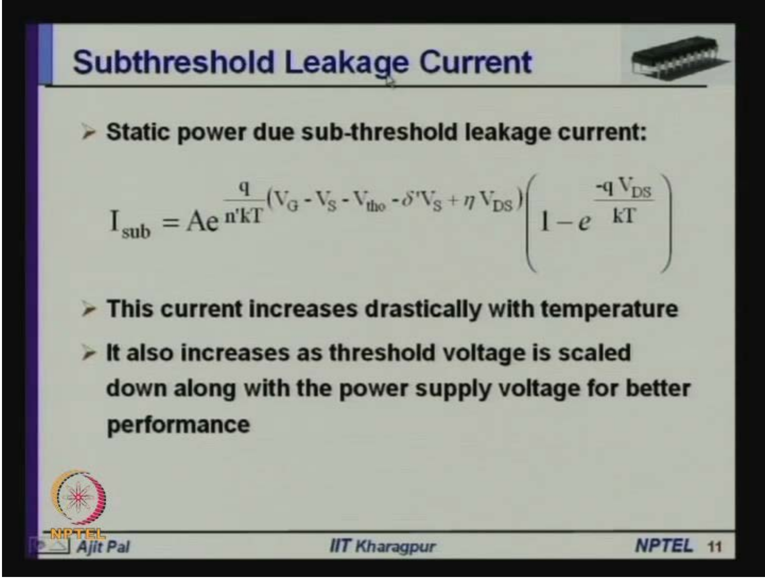

Now, let us focus on sub threshold leakage current. The sub threshold leakage current is a very significant, components of the leakage power and this current passes from drain to source through the channel.

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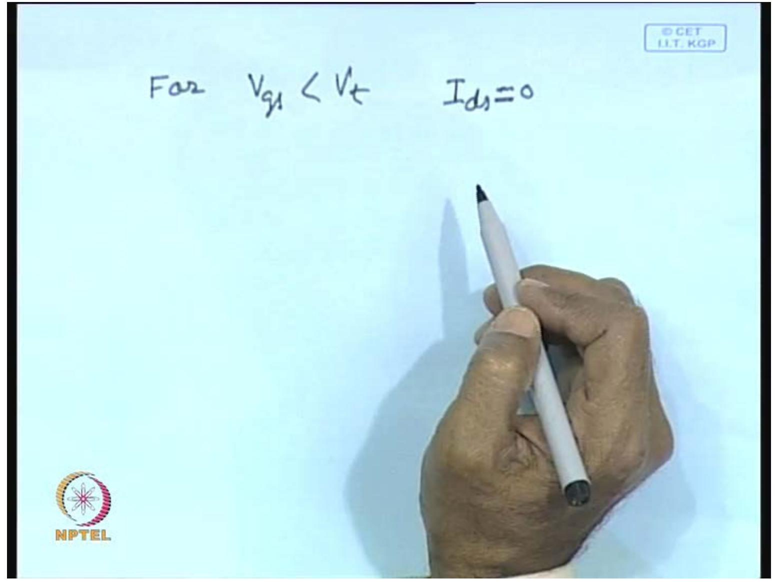

Normally, we know that, you know normally, we assume that for V g s less than V t, I d s is equal to 0 that means, there is no channel, if the gate voltage is less than the threshold voltage. And drain current will start flowing only when the gate voltage is larger than the threshold voltage of the device, but in practice that is not true. Particularly when the gate voltage is increased from 0 and it becomes closer to the threshold voltage.

There is significant amount of channel current that flows and that is known as sub threshold leakage current. Because since it is occurring for a gate voltage less than the threshold voltage, that is why the name sub threshold leakage current. So, the sub threshold leakage current is a significant component of the leakage current that flows between the source and drain.

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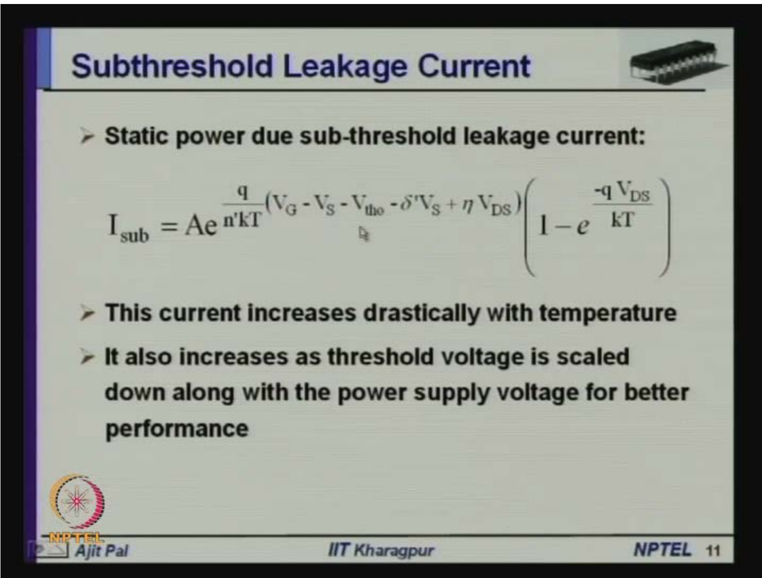

And here is the expression for the sub threshold leakage current, A is kind of constant primarily depends on the fabrication, length, width and various other parameters. Then, q be q by n das K T, V G is the gate voltage, V s is a substrate voltage and VT 0 is essentially the threshold voltage with 0 body bias, 0 bias of the, 0 bias on the substrate. And this delta das V s is the is due to the to take into account the body bias effect.

Later on you will see, I shall mention about these body effect when the substrate is not connected to the source A, if a voltage is applied it can be positive body bias or it can be reversed negative body bias. Whenever the body bias is negative, then you will see that threshold voltage is increased, when it is positive the threshold voltage will be reduced. And as a consequence, it has impact on the leakage current, I have already mentioned about this.

So, this is, this delta das is essentially, the sub threshold to take into account body effect so, this is known as body bias coefficient. And this particular parameter is to take into account the effect of dibble effect, drain to you know, whenever you apply drain voltage dibble effect, drain induced barrier lowering.

So, taking into account body effect and dibble effect, this is the expression for sub threshold leakage current. And as you can see, here also there is a dependence on the temperature q by k t and this current increases drastically with temperature and it is also increases at threshold voltage is scaled, as we know, whenever threshold voltage is reduced. You know this particular

current will increase and whenever we do device size scaling, then threshold voltage is also scaled, that means, you know.

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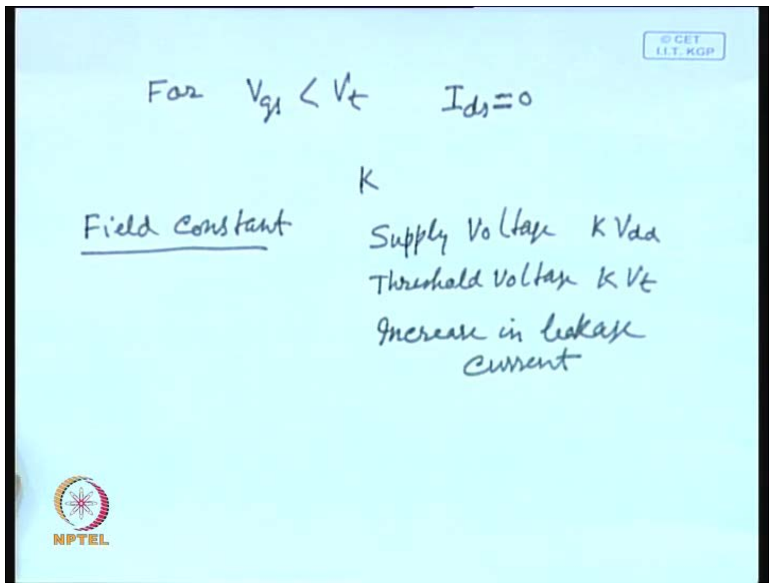

Let us consider, the situation suppose, you are reducing the dimension by factor of k, then as you reduce the dimension by factor by k, usually the supply voltage is also reduced by factor of K V d d is new V d d is K V d d. Similarly, the threshold voltage is also reduced at the same proportion say K V t. So, it is also K is a factor, reduction factor.

So, as you do that means, supply voltage is reduced to keep the field constant and as you do that to maintain performance, you have to reduce the threshold voltage. But, as you do that the leakage current increases that mean, this reduction in threshold voltage leads to increase in leakage current, that is a reason why? As the device dimensions are reduced as you go from one technology generation to the new technology generation, leakage current increases, because of the reduction in the threshold voltage.

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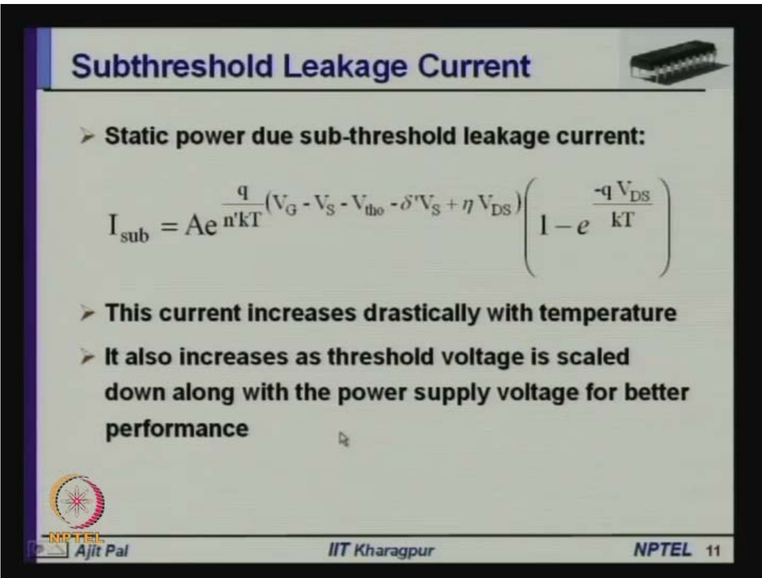

So, this has to be taken into consideration, how we can really reduce the sub threshold leakage current, this is a very important area; and then, point of concern and lot of I mean people are concentrating on how this current can be reduced. And in fact one important direction is to use high K dielectric, so that the thickness of the silicon dioxide layer is large. So, using high K dielectric the this leakage current can be reduced to some extent but, again this is another and then one way of reducing the sub threshold leakage current.

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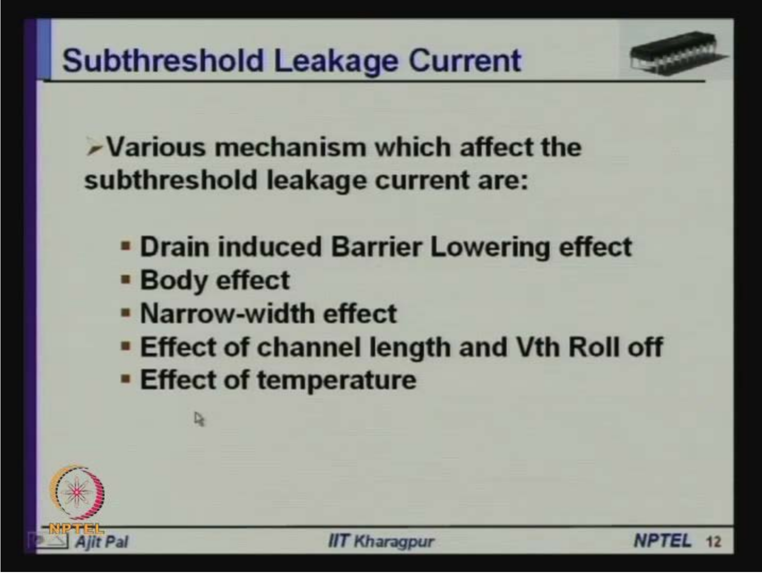

And this sub threshold leakage current has dependence on a number of parameters, there are various mechanism which contributes to the sub threshold leakage current. One is your I have already mentioned drain induced barrier lowering dibble effect, second is body effect, third is narrow-width effect, fourth is effect of channel length on and Vth Roll off and there is impact of temperature, effect of temperature.

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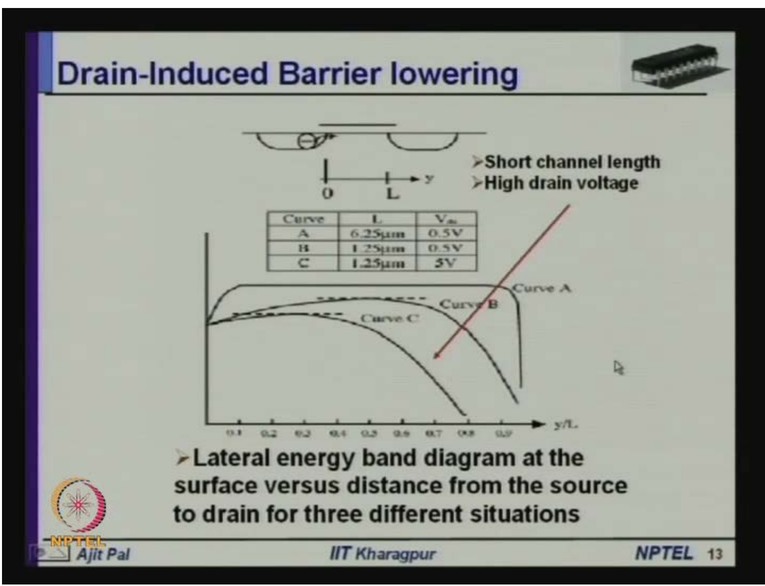

So, let us very briefly consider, how the threshold sub threshold leakage current is affected, because of these effects. First of all drain-induced barrier lowering, in this particular diagram, as you can see I have plotted the lateral energy band diagram, at the surface versus the distance. So, you can see here, this side is the source and this side is the drain so, here this is the y by L, length is a channel length.

And so as the length is on this side, we it is closer to the drain and this side, it is closer to the source and the energy band diagram is shown. Now, it is drawn for three different parameters by varying the length L and second 1 is by varying the drain voltage V D S. So, first one is you can see the length of the channel is long 6.25 micron and the drain voltage is also small 0.5 volt. So, in that case you can see curve is more or less perfect.

I mean the energy that energy band diagram is what is, what it should be and as a consequence the threshold voltage A will be, I mean you have to apply the gate voltage higher than the threshold voltage; so, that we induce channel current and so on. In other words the threshold voltage is high and leakage current will not be high. On the other hand as you can see in case of curve B and curve C, curve B corresponds to 1.25 micron length is small and supply voltage is small also.

And last one, the length is small supply voltage is large that means, whenever you have got small dimension and large supply voltage. Then you can see there is a significant lowering of the barrier of the energy band diagram, whenever there is a lowering of the energy band diagram what happens, you require lower voltage to induce current. And that leads to reduction in threshold voltage and as the threshold voltage is reduced, what happens the leakage current sub threshold leakage current increases.

So, we find that this is essentially, effect which is due to redox smaller dimension of the channel or normally we call it short channel effect. This is one of the short channel effects and it becomes predominant when the drain voltage is large; as it is evident from this diagram.

So, this is your drain-induced barrier lowering and I have already shown you the expression for the drain of, that you know that this expression, thus sub threshold leakage current where that V D S has been taken into consideration the impact of dibble induced lowering body effect, I.

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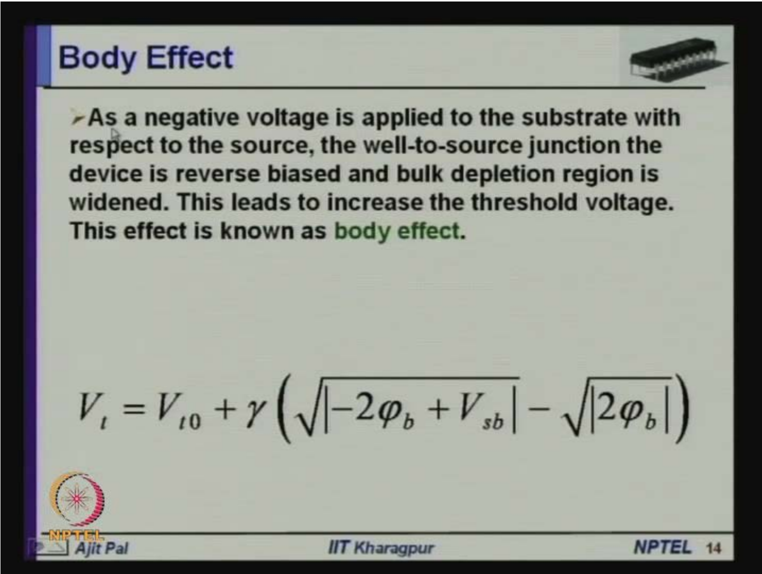

Second is the body effect, I have already mentioned about this while discussing the threshold voltage, there we have seen that.

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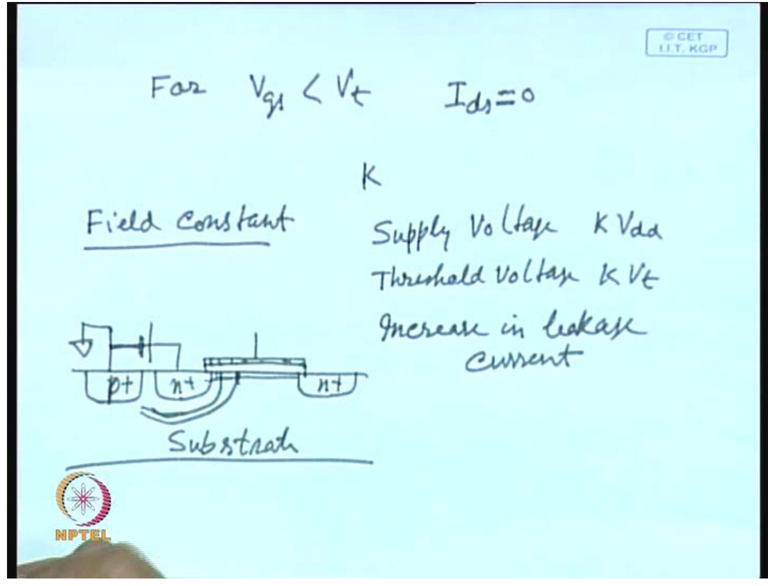

You know, instead of connecting the substrate to source for example, this is a nMOS type transistor, this is n plus n plus, this is the channel region here you got the gate, this is the gate. Now, here you have got a P plus region, which is normally, connected to source, then it is

grounded. So here this is substrate is grounded connected to source and then grounded. So in this case there is a 0 body bias now, suppose you apply a negative voltage to it with respect to source.

So, then we are calling it a reverse body bias, so you can apply a different substrate bias voltage with respect to the source. And that will actually change the threshold voltage, How it why it changes I mean the expression is there but, physically what occurs, what is a physical phenomenon? Actually as the negative voltage is applied to the substrate with respect to the source; the well-to-source junction the device is reverse biased, and bulk depletion region is widened.

So, the depletion region bulk, depletion region is widened that means, this region is there is a depletion region you know this depletion region is widened. So, whenever it is widened, it becomes wider; obviously you will require a larger voltage to be applied to the gate to induce a channel, that means the to overcome the depletion region. And to create to form the you that inverse to create the inversion layer a larger voltage is required, in other words threshold voltage is increased.

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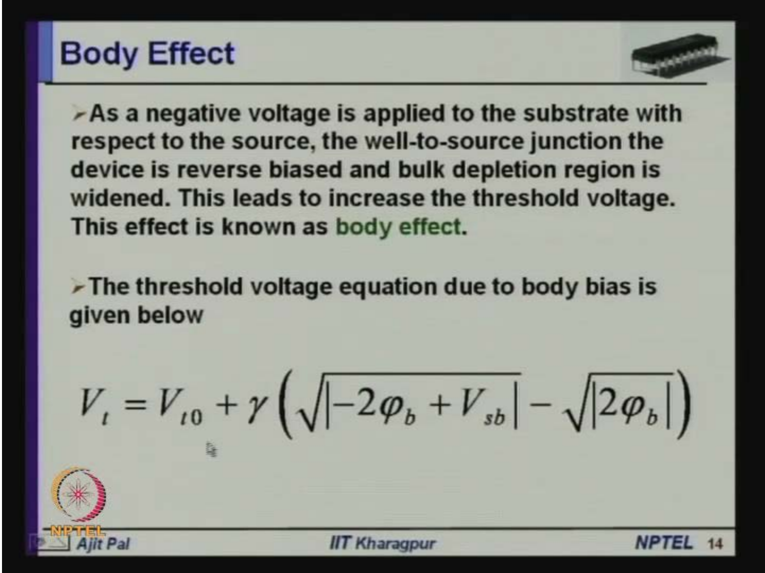

So, this is the, that is the reason why whenever reverse body bias is increased, threshold voltage is increased. On the other hand, you can apply a positive reverse voltage to substrate

with respect to the source; in that case, there will be reduction in the threshold voltage. And both you can do, but normally to reduce the leakage power it is essential to increase the threshold voltage.

So, you have to apply reverse body bias, on the other hand if you are interested in increasing the performance not to reduce the leakage current. Then, you can apply forward body bias to reduce the threshold voltage that will improve the performance. So, that also can be done, but our interest is to reduce the leakage current, so this is the body effect.

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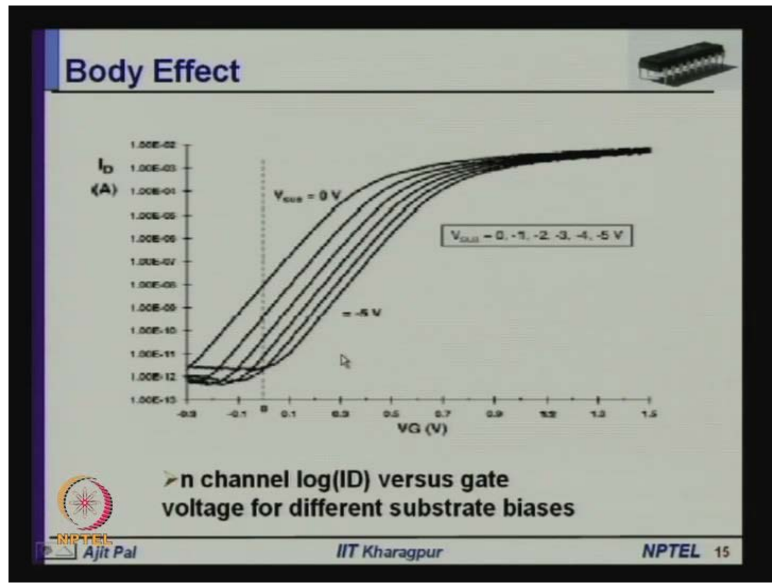

So, you can see in this particular curve, the how the body effect is changing the drain current so, here there is a plot of on the x-axis you have got the gate voltage, on the y-axis you have the drain current in logarithmic form. So, it is a kind of log linear curve, so y-axis log, logarithmic and x axis linear, that is gate voltage is linear now, you can see when the 0 gate voltage is there, even then there is a current flow.

So, there is a drain current and that drain current, when the gate voltage is 0 that means the substrate is connected to the source. Then you can see this is the current, whenever you increase the reverse body bias the substrate is connected to minus 1, minus 2, minus 3, minus 4 and minus 5 you can see, these are the different curves. And the lower curve corresponds to a reverse body bias of minus 5 volt.

So, you can see for 0 gate voltage for different body bias how the current is reducing so, this current is you can see, what is the order of magnitude difference, roughly four order of magnitude difference in leakage current. This is 1 into 10 to the power minus 12 ampere and this is 1 into 10 to the power minus 8 ampere. So, you can see four order of magnitude of reduction in leakage current is possible by reverse body biasing. So, this particular curve shows the impact of body effect on the leakage current, sub threshold leakage current.

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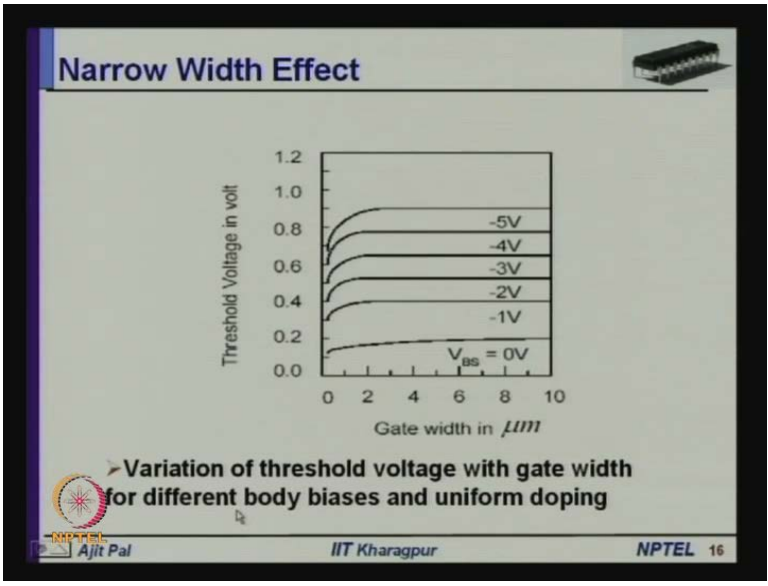

Coming to the narrow width effect you know, we have discussed about the effect of the length. Now, we have considering the effect of the width, when the width is small that too has an impact on the threshold voltage. So, here we see, how the gate width affects with the threshold voltage, you can see, when the width is large of the order of say 2 to 10 micron you can see, it has no impact on the threshold voltage. That means, threshold voltage is more or less independent of the width, so it does not change.

But, whenever it is small less than 1 micron, less than a micron you can see particularly when the gate voltage is large the body bias is body bias particularly, when the body bias is large. There you can see there is a lowering of the threshold voltage and this lowering of the threshold voltage occurs, whenever the width is small less than 1 micron and you can see the threshold voltage decreases sharply. So, because of this narrow width effect the threshold voltage is reduced and that leads to increase in the sub threshold leakage current.

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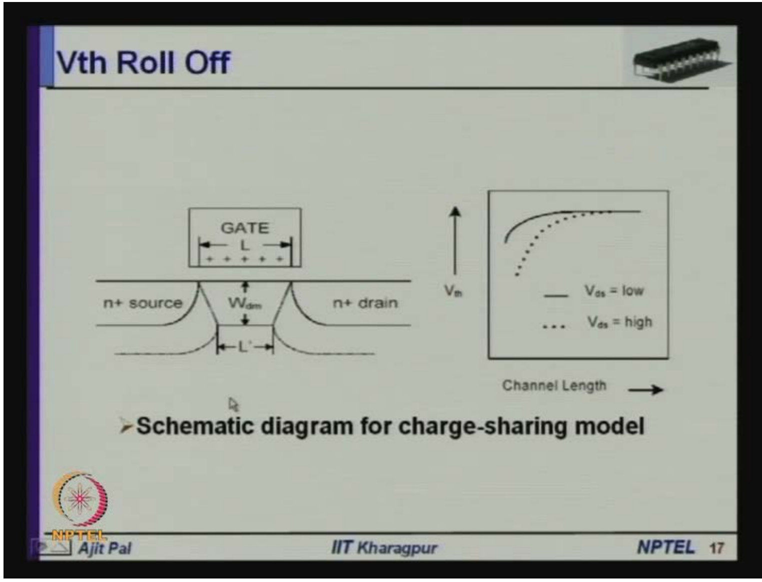

And let us consider the Vth Roll off you know normally, the gate voltage the your applying supply some voltage to the gate also, your applying voltage to the drain. As you know to attract the electrons from the source your, you apply positive voltage to the drain that is how the current flows.

Now, let us have a look at the channel region; channel region is shown here, you can see the length is L from here to here. So, from if you consider from this point to this point, this is the length but, whenever you apply a positive drain voltage, it creates depletion regions like this, these are the depletion regions. Because, of these depletion regions, it is no longer, if the channel length is no longer L in the lower part of the channel.

So, you can see it is no longer a kind of rectangle but, it takes the shape of a trapezoidal and as a consequence the effective area reduces, effective volume you can say, volume of the channel reduces. So, whenever the volume of the channel reduces what impact it has got, it has got the impact of lowering of the threshold voltage; that means, the area the volume is reduced that means you will require smaller voltage to create inversion layer in the channel.

And if the volume is then, you will require voltage to create the inversion voltage in the channel. And as a consequence what happens, when the channel you can see, when the channel length is reduced, you can see particularly this is also a short channel effect there is a kind of roll off of the threshold voltage.

And this is typically known as V th roll off that means V th roll off occurs, when the channel length is small. And particularly device dimensions are less than the are very close to the sub micron region and as a consequence the leakage current sub threshold leakage current increases, this is the Vth roll off.

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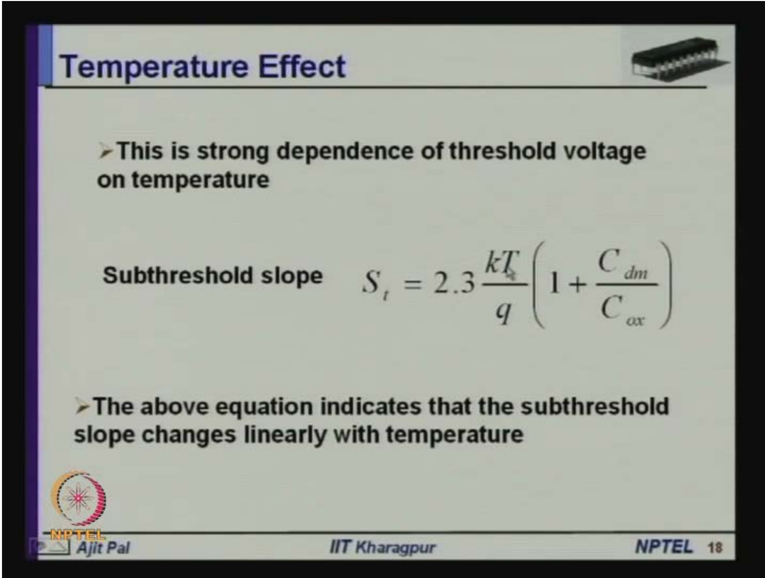

Coming to the temperature effect we have shown you, I shown you the plot of the drain current with respect to the gate voltage. And we have seen there is a slope, that slope is significantly affected by the temperature and this is known as sub threshold slope. So, there is there is strong dependence of threshold voltage on temperature particularly the sub threshold slope is affected. Sub threshold slope s t is represented by 2.3 into K T by q into 1 plus C d m by C d o x these are essentially some capacitances within the geometry.

Let us, not bother about that those are dependent on the physical fabrication parameters but, here you can see the temperature is here and there is linear dependence of sub threshold slope on the temperature.

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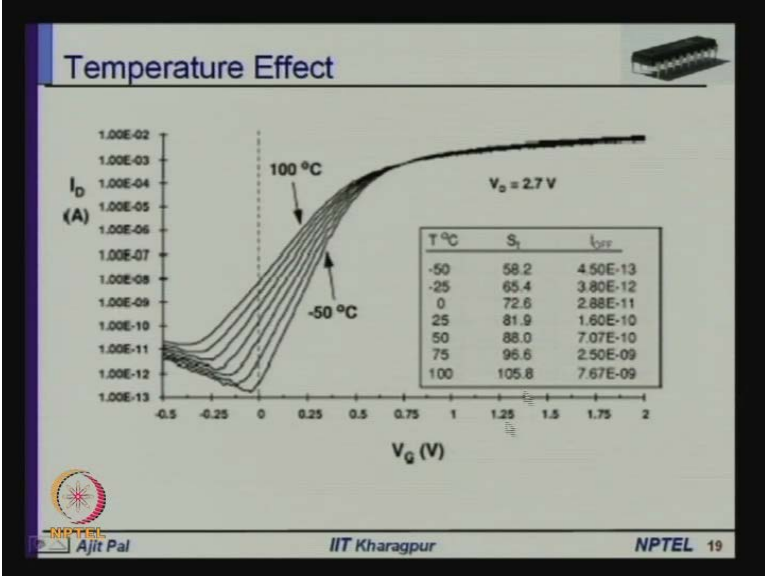

And actually this plot will illustrate it as you can see, here I have drawn the same diagram shown same plot is shown but, for different temperature. Here the gate voltage has been kept fixed 2.7 volt and on this side on the y-axis the drain current is plotted in logarithmic plot and gate voltage in linear plot, these are the gate voltages. So, you can see at 0 gate voltage, these are the different currents and lower curve corresponds to minus 50 degree centigrade, the upper curve corresponds to100 degree centigrade.

So, you can see the slope is changing as you are increasing the temperature slope is changing and as a consequence current is changing. The leakage current sub threshold leakage current is changing here also, as you go from minus 50 degree centigrade to 100 degree centigrade. You can see there is about I think 6 order of magnitude difference in the sub threshold leakage current.

So, here for minus 50 degree centigrade 4.5 into 10 to the power minus 13 Ampere and for 100 degree centigrade it is 7.67 into 10 to the power minus 9 Ampere. So, if see 4 order of magnitude 4.5 order, 4 4 order of magnitude difference in the sub threshold leakage current that is occurring. So, this is the temperature effect.

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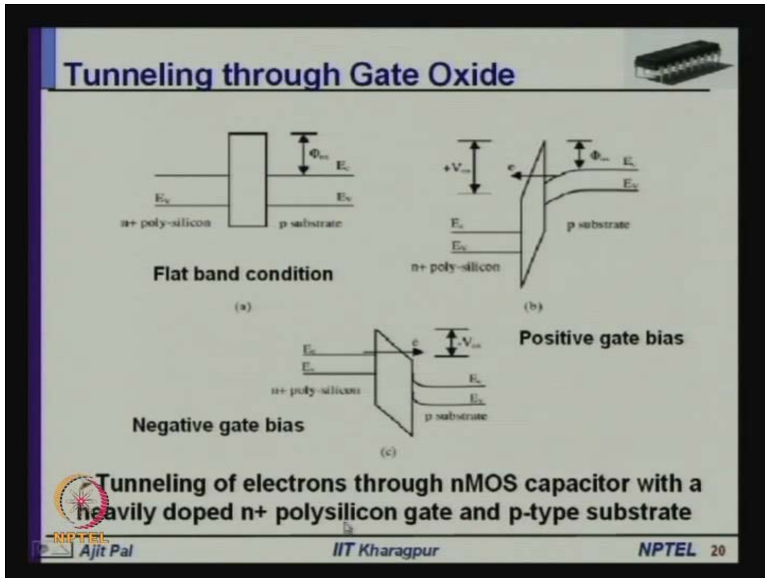

So, we have discussed about the various effects the on the sub threshold leakage current. Now, let us focus on the, those gate you know current the get oxide, gate tunnelling through gate oxide. Now, why do tunnelling occurs through gate oxide, the tunnelling through gate oxide is occurring, because thickness of the gate oxide layer is gradually reduced as you go from one technology generation to another technology generation. Length is reduced, width is reduced, the thickness of the silicon dioxide is also reduced.

In the present day technology you will surprised to know that thickness of the silicon dioxide layer is nothing but, few layers of molecules. And as a consequence, what happens you, whenever you apply a gate voltage that leads to tunnelling of current, this is illustrated with the help of this three diagrams. Here, you can see this is a flat band condition, where no voltage is applied to the gate.

Now, as you apply positive voltage to the gate you can see this is the p substrate and this side is the gate as you apply positive voltage the energy band diagram is lowered. Because, of these voltage applied to the gate and you can see electrons is passing from the substrate through the gate oxide layer to the gate.

So, tunnelling of electrons is occurring through the silicon dioxide layer, normally we assume that silicon dioxide it is a pure insulator, no current can flow through it, but this is not happening in deep sub-micron technology, because of this tunnelling through gate oxide.

And not only electrons the holes can also pass through the gate, whenever you apply a negative voltage to the gate but, because of higher mobility of holes, it is unlikely that the holes will pass through the gate I mean through the gate oxide. That means, whenever you apply a negative gate bias there is a possibility that holes will also, tunnel through the silicon dioxide layer.

But, that usually does not happen primarily, because we normally apply a positive gate voltage and because of lower mobility of electrons, they tunnel through the silicon dioxide layer. So, tunnelling of electrons through the nMOS capacitor with a heavily doped n plus poly-silicon gate and p-type substrate that is shown in this.

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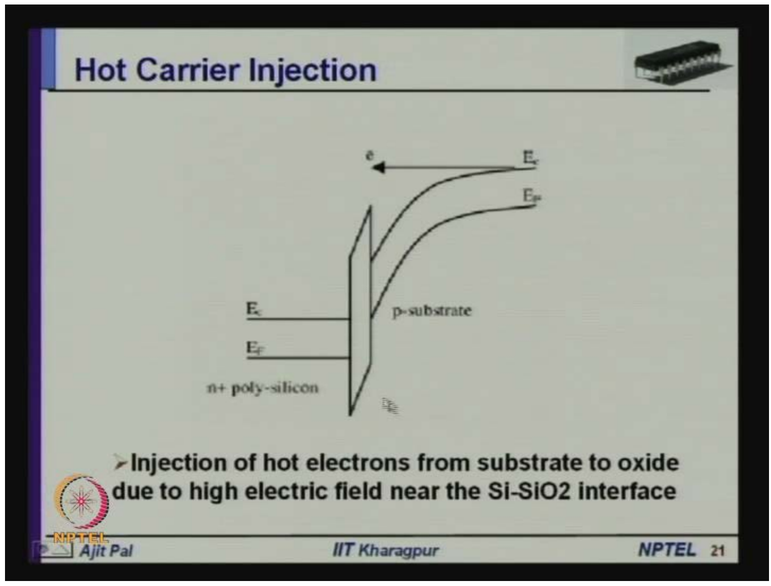

Now, there is another you know gate leakage that is known as hot carrier injection. You know, whenever you are applying a gate voltage. May be whatever may be very small, but because of the smaller thickness of the silicon dioxide layer that electric field is so, high that it creates some electrons of very heavy, very high energy. That means electrons acquire very high energy, those are known as hot electrons.

Those hot electrons acquire so much energy they can pass through the silicon dioxide layer that is, what is happening in this particular case you can see, the electrons are passing through the, because of the high electric field passing through the silicon dioxide layer going from the substrate to the poly-silicon of the gate region.

So, injection of hot electrons from the substrate to oxide due to high electric field near silicon, silicon dioxide interface, because of smaller geometry of the silicon dioxide layer, so this is known as hot carrier injection. So, these are the two phenomenon responsible for gate leakage, one is your hot carrier injection.

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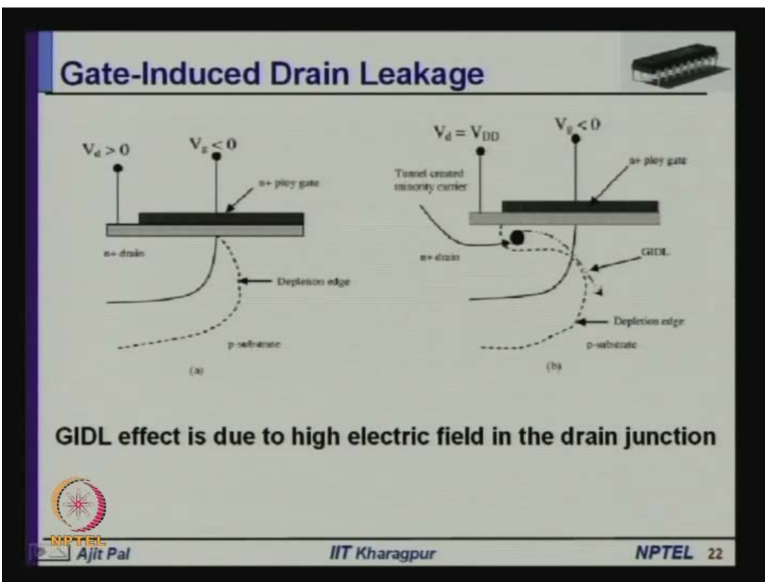

Another is your tunnelling through gate oxide coming to the another phenomenon that is your GIDL Gate Induced Drain Leakage. You know this happens, because of due to high electric field in the drain junction you can see, there is a overlap of gate and drain and here there is high electric field that leads to those electrons you can see these electrons are moving from this region going to the substrate. And that leads to current what is known as gate-induced drain leakage, this is due to high electric field in the drain junction. So, these are all arising out of short length and high electric field created, because of smaller dimension and even a small voltage can create large electric field.

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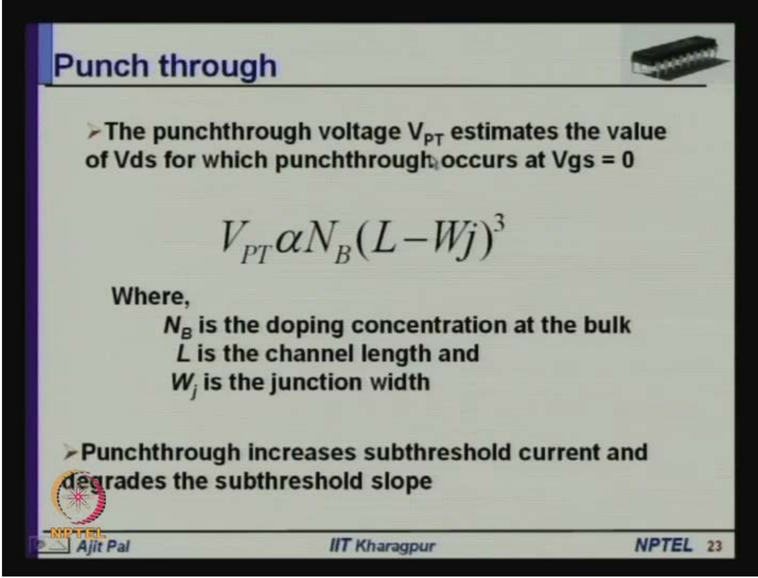

Coming to the last phenomenon that is, punch through the punch through voltage V p t let me, briefly explain what do you really mean by punch through.

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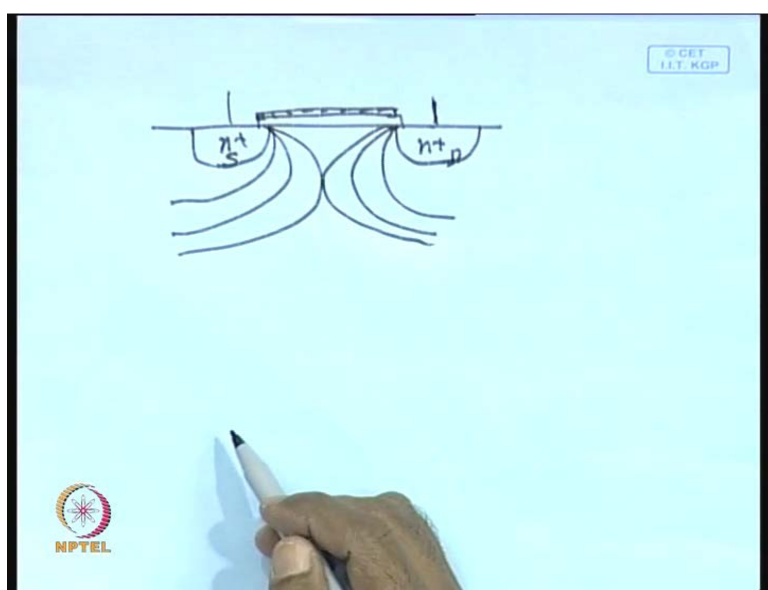

So, this is the mos transistor again I am drawing, say this is your say source n plus n plus Source, so this is Source this is drain. Now, whenever; and this is the gate region here, you have got poly-silicon layer, silicon on top of silicon dioxide. Now, whenever you apply a

positive voltage there is a there is you know, this is the depletion region now, as you increase the drain voltage what happens these depletion regions widens.

And it may so, happen that depletion regions will touch each other, this is this is know as punch through when the two depletions regions touch each other and that point we known as punch through has occurred.

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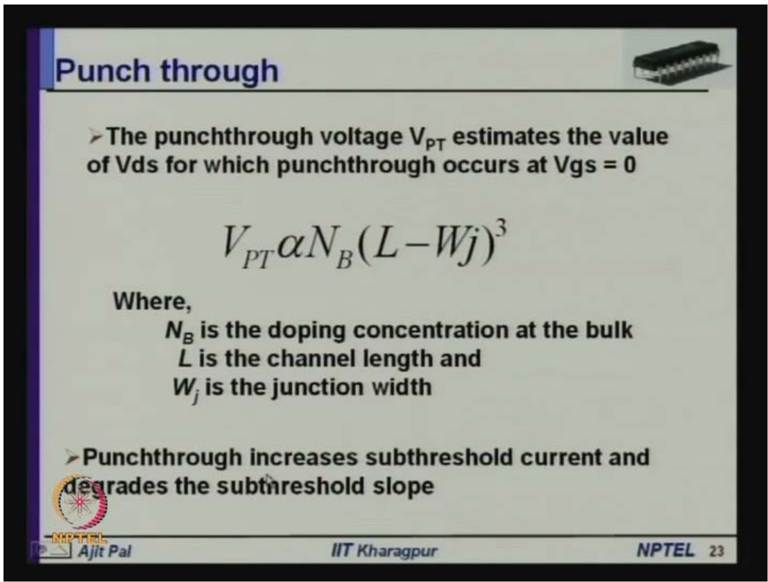

And this punch through voltage V P T the drain voltage, when it occurs estimates the value of the V d s for which punch through occurs at V g s is equal to 0. That means obviously, this punch through voltage is dependent on the gate voltage as well, when the gate voltage is small then, this is defined as the punch through voltage, when gate voltage is 0. This is represented by this expression V P T into alpha N B into L minus W j cube. So, N B is the doping concentration of the bulk, L is the length of the channel W j is the junction width.

So, punch through increases sub threshold current and degrades the sub threshold slope So, this is the impact of the punch through.

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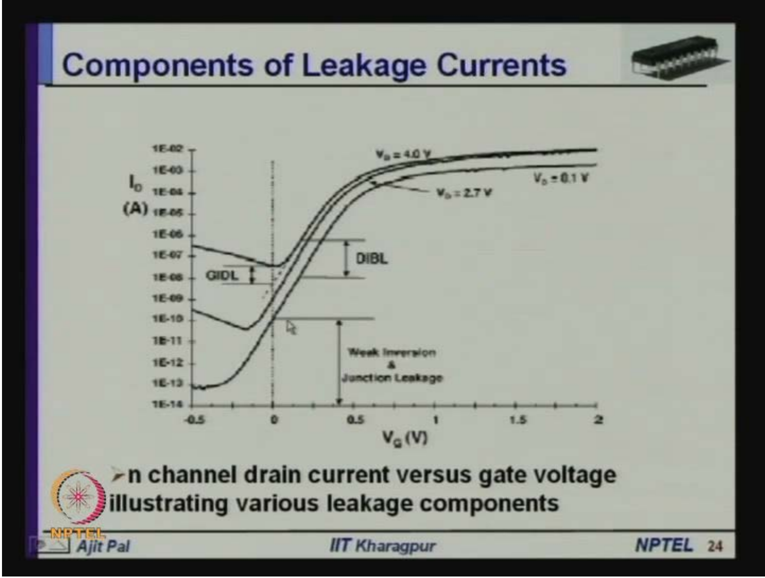

And in this particular diagram different types of leakage currents that, I have drawn explain are shown a summary of that is, shown here. For example, this is the 0 gate voltage, where there is a quadrant current, because of weak inversion, there is sub threshold leakage current and junction leakage current. And then, because of d i b l effect drain-induced barrier lowering and gate-induced drain leakage current you can see there are more currents I mean currents are increasing.

So, you see So, n channel current, drain current versus gate voltage illustrating various leakage currents components are shown in this particular, diagram for different drain voltages, it is shown. And So, you can see that we can we tell that this leakage current is very important and there are different components and these components I have explained in detail.

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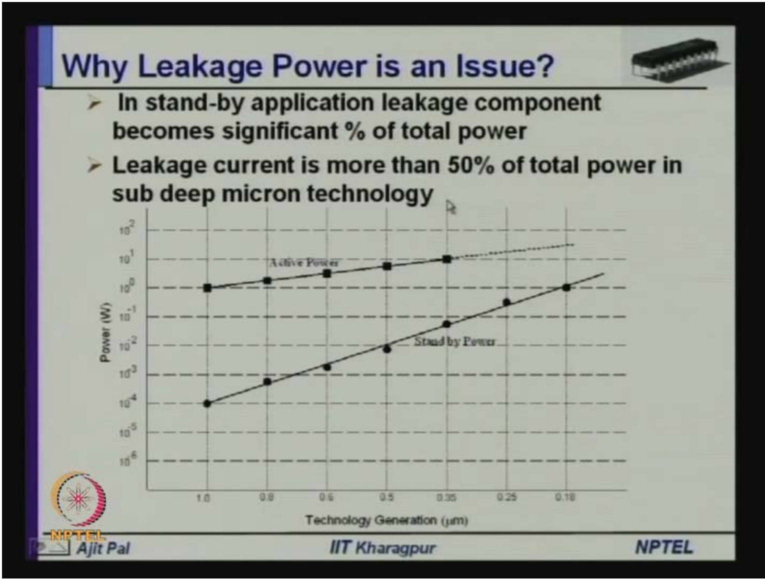

Now, let me conclude with another very important point, particularly the leakage current; you can then we I have to two lines the top one is drain current, the bottom one is leakage current or standby current. You can see the slope of this is larger than the other one that means, the leakage current is increasing at a faster rate, than, the than the active current active current or you can say dynamic current.

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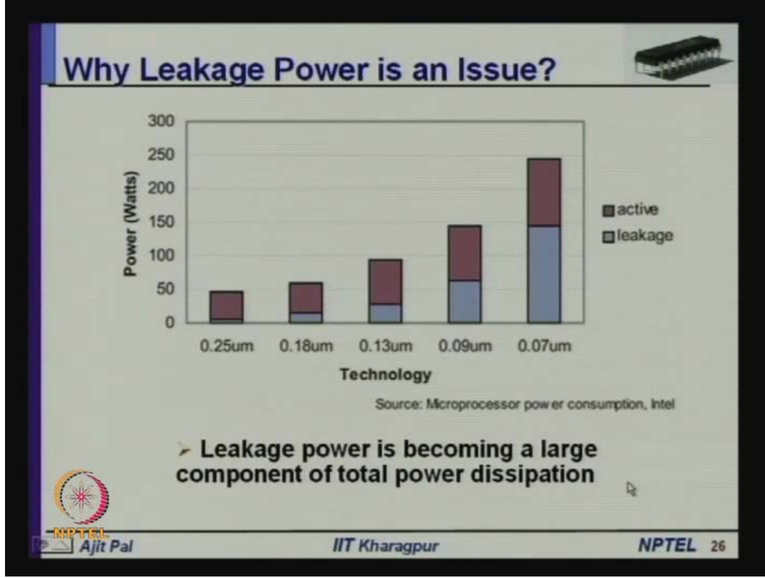

Now, leakage current it will be significantly higher, that will be more clear from this particular diagram. You can see here, for 0.5 micron technology leakage current is insignificant, but for 0.18 micron it is visible, it is significant component of the active current. But, whenever we go to 0.07 micron that is your 70 nanometre, you can see the leakage current component is more than the dynamic current component, that means leakage current leakage power is becoming a large component of the total power dissipation.

What is the impact of that? Impact of that is you have to reduce runtime leakage current; what do you really mean by that. Earlier people were developing techniques by which you can reduce the dynamic power, when the circuit is in operation circuit is active. And leakage current was reduced when the circuit was in standby mode.

But, now since the leakage current component is significant component of the dynamic power. When the circuit is active it is in runtime condition. Then, also, you have to reduce the leakage current that means runtime leakage power, reduction is becoming a very important research area in the present day context.

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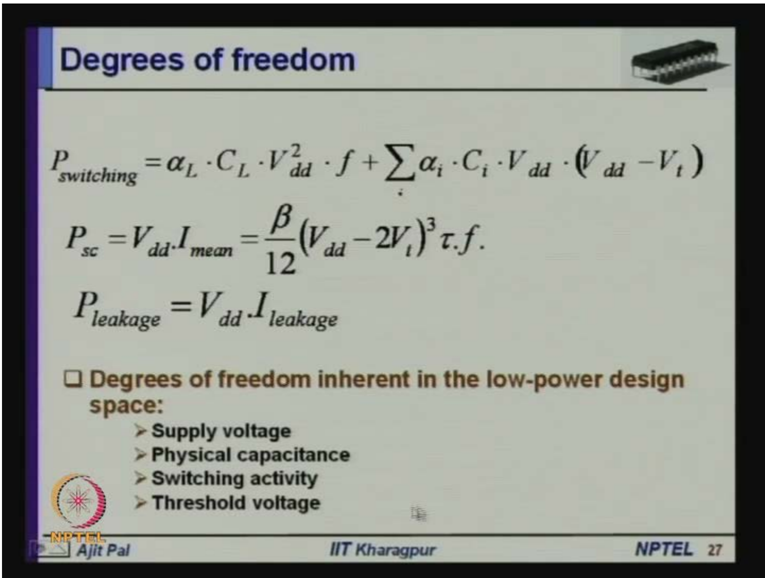

Let me discussed about the various degrees of freedom. I have discussed about different types of power dissipation, switching power dissipation, short-circuit power dissipation, leakage power dissipation. We find from these expressions different parameters are present which parameters are important rather, how can you really reduce these power dissipation. The first

and the most important one is the supply voltage, we find that supply voltage is present in quadratic form, in cubic form or in linear form, so in these all these expression supply voltage is common, everywhere it is present that is the reason, why?

Supply voltage reduction is the one of the most important technique, that is being used to reduce power dissipation. Then of course physical capacitance C L C i that has to be reduced, then switching activity alpha l alpha i reduction of physical capacitance and reduction of switching activity these two are to be reduced to reduce the dynamic power. Then, threshold voltage reduction is necessary particularly, to reduce the leakage power dissipation, we have seen that leakage power is has exponential dependence on the threshold voltage.

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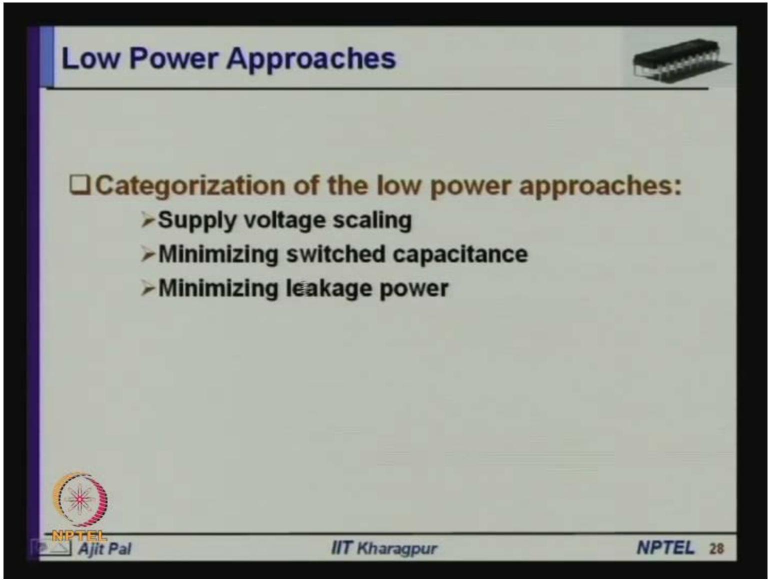

So, based on this discussion, I shall be discussing various techniques of reduction of I mean I mean low power techniques. And they can be broadly divided into three category; first one is supply voltage scaling, second one is minimizing switch capacitance. They are essentially, we shall be minimizing the capacitance value as well as the switching activity; and last one is minimizing leakage power primarily by controlling the threshold voltage. So, from next class onwards we shall concentrate on various techniques for reducing power dissipation rather low power techniques; thank you.