Low Power VLSI Circuits and Systems

Prof. Ajit Pal

Department of Computer Science and Engineering

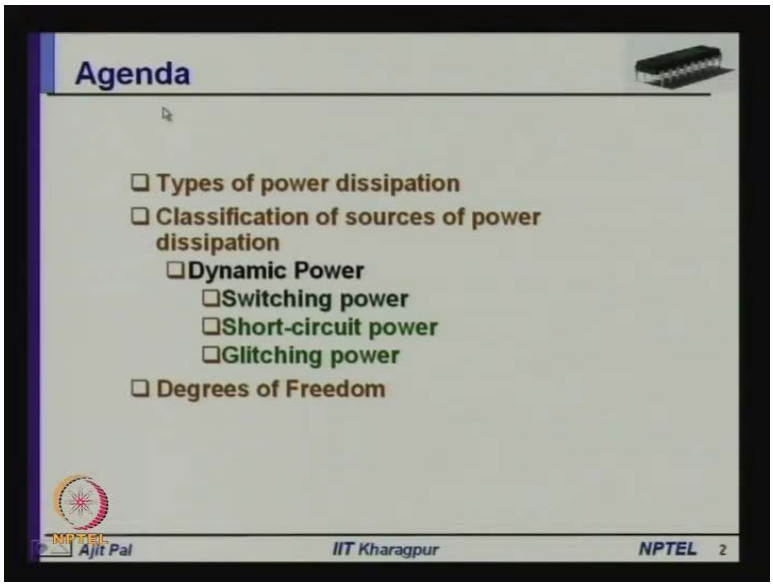
Indian Institute of Technology, Kharagpur

Lecture No. # 20

Dynamic Power Dissipation

Hello and Welcome. Today's lecture on dynamic participation. We have started our discussion on various sources of participation in CMOS circuits in the last lecture. And I have mentioned about two different types of participations; whetherr you can categorize the sources of participation into two types dynamic and static. And in the last lecture I have introduced the switching participation which is one of the components of dynamic participation. And today we shall continue our discussion on switching participation and then as we shall see later on I shall discuss about the short circuit participation which is another component of dynamic participation.

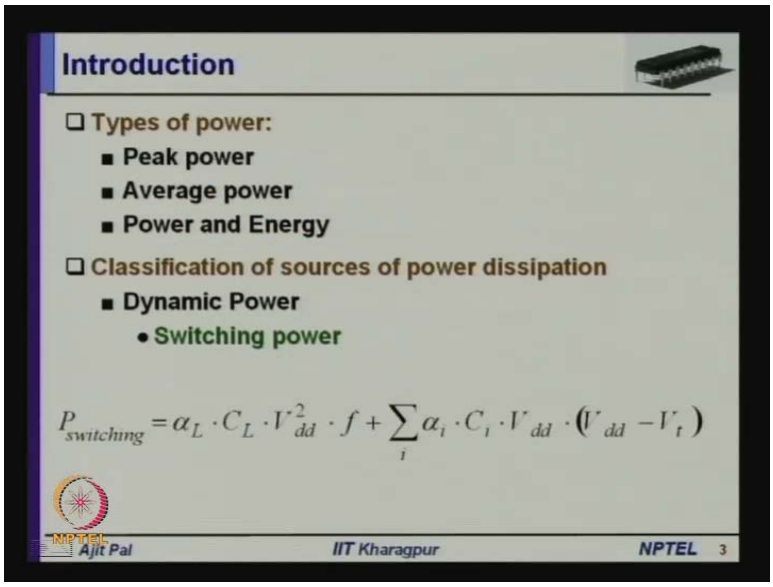
(Refer Slide Time: 01:15)



So, here is the agenda of today's lecture. Essentially I shall briefly recapitulate about the types of participation, then classification of sources of participation. As I mentioned we are focusing on dynamic power in this lecture. I have already started discussion on

switching participation and it will be followed by short-circuit participation and glitching participation. And later on I shall discuss about the degrees of freedom that means what are the parameters you can use to reduce dynamic participation rather what is your hand now in reducing the participation

(Refer Slide Time: 01:58)



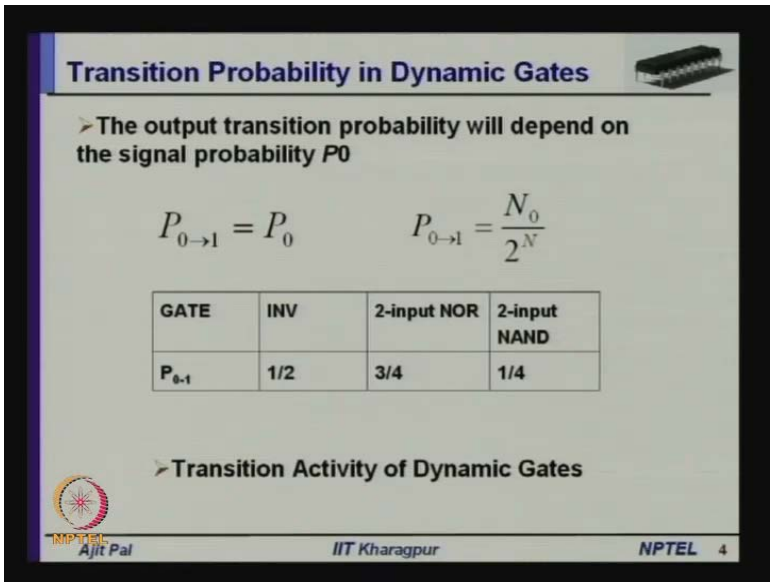
We have discussed about three types of power in my last lecture, peak power, average power and this difference between power and energy. As you know peak power is very important, because at any instant of time what is the maximum power that is being that is taken, that is drawn by the circuit in operation is very important for reliable operation of the circuit. And as you know, because of the peak power there is transience on the power lines and that may lead to glitch and error in the signal, we are not going to discuss in detail today.

Similarly, the average power is important particularly for battery operated embedded systems. Battery operated portables systems where the life of the system depends on the battery. I mean how long the battery can sustain the power and on the average how much participation is taking place that is very important. That is why most of our discussion will be based on this average participation. And I have mentioned about the difference between power and energy, as we shall see actually in case of your battery operated systems energy is the most important thing and sometimes we use power and energy. I mean without making any distinction but that is not true.

Actually, energy is the energy is very important in the battery operated systems and essentially we are talking about reducing energy that is being drawn by the portable system whenever we are discussing about low power systems. Now as I mention we discussed about classification of sources of participation, dynamic power and the most important component of this dynamic power is the switching power. And in the last lecture we have derived expression for the switching participation, and which is equal to alpha L where alpha L is the load I mean capacitive load alpha L is the switching activities C L is the load capacitance, V d d is the supply voltage and f is the frequency of operation.

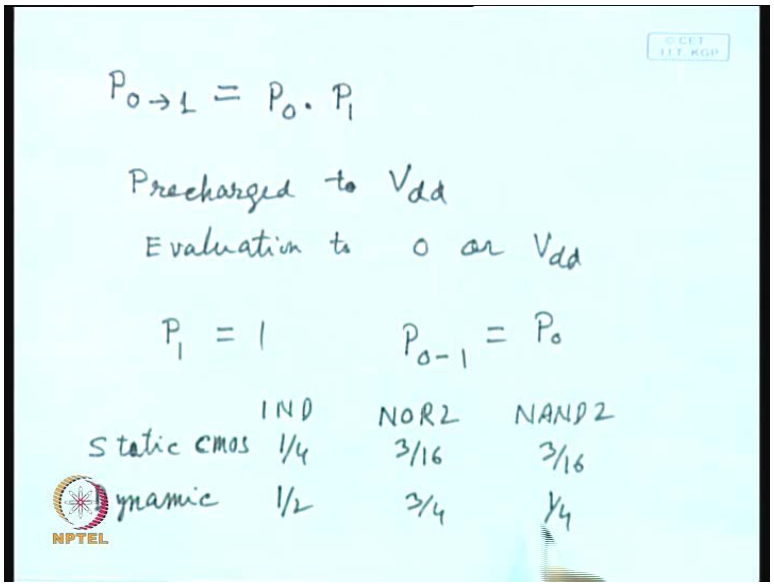
So, this is the participation that occurs because of the because of the I mean charging and discharging of the load capacitance. And so it is equal to alpha L C L V d square into f and as you have seen there are many internal loads where also participation occurs. And that can be represented by alpha I dot C I dot V d d into V d d minus V t I mean summation of all such different nodes. And you may note that here instead of V d d square there is a term V d d into V d d minus V t the reason for that is you know for internal loads the power that the supply voltage does not change between 0 to real . I mean V d d actually when you charge a internal load it can reach up to V d d minus V t and as the consequences the equation is little different from the participation of the output capacitive loads.

(Refer Slide Time: 05:30)



So, with this background now we shall focus on transition probability in dynamic circuits, we have already discussed about this switching activity of static CMOS circuits

(Refer Slide Time: 05:48)



And we have seen that the switching the switching activity can be represented by P 0 to 1 which is equal to P 0 which, where P 0 is the probability of remaining the circuit in with output 0 and P 1 probability for remaining the circuit in 1.

So, from this you can find out the switching activity in static CMOS circuits. We have discussed in neither detail how this can be calculated in difference situations and for different types of gates NAND, NOR exclusive or and so on. And also you have discussed about how the switching activity changes as we change the fanning. Now whatever about dynamic CMOS circuits? In case of dynamic CMOS circuits we know that the output is pre-charged to always output is pre-charged to pre-charged to V d d.

It is always pre-charged to V d d then of course, during the evaluation phase it may discharge to 0 or remain V d d remain output remain V d d. That means the output may make a transition from V d d to 0 or it may remain at V d d so this is how the dynamic CMOS circuit works. But in such a situation as you can see always in each I mean for each computation you have to charge the output to V d d that means what we can say that P 1 probability that the output will be 1 is always 1. And as the consequence if you substitute in this than P 0 to 1 this switching activity will be equal to P 0. That means since we are always charging to one either it may make transition to 0 or may not make

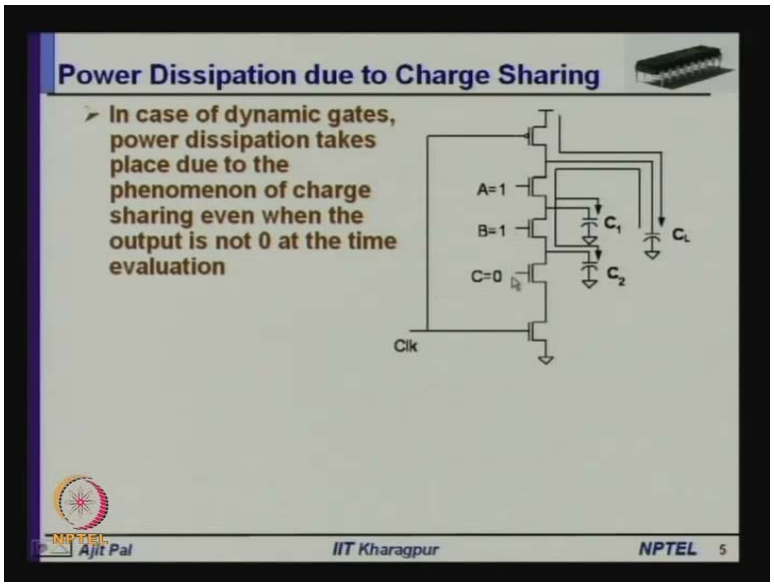
transition, that is why the switching activity is equal to probability of transition to 0 not the P 0 into P 1.

So, obviously this switching activity will be more in dynamic CMOS circuits. Because always you are charging output to1, and it may either discharge or may not discharge as a consequence the switching activity is more as you can see for different types of gates. What is the switching activity, transition activity? For inverter it is 1 by 4 and you may recall that for static CMOS circuit it was 1 by 4 not half but, 1 by 4 it was because P 0 was P 0 is half for inverter output can may become 0 or 1. And the consequence of the probability of becoming 0 is half probability of becoming 0 is also half and as a consequence P 0 that is switching activity was 1 by 4 but, in this particular case for inverter it is equal to half not 1 by 4.

Similarly, for 2 input NOR gate it is equal to 3 by 4, and because as you know in case of NOR gate probability of becoming the output 0 is 3 by 4. It will become you know whenever for NOR gate whenever both the inputs are 0, output is 1. And so whenever anyone of the inputs are 0 I mean 1 then output is 0 and as the consequence the for 2 input NOR gate is 3 by 4 and 2 input NAND gate it is 1 by 4. And in case of the static CMOS circuits you may recall that this was equal to 3 by 4 into 1 by 4 so 3 by 16 and for 2 input NAND gate it was also 3 by 16.

That means if we compare, we find that say for inverter say for static CMOS and say dynamic CMOS, if we compare for inverter it is 1 by 4 for dynamic CMOS it is 1 by 2 for 2 input NOR 2 it is here it is 3 by 16 here it is equal to 3 by 4 for NAND 2 and 2 it is 3 by 16 but here it is equal to 1 by 4. So, we find that the for the dynamic power dynamic CMOS circuits the switching activity is more. But you may recall that I mentioned that in dynamic CMOS circuit the overall participation is less. Why so? The reason for that is although the switching activity is more but the overall capacitance is much less, and overall capacitance is less, and secondly you will see that the output is driving to one of the capacitance. I mean one of the transistors not both. I mean either n MOS or P MOS as a result the load capacitance is also less the that is the reason why although switching activity is more but the participation is usually lesser in dynamic CMOS circuits.

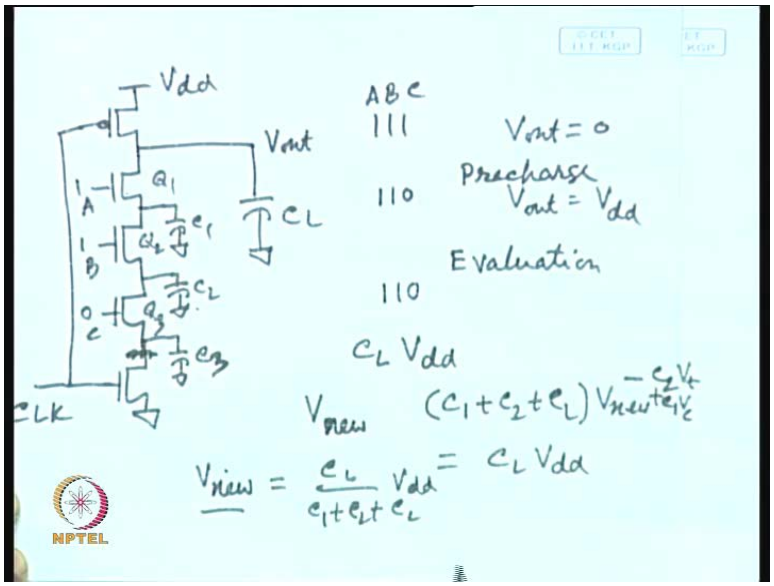
(Refer Slide Time: 11:22)



Now another very important aspects of dynamic CMOS circuits is participation due to charge sharing. In case of dynamic gates participation takes place due to phenomenon of charge sharing, even when the output is not 0 at the time of evaluation. As we know in static CMOS circuits participation, dynamic participation occurs only when output changes from 0 to 1 and 1 to 0. If the output remains 0 in consecutive computation, there will be no dynamic participation in dynamic CMOS circuits. But unfortunately that is not true in case of dynamic CMOS circuits so in case of static CMOS circuits we will find that power dynamic participation occurs only when there is out transition at the output.

But even when there is no transition at the output in dynamic CMOS circuits then there can be dynamic participation because of charge sharing. How let me explain here. So, this is a dynamic CMOS gate essentially, it is a 3 input NAND gate and as you can see in addition to the output load capacitance there are 3 you know 3 nodes 1 node is here another node is here another node is here; in third node there is also capacitance here C 3 which is not mentioned. So, let us assume that initially the input was 1 1 1 so whenever the input is 1 1 1 then the as you know the output will be output will be 0. So, all these capacitance will be discharged. Now suppose output input is 1 1 1 0 so whenever you make it 1 1 0 output will switch to 1. So, at that time this capacitor will charged to V d d during the pre-charged phage so what will happen let me redraw it to explain the operation.

(Refer Slide Time: 13:35)



So, here you have got a P MOS transistor then there are 3 n MOS transistors, because it is a then of course, there is a another transistor here which is connected to clock. So, this is connected to clock because it is a dynamic CMOS circuit it is connected to V d d and these are the 3 inputs A B and C. So, you have got one load capacitance here C L and here load capacitance C 1, then another capacitance C 2 and another capacitance C 3, 3 capacitance. So, initially you have applied the input 1 1 1 so 1 1 means this V out is 0, V out 1 1 means V out is equal to 0.

Now this second input that means at that time since the transistor is on. Let me give the name Q 1 Q 2 and Q 3 all are on then what will happen all these capacitor will be discharged not only C L but C 1 C 2 and C 3 all will be discharged. Now suppose the next input is 1 1 0 that time, you know the output is pre-charged during the pre-charge phage output is pre-charged to V d d. Now what will happen during evaluation phase this is during pre-charge. So, during evaluation phase what will happen this capacitor here the charge is C L into the charge that has been accumulated is C L into V d d.

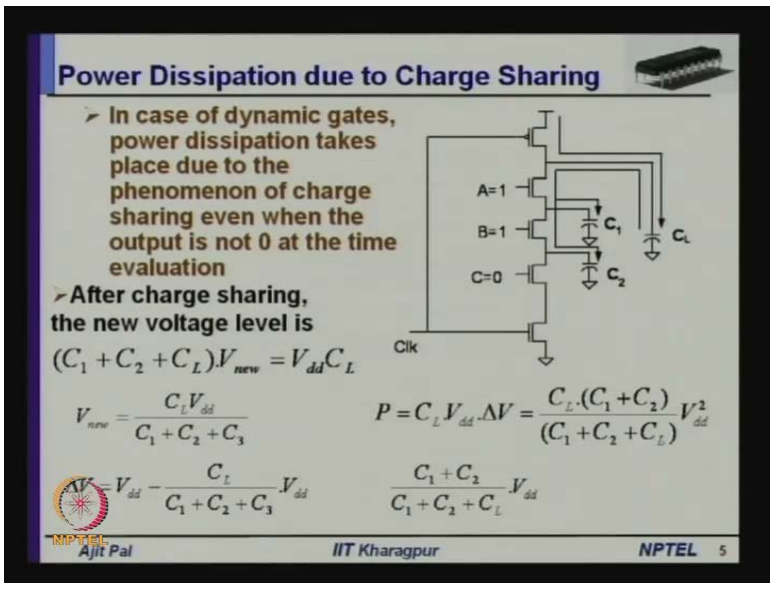
So, this is 0, this is 1, this is 1, so A B C so what will happen this transistor is off Q 3 is off but Q 1 and Q 2 these 2 are on. An as consequence since this transistor is on, this transistor is on, this charge will get redistributed in C 1 and C 2. And since earlier input was 1 1 1, this capacitor were discharge what will happen this charge will get distributed in C 1 and C 2 and as a consequence what will happen, the output will become will

because of re-distribution the output will be not V d d, say it will attain a new value V new lets assume because of re-distribution of charge.

So, how do you calculate V new. You can calculate it in the same way because by considering the conversation of charge say C 1 plus C 2 C 1 plus C 2 into plus C L into V new this is the new total charge I mean this is the total charge that will be equal to C L into V d d so V new will be equal to will be equal to C L by C 1 plus C 2 plus C L into V d d. Of course here I have not taken into consideration that this capacitor will not charge to not will not charge to V d d. But it will charge to V d d minus V dt that that of course, we can take into consideration, that means this will be here you will be having actually C 2 into V new minus here it will be C 2 V t plus, C 1 V t these 2 factors will be there.

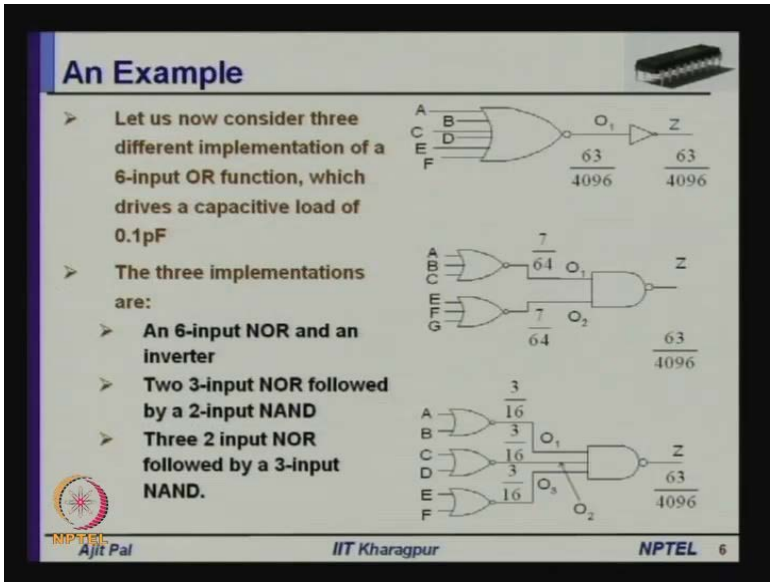
So, this you can take into consideration while computing but the main point is output will not be equal to V d d but less than V d d, it will reduce because this factor is more than C L and as consequence it will drop. Now next time whenever you apply the same input what will happen, again from V new it will charge to V d d so next time you are applying the same input. So, in case of static CMOS circuit there will be no change in the output but in case of dynamic CMOS circuit it will charge output will charge from V new to V d d during pre-charge phase, and again during evaluation phase it will be they get discharged to a new level that is your V new.

(Refer Slide Time: 18:28)



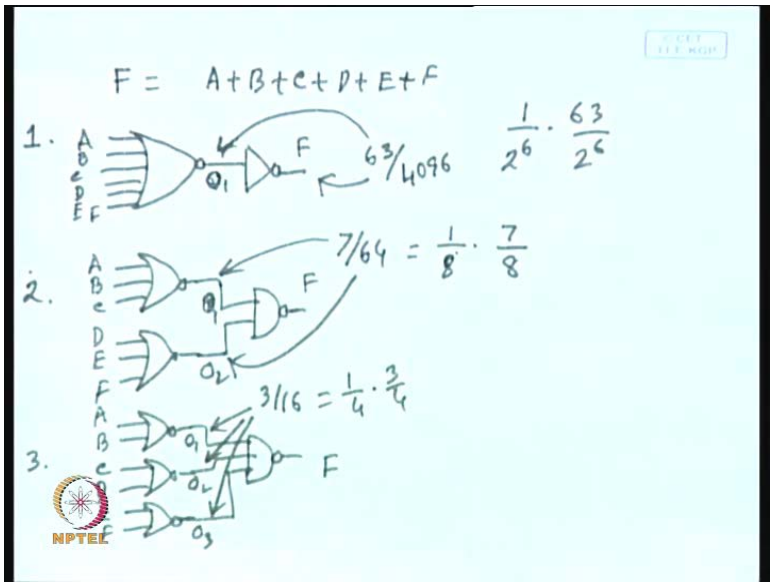
So, as consequence there will be a dynamic participation and here you can see that delta V which is the change in the voltage is equal to V d d minus C L by C 1 plus C 2 into C 3 into V d d. And that leads to that that makes difference and as consequence this is the participation that will occur because in spite the fact that you have applied these same input the there will be some participation at the output that is equal to C L into V d d into delta V that is C L into C 1 plus C 2 by C 1 plus C 2 plus C L into V d d square. So, this is a new component that is only present in dynamic CMOS circuits, that means participation due to charge sharing can occur only in dynamic CMOS circuits it is it does not occur in static CMOS circuit.

(Refer Slide Time: 19:23)



Now having discussed the switching participation in static CMOS and dynamic CMOS circuits, now let us take up an example here is an example where you have got where we have to realize a function.

(Refer Slide Time: 19:53)



That function is equal to let us assume function that you are realizing is equal to F is equal to it is a OR function say A or B or C or d or E or F so it is a 6 in put or function you are realizing. Now you can realize this function in a number of ways. So, first technique can be you will use a 6 input NOR gate 1 2 3 4 5 6 so A and then you will apply B C D E and F 6 inputs; then you will put an inverter to realize the OR function. This is the first technique of realizing your 6 input or function, second alternative is what you can do in the first stage you will have 2 NOR gates 2 NOR gates A B C you apply here A B C and D E F D E and d E and F is applied here then you will be require a 2 input NAND gate instead of inverter at the output state to realize the function F in all the cases function realize these F.

And third alternative that you can have is you can have 2 input 3 2 input NOR gates in the first stages so A B then C D and E and F so and then you will require a 3 input NAND gate. So, in all the three cases you are realizing in the same function so at the time of what is known as technology mapping you can choose one of the three configuration in realizing the function. Normally in standard cell library you will get an inverter 2 input NAND and NOR gates, you will get 3 input NAND and NOR gates so you and also you can have 4 input NAND and NOR gates and up to 6 input NAND and NOR gates.

So, whenever you do the realization in one of the in one of the three ways is there any difference in area participation. Because our main concern is participation but you have to also look into that two parameters which is power and performance. So, lets us try to compare the differences in area, performance, speed of operation and the dynamic power rather switching power that we shall compare for these three circuits and let us assume we are realizing using static CMOS circuit. So, now lets us consider to compute the dynamic power you have to find out the switching activity. So, what will be the switching activity at this point, at this point. So, here let me give the name of this node as output 1 O 1 here it is here are 2 outputs O 1 and O 2 here 3 O 1 O 2 and O 3 internal nodes and finally, we have got the final outputs.

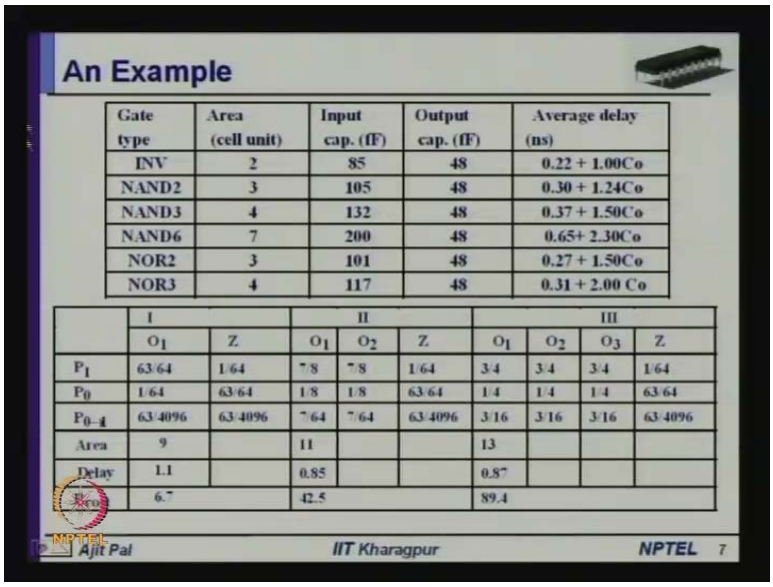
Now what is the switching activity at internal node O 1 and in the first case? As you know it is a 6 input NOR gate and as you know this switching activity will be equal to 63 by 4096. The reason for that is it will be you know 1 by 2 to the power 6 into it will be 63 by to the power 6 so that that gives you 63 by 4096. So, that will be the switching activity here; and same switching activity will be taking place here. As well because the number of transitions that will occur at this point will be same as the number of transition that will occur as this point because this is a simple inverter.

So, this is the switching activity now what will be the switching activity at this point, at this point this switching activity will be equal to 7 by 64 that we are getting because it is a 3 input NOR gate so the switching activity is equal to 1 by 2 to the power 3 that is your 16 2 to the power 3 is 8 and into 7 by 8 that makes it 7 by 64. So, same will be the switching activity at this point however at this output this switching activity will be the same 63 by 4096 because this 3 inputs are considered to be independent. Assuming that A B C D E F all are independent and they have equal probability of becoming 1 and 0 you will get these switching activities.

What about this particular case? In this particular case the switching activity at this point will be equal to only 3 by 16, that we are getting from 1 by 4 into 3 by 4 and this same will be same will be for all the 3 inputs, all the 3 points. In all the 3 points this switching activity will be 3 by 16 however switching activity here will be 63 by 4096. So, from this we observe that this switching activity of this particular implementation is much less at this point 63 by 4096. On the other hand switching activity is more at this point and at this point that is 7 by 64; and here it is still more 3 by 16 at 3 points. So, from this simple

observation we may tell that the switching activity for implementation 3 will be much more, compared to implementation one.

(Refer Slide Time: 26:08)



Now lets us have the comparison of this; so here I have taken from some standard cell line specification you can see the in area for different cells inverter NAND 2 NAND 3 NAND 6 NOT 2 NAND 3 are given here relative area so cell unit is 2 for inverter cell unit is 3 for NAND gate for NAND 3 gate the 3 input NAND gate it is 4 ,6 input NAND gate it is 7 for 2 input NOR gate it is 3 and 3 input NOR gate it is 2. So, an input capacitance as you know is dependent on the fem in so for inverter the input capacitance is 85 fem to farad and for that 2 input NAND gate it is 105 fem to farad, for 3 input NAND gate it is 132 fem to farad , for 6 input NAND gate is 200 fem to farad and the for NOR gate we can see it will be very close to 2 input NAND gate it is 101 fem to farad the input capacitance for 3 input NOR gate this is capacitance is 117.

And output capacitance however it will be same 48 nano fem to farad for all of them. Of course, here we have not this is the intensive output capacitance, you may have some output capacitance because whenever you are driving capacitive load or you are driving some on that gates then of course, the load capacitance will be more and which is expressed by this expression the average delay will be dependent on the output capacitance. So, for inverter it is 0.22 plus 1 1 into C 0 for 2 input NAND gate it is 0.3 plus 1.24 C 0 you can see this factor is increasing because of increasing fanning and for

3 input NAND gate it is 0.37 plus 1.55 C 0 into C 0 for 6 input NAND gate it is point 65 plus 2.3 0 into C 0 and 2 input NOR gate it is 0.7 plus 1.5 into C 0 so these are the average delays in nano second and for 3 input NOR gate it is 0.31 plus 20.0 into C 0.

So, based on these based on these parameter you can calculate the dynamic participation of course, we are not interested in absolute values. But we can calculate the relative values which are shown here the switching activities. I have already mentioned for the three nodes this is for implementation one the switching activity as given here at and for implementation two the switching activities are given here these P 0 and P 1 both are given and for implementation three the switching activities are also given here so the switching activity for different nodes. I have already mentioned these different values of switching activities so using these switching activities, you can calculate the dynamic participation and also you can calculate area and you can calculate delay from this.

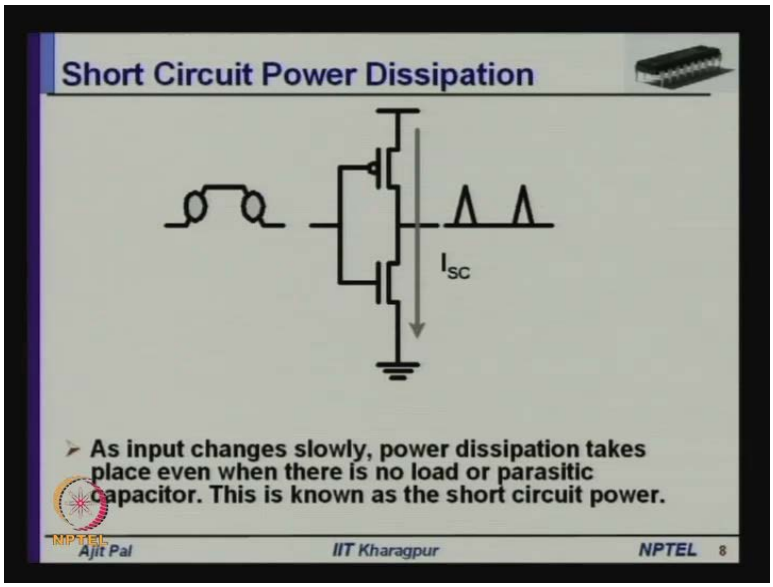
So, here is the comparison for implementation one, area is equal to 9 because you will you are requiring1, 6 input NAND gate and followed by inverter. So, 6 input NOR gate and inverter actually here it will be NOR gate I made my mistake I have written NAND anyway so it will be 9, area is 9 delay is 1.1 you can calculate delay for both the gates and using these equations and you will get 1.1 nano seconds and the participation is equal to 6.7. Participation is actually switching activity into load capacitance that has been calculated; and this is the sum of these switching activity and load capacitance 6.7. In this case and the power the participation cost is 442.5 in the second implementation and delay is 0.85 and area requirement is 11, because you are you are requiring 3 2 2 3 input NOR gate followed by 1 2 input NAND gates so 3 plus 4 into 2 that is 8 plus 311 that is given here.

And similarly, for the third case you will require 3 2 input NOR gates 3 into 3 9 plus 1 3 input NOR gate 9 plus 4 13 area unit area and delay is 0. 87 and participation cost is 82.4 for the third implementation. So, from this it is evident that although the implementation one is area efficient delay, but delay is more and participation is less that means implementation one for implementation one dynamic participation is less area required is less but delay is more. For implementation two we find that area is more than implementation one delay is less, but the participation is much higher. For implementation three participation is much larger because of higher switching activity at the three nodes, you have seen that the switching activity much more here from 3 by 3 by

6 3 by 16 3 by 16 3 by 16 and 3 by 16 at 3 nodes, these are the 3 nodes here, here and here.

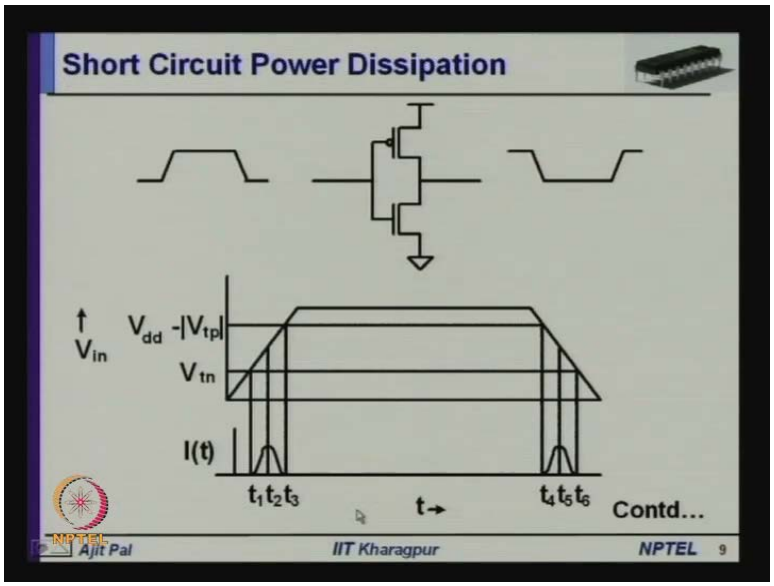
And as consequence the whenever you go for low power implementation obviously the implementation one is most suitable. But whenever you go for minimum I mean minimum delay then of course, implementation two or implementation three is important. So, this particular example clearly demonstrates that you may realize the same function in different ways by choosing different cells from the cell library. And that may give you different area different delay and different dynamic participation. So, depending on your requirement you can choose you can do the technology mapping.

(Refer Slide Time: 32:46)



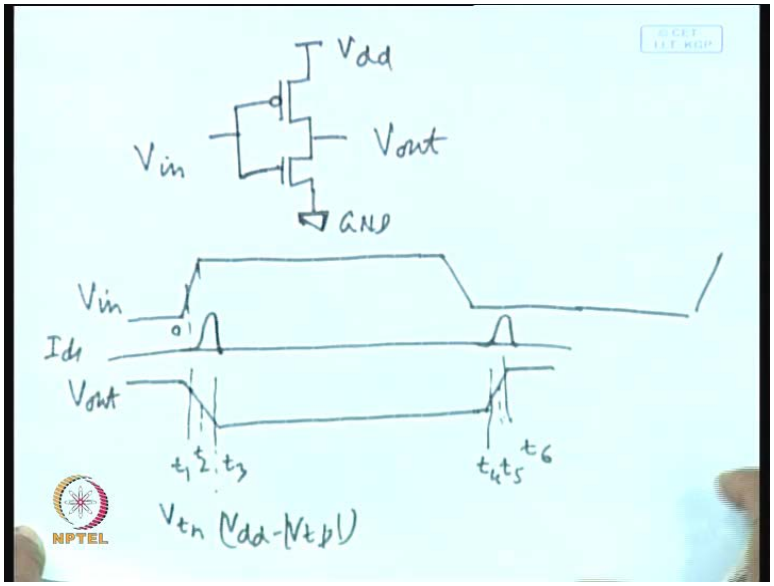
So, these example now we shall come to another important types of participation, we have switching gear to a new types of circuit that is short circuit participation. And as you already short circuit participation occurs because of slow change in the input, and particularly as the input is rising changing slowly either going from 0 to V d d or from V d d to 0 in the middle portion when the input is above the and more than the threshold voltage of the n MOS transistor. And also when it is V d d minus V t P in this part there is there is a short circuit between the supply voltage and ground. I have already mentioned about it. And then there is participation and that participation we shall compute now and this is known as short circuit participation.

(Refer Slide Time: 33:41)



So, here I have we have taken an example of an inverter although an inverter example has been taken it can it is applicable to any CMOS circuit, only difference will be instead of the P MOS transistor as pull up you will have a network of n MOS transistors in the pull up and a network of n MOS transistor as pull down. But otherwise we had known that derivation will be very similar. Now let us consider how the participation is occurring?

(Refer Slide Time: 34:23)

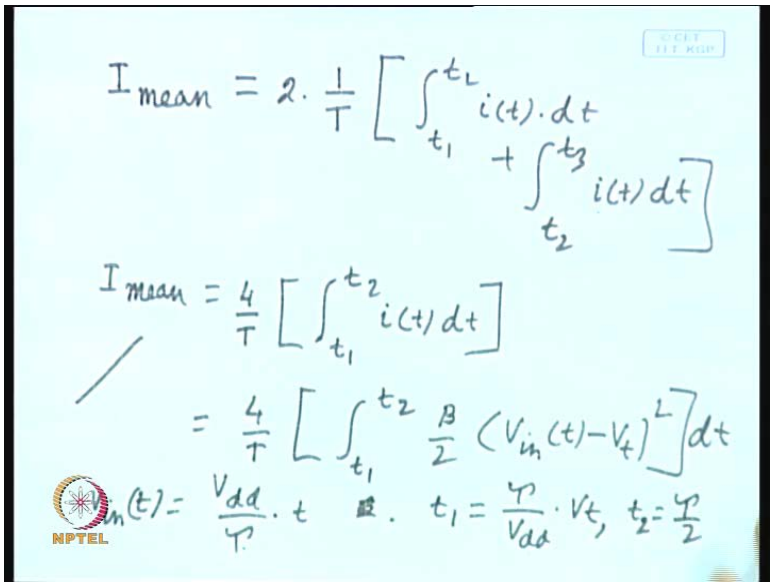


Let me redraw it so here you have got an inverter static CMOS inverter this is a P MOS transistor this is a n MOS transistor pull down and this is V d d and this is ground. So, you are applying V in you are getting V out, now say whenever you are you are changing the inputs. Let us, assume your input is like this is your input so output we will have opposite phase this is the output. So, this is V in this is V out. Now here you have got 3 points, here also 3 points. This is time t 1 when this is time I mean this is the time t 1 when the input is reaching V t n that means input is input is going from 0 to V t n, this is t 1 then the participation is starting I mean short circuit is getting established. And it will continue until your this is your this point is V t n here and this is the point corresponding to V d d minus V t P absolute value of V t P and in between of course, you will be having V d d by 2 points here also you will be have 3 points t 1 t 2 and t 3 and here say let us assume t 4 middle point is t 5 and end point is t 6.

So, during this period conduction is occurring and participation will occur. So, if you if you draw the current this is your I d s so you'll find that it will be somewhat like this. I we have already discussed about this characteristic so it will start at t 1 continue up to t 3 and again it will be start with that t 4 t 4 it will continue up to t 6 so we shall derive expression for this current. How can we derive? So, first let us calculate the current. What is the mean current? That will flow obviously, as we can see this current is not small is not is not constant it will attain peak value when the input is equal to V d d by 2 both the transistors are in saturation maximum current will flow, then it will I mean it will again it will fall. So, current is not constant so what is the average current that will flow so this is equal to 2 into 1 by t 1 by t is the period.

Period means you know in one cycle, in one cycle you'll be having one low to high and another high to low terminations. So, accordingly here you will have high to low and low to high transitions so since they are symmetric. Let us, assume that both of them are symmetric that means these two transistors are I mean their switching characteristics are identical

(Refer Slide Time: 38:04)

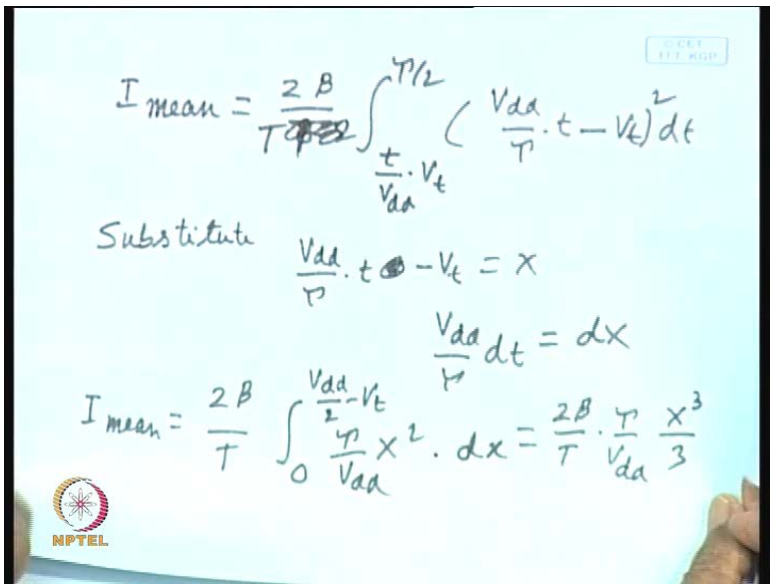


Assuming that we may write 2 into 1 by t and you can take summation from t 1 to t 2 i t into dt plus t 2 to t 3 i t into dt. So, this is the this is only for the first particular first transition since for the second transition it will be same we have we have just multiplied by 2 and then taken the average over period of 1 by T. Now what is I mean again these two can be assumed to be same so what we can say that this part if it is symmetrical that means if we divide it into two parts t 1 to t 2 and t 2 to 3 again it can simplified. It will be 4 by T and only t 1 to t 2 i t dt assuming that all the transitions are symmetric; in the sense that they will follow each of them the it may one may be mirage image mirage image of the other. For example, in this particular case this is mirage image of the other one but the current that area for both the both the both the curves should be identical so we can calculate this.

Now in this particular what will be there? I mean that we can calculate this is equal to 4 by T t 1 to t 2. What is I what is i t? Assuming that the transistor is in saturation, because we know that it is occurring when the input is above the threshold voltage of the n MOS transistor and it is going up to V d d by 2. So, during this period the transistor will been saturation so as you know the expression for current is beta by 2 into V d d minus V d d minus V t n square. So, we can write beta by 2 into V in t input in changing minus V t hole square into dt. Now what we can do we can make this substitution V in t is equal to V d d by tau into t so here what we have made one simplification we are assuming that the input is raising linearly input is raising linearly so input is raising linearly.

So, as you can sequence your V in t is called to V d d by tau, tau is the rise time and at at any instant it will be the voltage will be equal to V d d by tau into V t so in time tau it will reach V d d so at any at any instant of time t it will equal to V d d by tau into t so we can substitute this here; and this will become equal to and you can make some more substitution. So, here t what will be the value of t 1 if we substitute t 1 then it will be equal to tau by V d d into V t as we know when the input is called to V t. Then it is then time is t 1 so it is tau by V d d V t into similarly, for t 2 it will equal to t 2 equal to V d d by 2 so t 2 equal to tau by 2 because V d d will become V d d by V t by V t will be equal to V d d by 2 so V d d V d d will cancel it will be be equal to tau by 2 so this we can substitute in this expression.

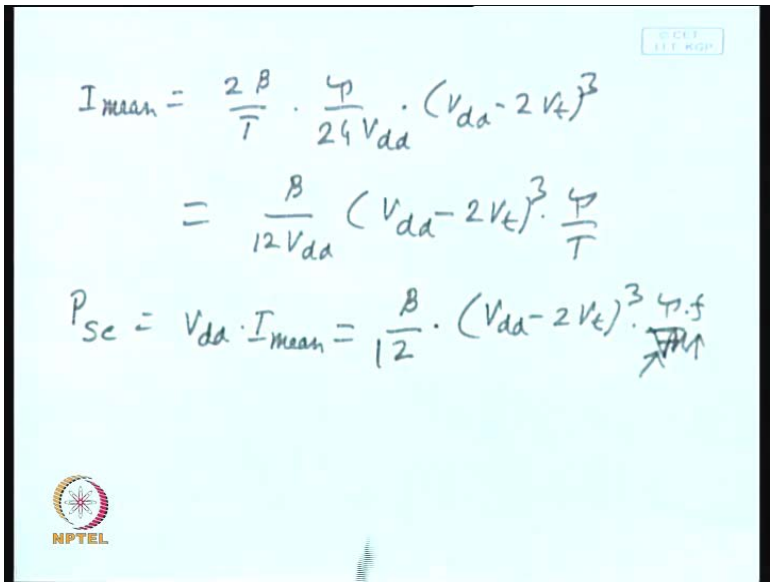
(Refer Slide Time: 42:22)



So, after substitution what we shall get is I mean is equal to 2 beta by 2, then it is will be equal to t by V d d into V t; and here it will be tau by 2 so here substituted in place of t 1 tau by V d d into V t and for t 2 tau by 2 and here it will be equal to V d d by tau into t minus V t into dt of course, here there will be square. Now again we substitute V d d by tau into t is equal to minus V t is equal to X . Then V d d by tau into dt if we differentiate that will equal to dX so this if we substitute here what will shell get here by substitute being this will become I mean is equal to 2 beta by t 2 b ta by t so this is t into it was 2 only. So, that has come from this expression 2 beta beta by that average value will be earlier it was it will be t only. So 2 beta by t into here it will go from 0 to V d d minus by 2 minus V t X square. So, this is this is X we have substituted and this is dX into of

course, this factor will be there tau by tau by V d d so then this will be equal to 2 beta by t into tau by V d d into X square X cube by 3 by after integration.

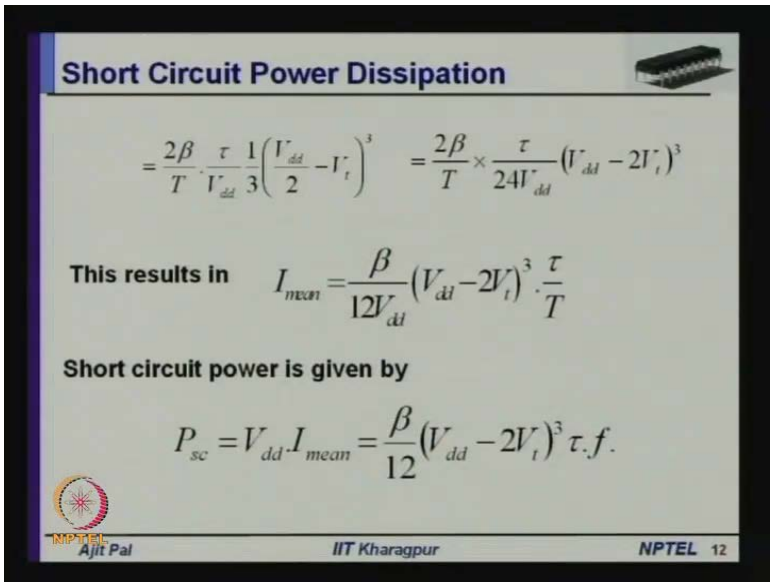
(Refer Slide Time: 44:58)



So, if we substitute X what we shall get after substituting X what we shall get this is I mean will be equal to 2 beta by t into tau by 24 V d d into V d d minus 2 V t whole cube or you can simplifies beta by twelve V d d into V d d. We have you can rewrite this 2 V t whole cube 3 into tau by t. Now this is the current so the participation will equal to P short circuit will be equal to V d d into I mean that will be equal to beta by 12 into this V d d will cancel with this V d d so we shall get V d d minus 2 V t cube into tau by t or this t can be written as f anyway so this is the expression. So, this we can write into f instead of tau so for. What does this expression tell us? This expression tells us that the short circuit participation if proportional to the frequency of the operation f it is proportion to the rise and fall time that is the transition time.

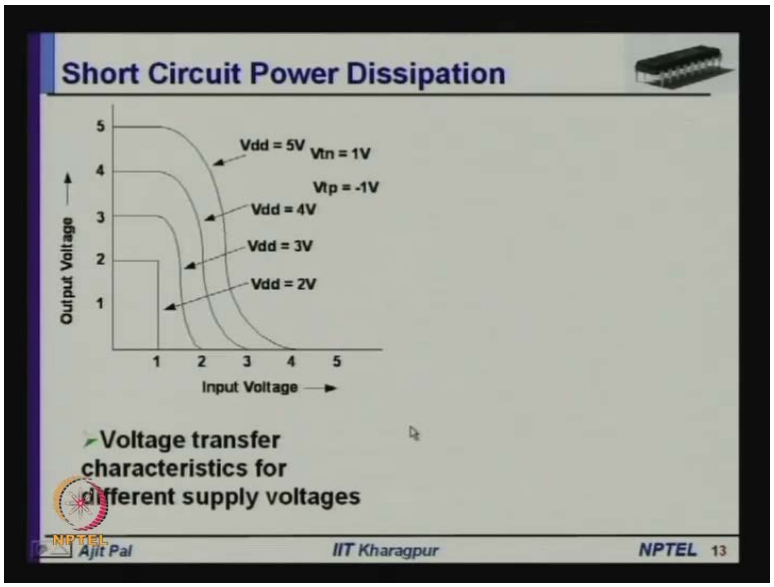
It is proportional to V d d minus 2 V t cube it is depended on this supply voltage an also it is dependent on beta. You know in beta we have the parameter that is mobility of electron then we have the parameter width of the transistor length of the transistor. So, the short circuit participation is depended on the physical dimension of the transistors, mobility of electrons and holes the transition time rise and fall time of the input and the frequency of operation and of course, last but not be least component is the supply voltage, because there is a factor of V d d minus V t 2 V t n cube.

(Refer Slide Time: 47:12)



So this is the short circuit dissipation expression

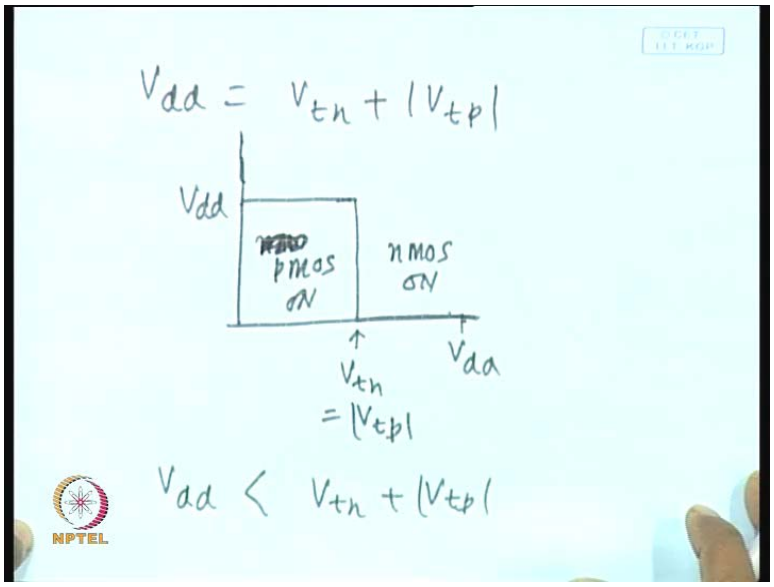
(Refer Slide Time: 47:18)



And obviously this expression this particular current is significant in some circuits when the input is changing slowly. Now as the supply voltage is reduced what impact it has got on this short circuit participation? So, here I explain the transfer characteristics for different supply voltages as you can see as the supply voltages is reduced from 5 volt to 4 volt as you mean V t n is equal to 1 volt and V t b is equal to minus 1 volt we can see

the characteristics curves will change and the region of short circuit participation of is also getting change.

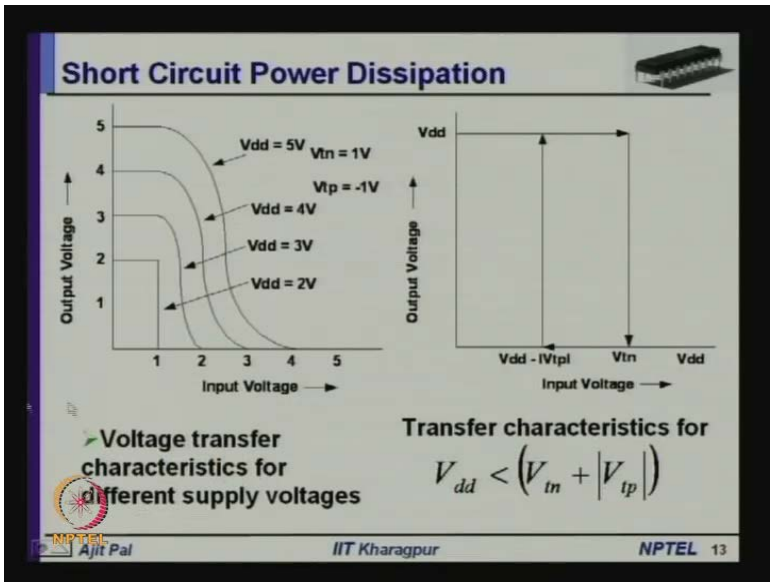
(Refer Slide Time: 48:14)



And when we are reaching when we are reaching the point V d d is equal to V t n plus absolute value of V t P. At that point what will happen at that point as you know this transfer characteristics will be somewhat like this; and this is the point where we have got V t n and also this is equal to absolute value of V t P this is the point.And of course, this is V d d. So, at this point you find there is no slow transition that means this is V d d and here it is V d d; and when the transition is occurring in the middle there it is changing abruptly and there is no current flow through the circuit. Because as at that point the initially the n MOS transistor is on n MOS this is P MOS transistor is on and here n MOS on so there is no point where both this transistor is on.

And as a consequence what will happen there is no short circuit participation so you may say that why not use a supply voltage which is equal to V t n plus V t P absolute value of V t P. But unfortunately if you do that then will see that delay will increase delay will be very high. So, although this is a way of reducing the short circuit participation but, this technique cannot be used because of high delay of the circuit. And another situation is when the input voltage is less then this that means if the input voltage is whenever V d d is less then V t n plus V t P will the circuit operate in this particular case yes the circuit will operate but, the transfer characteristics will have a kind hysteresis.

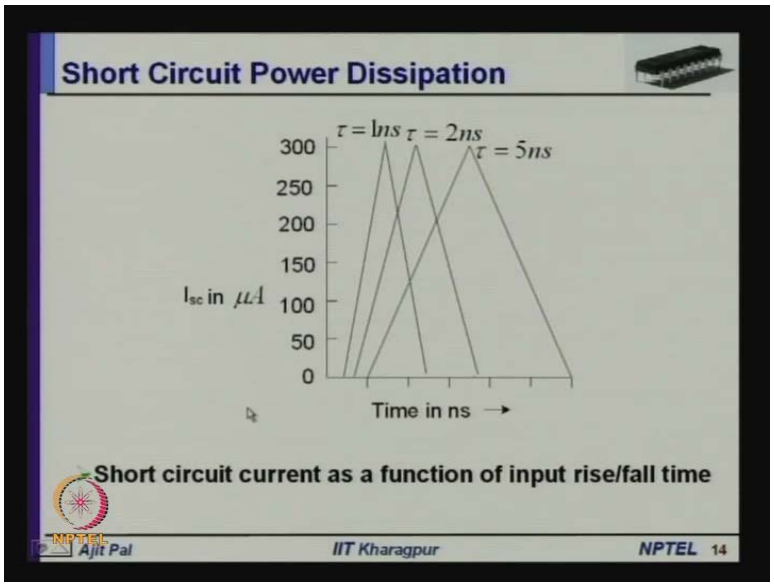
(Refer Slide Time: 50:25)



As you can see when the input is increasing it is going from say initially the output is V d d, then at point the P MOS transistor is turning off. And during this period since the output is already charge to V d d it continuous until this point when the n MOS transistor I mean turning on and output is down to 0 and then it is going to V d d. On the other hand when it is reduced from V d d to input is reduce from V d d to 0 you can see it will follow this path. So, the initially the n MOS transistor will remain on and it will remain on up to this point and then it will continue on the output will remain continue to be 0. Because output the none of the transistors are on during this period and at this point where V d d minus V t P absolute value of V t P again it will rise to V d d because the P MOS transistors will turn on.

So, you find that during this period none of this transistors are on so the between this V d d minus V t P to V t n so during this part of the curve none of this transistors are on and you will get a kind of hysteresis. If you draw transfer character if you will get hysteresis so circuit will offer it. But you will find the delay will be very high. The reason for that is you can see while in the input is increasing only for this part P MOS transition is on and during this part none of this transistors is on. Similarly, while the input is reduce from V d d to 0 during this period the n MOS transistor is up to this point and during this period none of these transistors are on and then again here P MOS transistors is turning on to bring it to one so delay will be very large.

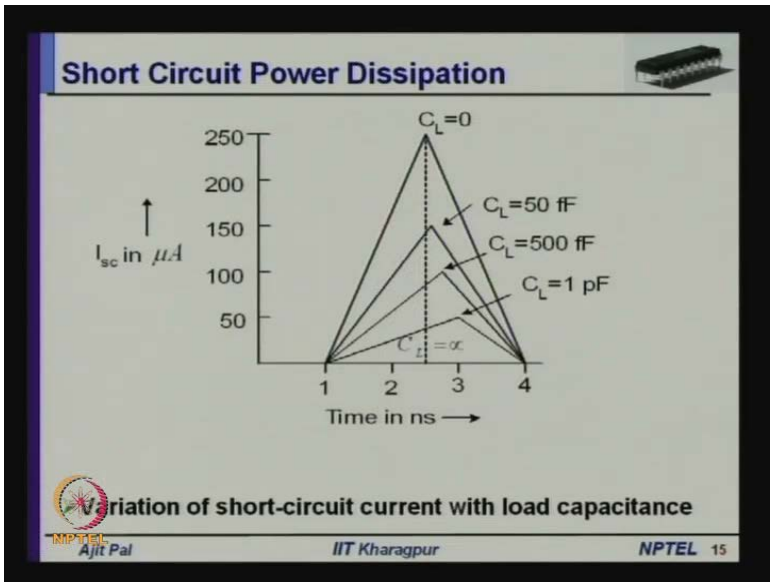
(Refer Slide Time: 52:25)



Now how this short circuit participation changes as you change the rise and fall the transition time of the input that means the value of tau we have seen that there is a dependence linear dependence on the value of tau.

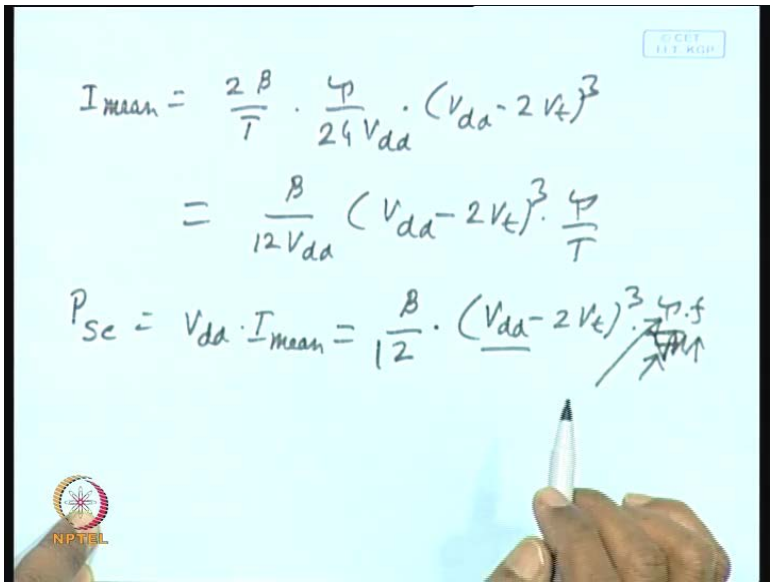
So, here you can see so how the short circuit participation will change you can see will have plated for three different values of tau 1 nano second 2 nano second and 3 5 nano seconds. Obviously, when the rise time and fall time is equal to 5 nano second that time we find that this area is much larger that means this particular the area that will cover by this triangle will be a much higher than when it is tau is equal to 1 nano second. So, this is the current that will flow for different rise and I mean rise and fall time of the input signal. So, this shows how the participation will change as you change the rise and fall time, and that is the region why we insert buffers at regular intervals in the circuit. So, that the rise and fall times are not high I mean they should be re kept to the certain limit.

(Refer Slide Time: 53:50)



Coming to a third important accept you can see we have short circuit participation for different load capacitance so initially the load capacity is 0; and then we have increased the load capacitance and you can see the it is the curve is going down because it will not charge to a higher level. But it will that go down as sequence the current that will flow will be smaller, and the area that will be closed by this rectangle by this triangle will be less. That means when be load capacitance is increased this short circuit participation gets reduced however the although the short circuit participation reduces the delay will increase. Because of increased capacitances so from this discussion, what conclusion we can make? So, for as the short circuit participation is concerned there are they we have seen there are three important parameters,

(Refer Slide Time: 55:01)



Which we can control one is frequency operation but we cannot usually compromise on performance that is the reason why we cannot really reduced frequency to reduced short-circuit participation. However can reduced tau we can also reduce the parameter that is your sometime you can reduce the load capacitance and load capacitance can be increased to reduce the short circuit participation? And of course, this supply voltage scaling reduction of the supply voltage is the most important parameter I mean important parameter that can be used to reduce the short circuit participation.

So with this we shall we have come to then of today's lecture in the next lecture we shall primarily discuss about the leakage participation but before that we shall also discuss about the dynamic participation due to glitching there is another participation that known as glitching participation that we shall discuss in the next lecture. Thank You.