**Low Power VLSI Circuits and Systems**

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**Module No. # 01**

**Lecture No. # 19**

**Tutorial - I**

Hello and welcome, to today's tutorial; in this class today we shall discuss about the class test one questions, that was more or less objective type, and it will be followed by discussion about the questions, that you will raise in this class.

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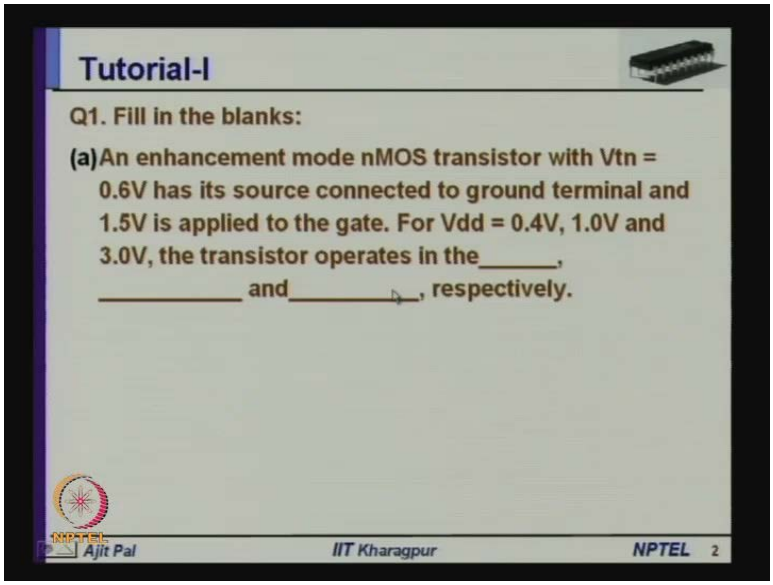


So, first question was, essentially a fill in the blanks question. It was an enhancement n MOS transistor with V t n is called 2.6 volt, has it source connected to ground terminal, and 1.5 volt is applied to gate. For V d d is equal to 0.4 volt 1.0 volt and 3 volt, the transistors operates in the dash dash and dash respectively. So, in what regions they really work, that has to be decided.

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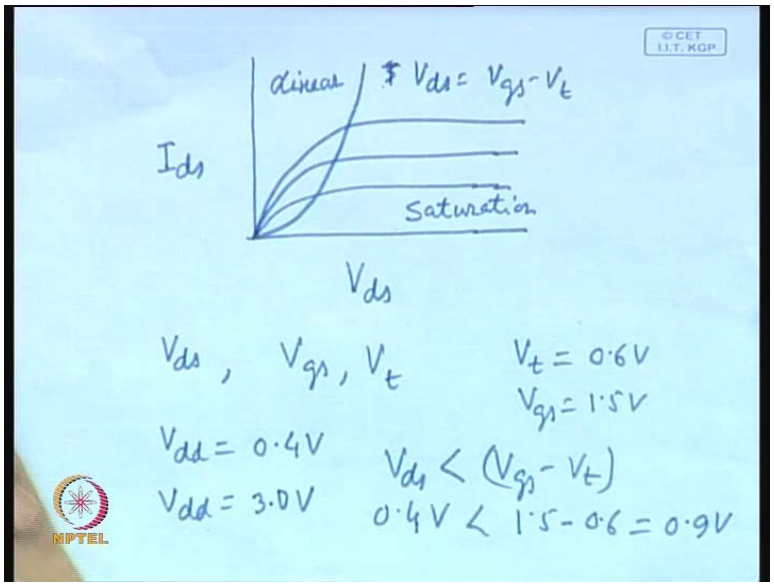


As you know, If you look at the characteristics of a MOS transistor, n MOS transistor, if you plot, say this is V d s verses I d s, current voltage characteristics, it is somewhat like this. And a line which separates this is equal to V d s, V d s is equal to V g s minus V t. So, this particular line separates the linear region with the saturation region. This part is the saturation region, and this part is the linear region. So, there are three parameter; one is your V d s, second is your V g s, third is your V t that determines in which region the transistor is operating, though in this particular problem (Refer Slide Time: 02:23) we find that your V t n is equal to 0.6 volt, and V g s is equal to 1.5 volt these are fixed; that means, V t is equal to 0 0.6 volt V g s is equal to 1.5 volt.

Now, V d s is essentially the voltage that is applied across the transistor. Now, for in the first case, when V d d is equal to 0.4 volt, then we find that V d s is less then V g s minus V t; that means, this is 0.4 volt and this is 1.5 minus 0.6 that is equal to 0 9 volt. So, since this is less than 0.9 volt it transistor is in linear region. On the other hand, in the second case when it is 1 volt, so this is more than this V g s minus V t, so it will be the saturation region. In the third case when V d d is equal to V d d is essential is supply voltage drained and source is equal to 3 volt, then also it will be saturation.

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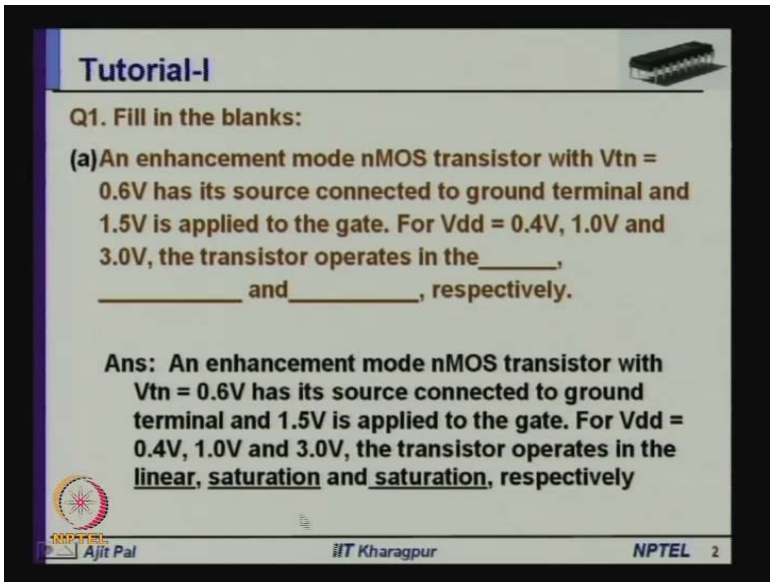


So, therefore, in this particular case the answer is, it will be in linear region saturation region and saturation region. So, this is the first question.

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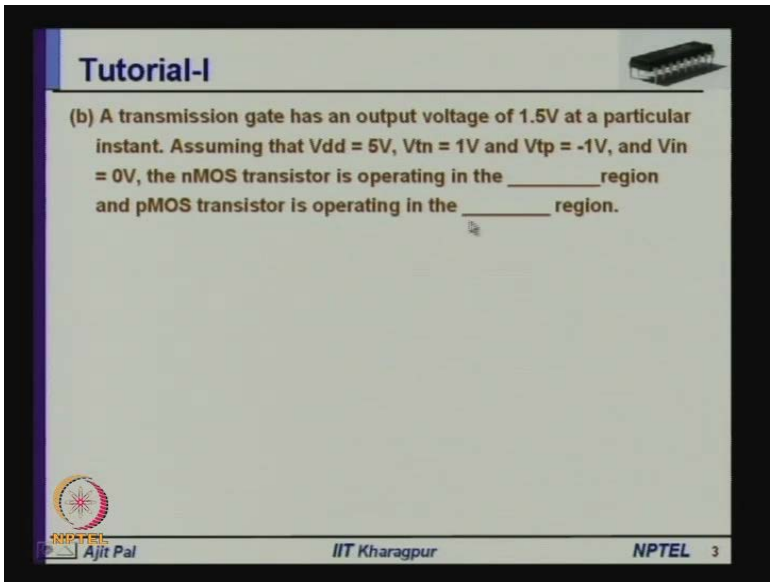


Second question was a transmission gate has an output voltage of 1.5 volt at a particular instant, assuming that V d d is equal to 5 volt V t n is equal to 1 volt V t p is equal to minus 1 volt and V in is equal to 0 volt. The n MOS transistor is operating in the dash region and p MOS transistor is operating in the dash region.

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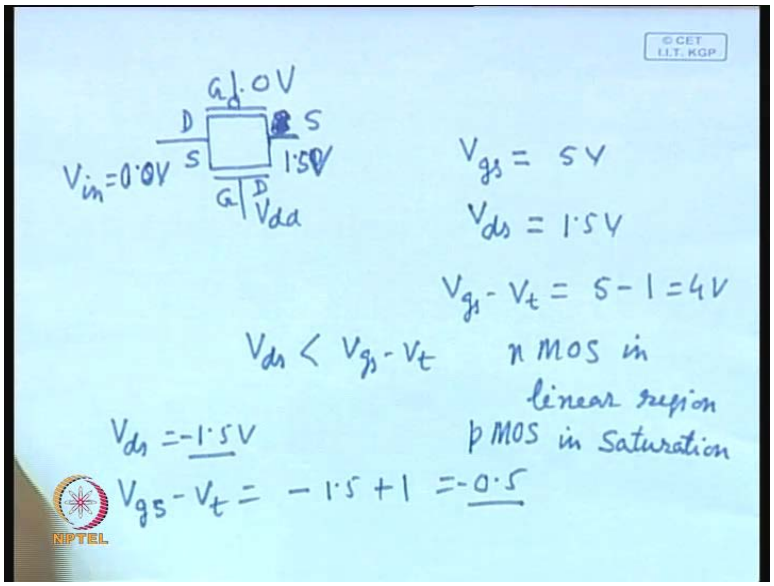


So, in this particular case you consider a transmission gate. This is the p MOS transistor and this is the n MOS transistor. Since the switch is transmission gate is on; that means, this is a 0 volt is applied to it and V d d is applied to the n MOS transistor. Now, you have applied a voltage of V in is equal to 1.5 volt here, 1.5 volt this is your this is your V in; no sorry output voltage is 1.5, V in is equal to 0 volt, 0.0 volt, 1.5 volt. So, in this case, what is the condition of this three transistors. Now, here we find this n MOS transistor, n MOS transistor we consider it as the source, this is gate, and this is drained. Now, what is the gate voltage; gate voltage V g s, V g s is equal to 5 volt, in this case gate voltage is 5 volt. And what is the drained voltage, I mean the V d s is equal to 1.5 volt, and what is V g s minus V t that is equal to 5 minus threshold voltage is 1 volt. So, it is 4 volt.

Therefore, in this case we find that V d s is less than V g s minus V t. So, what is the condition of the transistor. The n MOS transistor will be n MOS in linear region, what about the p MOS transistor. In case of p MOS transistor we find that, we can consider it as, this one as source, this one as gate, and this one as drain. So, since this is source, this particular terminal is source, and this is 1.5 volt and this is 0 volt; that means, this transistor is in the gate is more negative with respect to source. Therefore, and threshold voltage is minus 1 volt, this transistor is definitely on. Now, in which mode it will it will be. So, in this particular case you find that, the V d s is equal to 1.5 volt, and V d s is 1.5 volt minus 1.5 volt, and what about the V g s minus V t, what is the value here; V g s is

equal to minus 1.5, and threshold voltage is minus 1 volt. So, it becomes plus. So, it is become minus 0.5 volt. So, in this case what is the situation. This transistor will be, so this 1, this one is less than this one. So, therefore, this transistor will be in saturation; that means, p MOS in saturation. So, p MOS will be in saturation and n MOS will be linear region.

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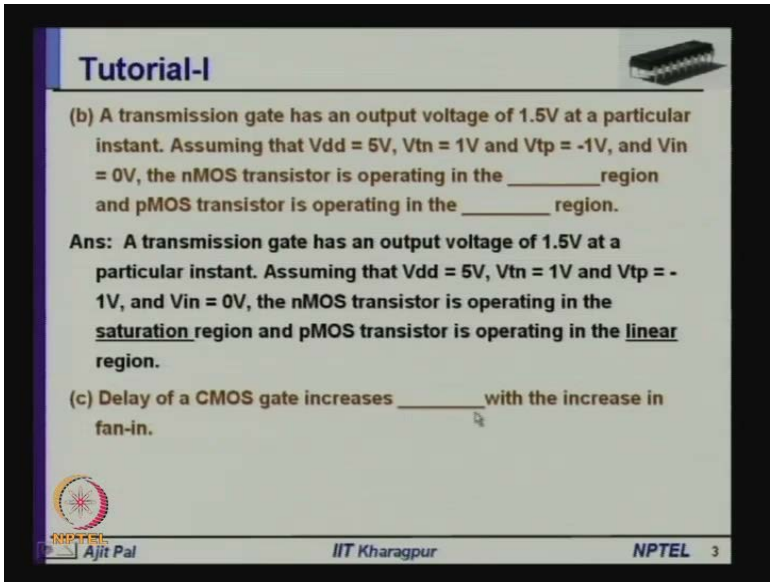


I have written it just the opposite by mistake, this here is a type of; that means, it will be in linear region n MOS and p MOS will be in saturation region. Now, coming to the third question; delay in CMOS gate increases with the increase in fan-in. So, how the delay of a CMOS gate increases, both for NOR and NAND.

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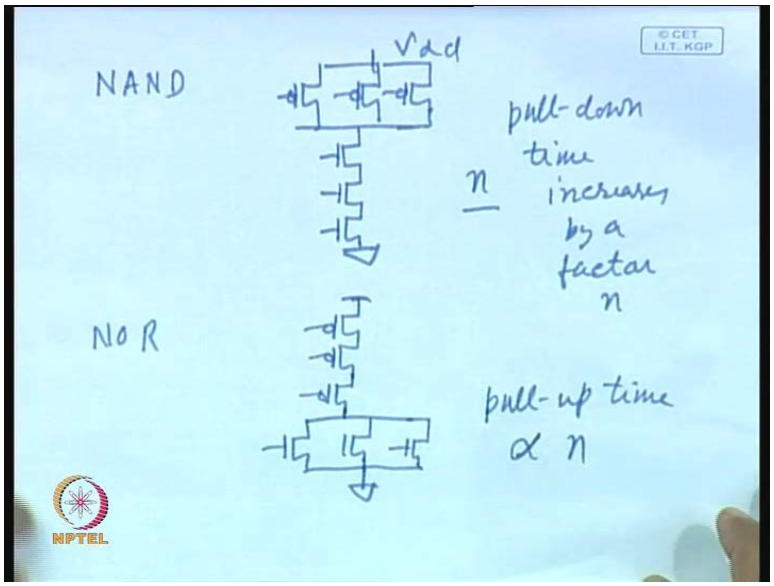


In case of NAND gate, as we know we have the n MOS transistors in series in case of NAND gate. So, here it is V d d, I have drawn a 3 input n gate. So, how the delay increases in this case, delay as we know is proportional to n if n is input, therefore I mean the pull-down time is increase. So, pull-down time increases by a factor of n with respect to inverter. Similarly, if we consider NOR we find that the p MOS transistor are in series, whereas n MOS transistor in parallel. So, in this case the pull-down time will not be affected, but pull-up time will increase by factor of n. So, it will be proportional to n, the pull-up time. Therefore, we may say that in both the cases, the delay is increasing linearly with the fan-in.

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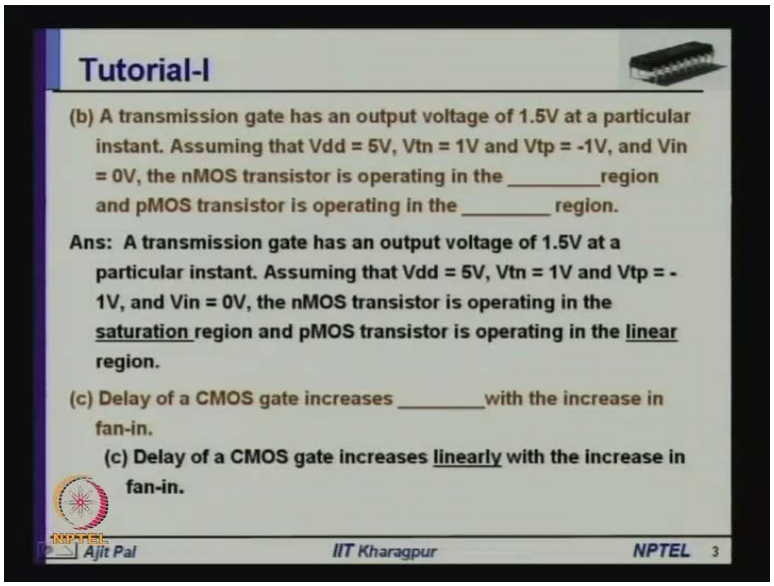


So, the answer is, the delay of a CMOS gate increases linearly with increase in fan-in. But the increase in delay that occurs in to two different ways, in two types of gates. In case of NAND gate it is, because of the delay of the series n MOS transistors. In case of nor gate it is, because of the delay of series p MOS transistors, that you have to keep in your mind.

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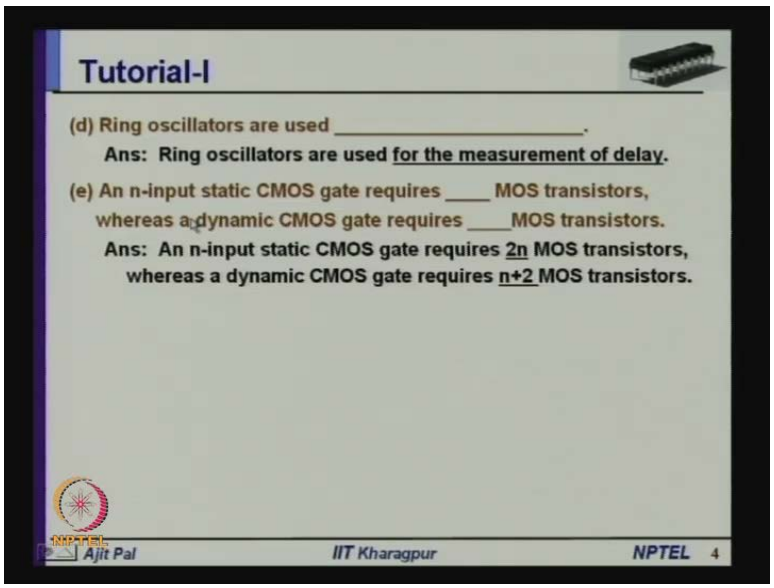


Coming to the 4th question ring oscillator; ring oscillators are used for what purpose that is written here. So, ring oscillators are used for the measurement of delay that is one of

the primary application. However, although this is one of the most important applications, where a particular device is fabricated based on new technology. Ring oscillator can be used as a clock, but you know that clock is not the primary application, because you know the clock frequency cannot be precisely controlled. Normally, we use r c oscillator or sometimes we use crystal oscillator, where you want to vary stable fixed frequency. So, therefore, primary use is not as clock generator, although it can be used as clock generator, but it is routinely used for characterization of a device of new technology. In other words it is being used for the measurement of delay. So, an n input static CMOS get requires how many MOS transistors, and whereas a dynamic CMOS gate requires how many transistors, so this is the question. So, as you know, an n input statics CMOS gate requires 2 n MOS transistors, if n is the number of inputs. For example, here this is a three input NAND gate. So, you require 6 transistors.

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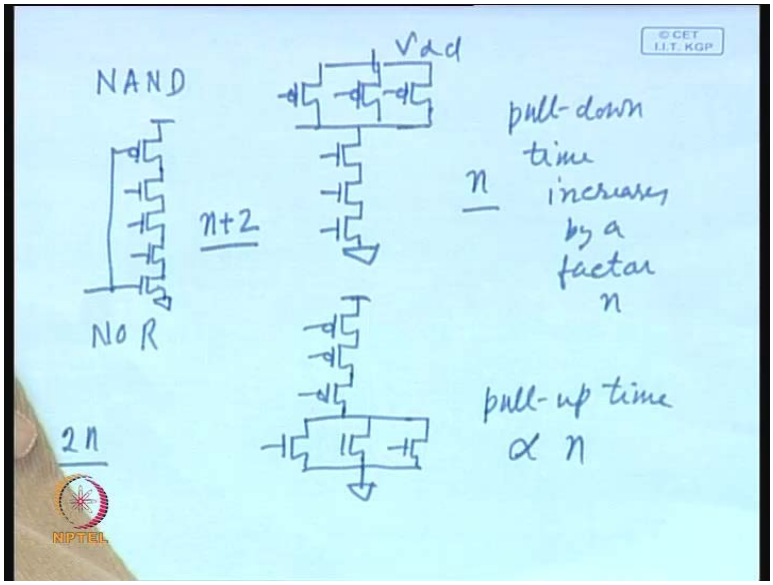


So, this is a three pull NOR gate requires 6 transistors; that means, 2 n is the number of transistors that we require. On the other hand, whenever we go for dynamic CMOS as we know, we can use either the p MOS network or n MOS network, whatever we use, say in this case we have used n MOS network, in that case we require these n transistor plus 2. So, in this case we require n plus 2 transistors. So, that is the answer, and n input statics CMOS gate require 2 n MOS transistor, whereas a dynamic CMOS get requires n plus 2 MOS transistor.

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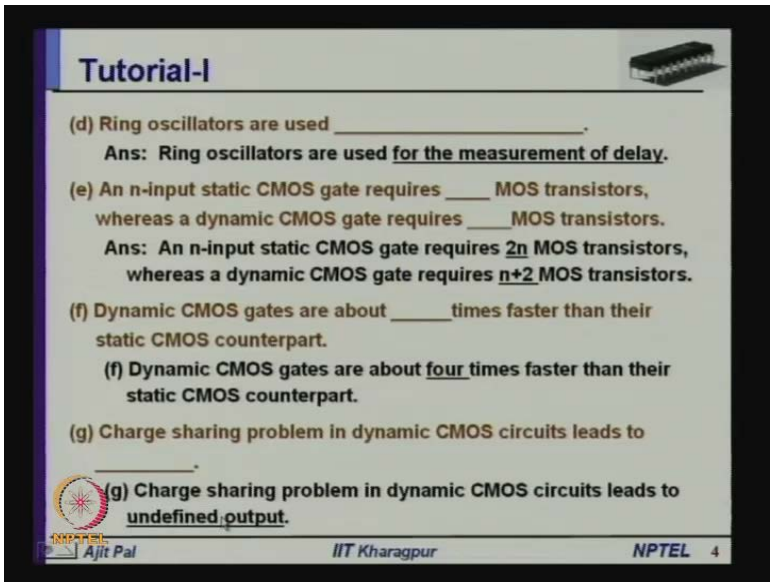


Next question is dynamics CMOS gate, gates are about how many time faster than there static CMOS counterpart. We have explain that, the increase in speed occurs, because of two reasons; number one is, the number of transistor is almost reduce to half. Secondly, the capacitance that it will be driving, output will be driving also reduces by a factor of 2. So, half reduction, due to reduction in the number of transistors, another half reduction because of the lesser capacitance. So, we may say that about fourth times increase in speed is possible, about fourth times. So, answer is dynamics CMOS gets are about four times faster than their statics CMOS counterpart. Next question is, charge sharing problem in dynamic CMOS circuits leads to some problem, what is the problem. Charge sharing problem in dynamic CMOS circuits leads to undefined output.

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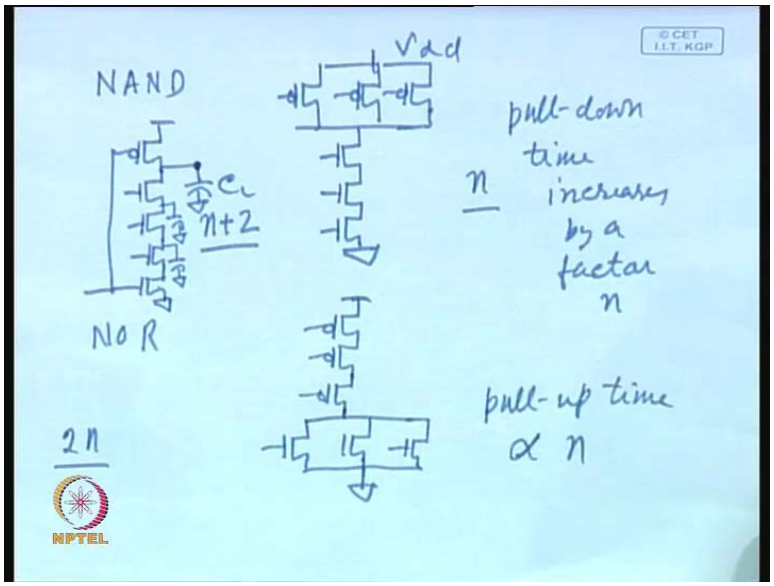


So, we know that, whenever in dynamic CMOS. Say for example, here this one we have a capacitor, load capacitance, and here are here two more capacitance are present. It may so happened that, because of charge sharing after redistribution of the charge, which is stored during recharge period here, will be distributed in this three capacitors, that will lead to reduction in the voltage, as a consequence that voltage cannot be precisely defined. You cannot tell it high, you may not tell it 0. It all depends in the relative value of various capacitances, and the way the charge sharing occurs. This is one of the most important outcome of charge sharing, and of course later we shall see, that charge sharing also leads to, kind of a additional path distribution. For example you have charge it to 1, and subsequently next output is also 1. So, in between, during evaluation it will discharge and again you have to charge. So, that will lead to, kind of additional power distribution, but primary outcome is undefined output.

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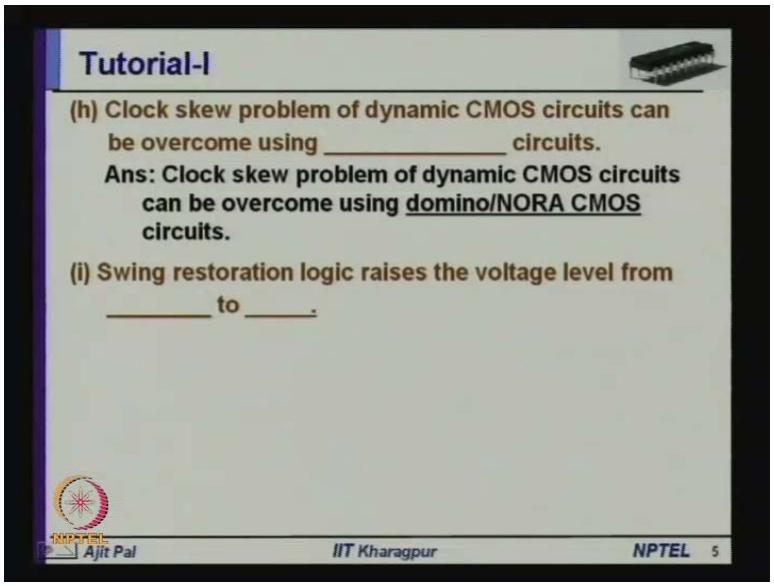


Next question is clock skew problem of dynamic CMOS circuits can be overcome using dash circuits. As you know clock skew occurs, because of distribution of the clock, in the circuit, and you know the next stage, may receive the clock earlier than the presiding stage, it may so happen, because of the clock distribution circuit. And that leads to clock skew problem, and you know you may get incorrect output. And we have already discuss this problem can be overcome, by use of two types of circuits; one is known as domino CMOS or NORA CMOS. So, by using either of the two types of circuits, you can overcome the problem of clock skew. Then comes the swing restoration a problem. Swing restoration logic resist the voltage level from this to this. So, swing restoration logic is used in pass resistor logic circuits.

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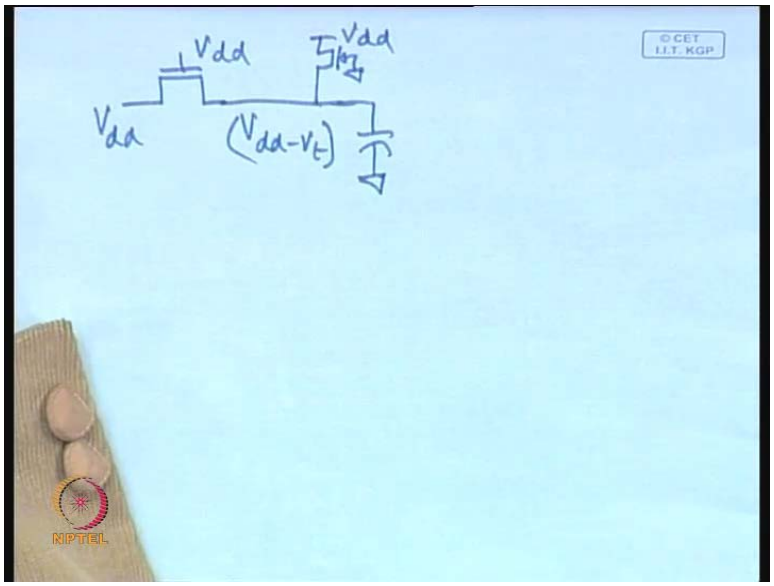


As we know, whenever you want to pass a 1 through a pass transistor, say V d d is input, here you apply V d d and you will get here V d d minus V t, and here you normally put a swing restoration logic, normally a weak p MOS transistor is connected to a V d d and gate is connected to ground. And what is the swing restoration logic does, it resist the voltage from V d d minus V t 2 V d d. So, the charging of this capacitor, which is essentially the gate capacitor from next stage, will be raised from V d d minus V t n to V d d.

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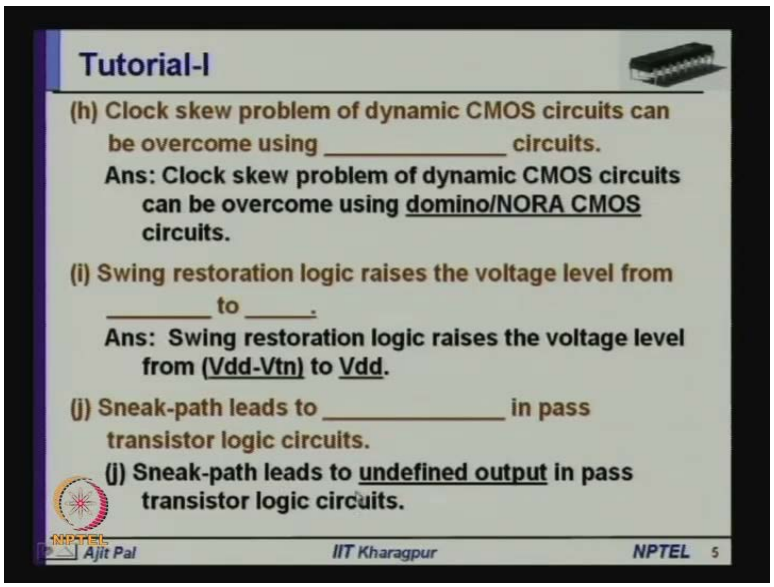

So, that is the job of the swing restoration logic, it raises the voltage level from V d d minus V t n 2 V d d. Next question is, sneak path leads to some problem in pass transistor logic circuits, what kind of problem it can lead. Again, in this case it leads to undefined output.

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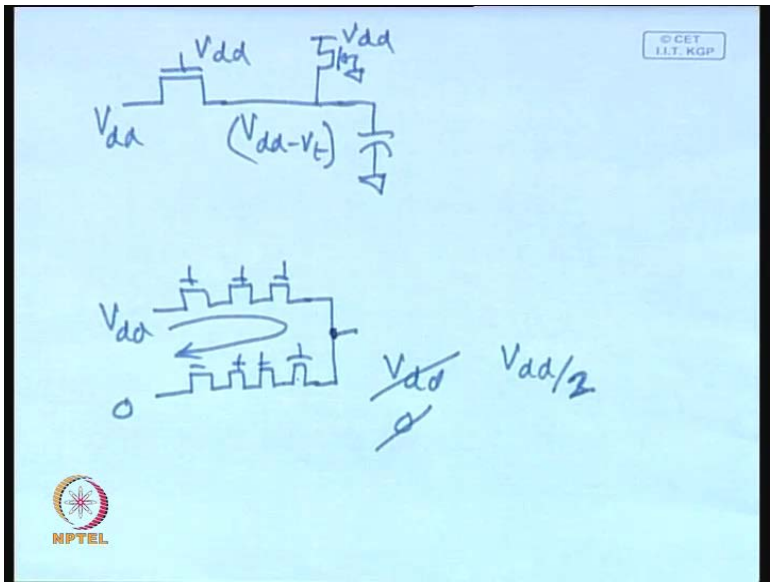


As you have seen, suppose you have a number of pass transistors, and this is connected to V d d and these are all on, and you have another set of pass transistors, through this is connected to ground. And. So, as sneak path has been created here, and the voltage here, actually will be dependent on the relative value of the own resistance, of this n MOS transistors and the other resistance of the transistor, as a result you will neither get V d d nor get 0. So, something in-between, it may be V d d by 3, 2 or something. It depends in the, resistance is equal you will get in V d d by 2 or something else, that will depend on number of transistor in series in this part and this part. So, it again leads to undefined output in pass logic circuits.

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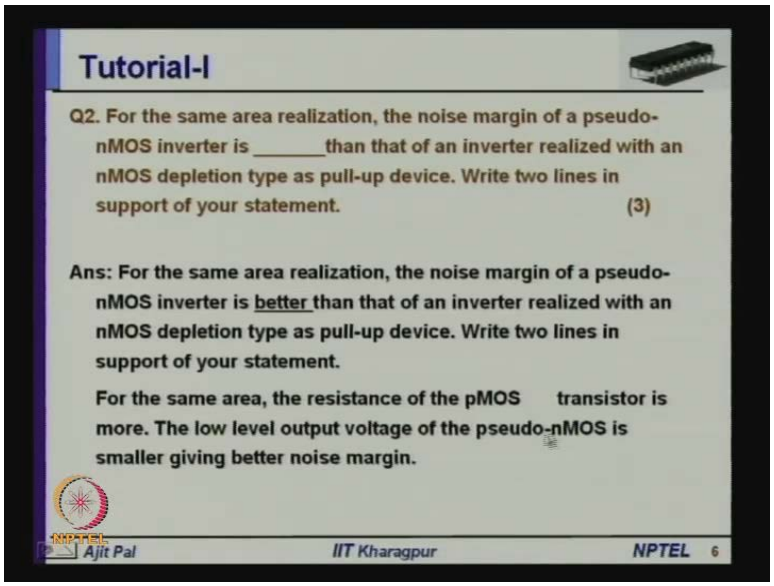


Then coming to question two, it was for the same area realization, the noise margin of pseudo-n MOS inverter is dash. Then that of inverter realized with an n MOS depletion type as pull-up device. Write two lines in supportive of the statement, first you have to complete your sentence. For the same area realization the noise margin of pseudo-n MOS inverter is better, than that of an inverter realized with an n MOS depletion type as pull-up device, and in support of the statement have to write for the same area the resistance of p MOS transistor is more, as you know p MOS transistor, because of lesson mobility of holes, with respect to electrons, for the same area a p MOS transistors will be offer more resistance, as a consequence the low level output voltage of pseudo-n MOS is smaller giving better noise margin.

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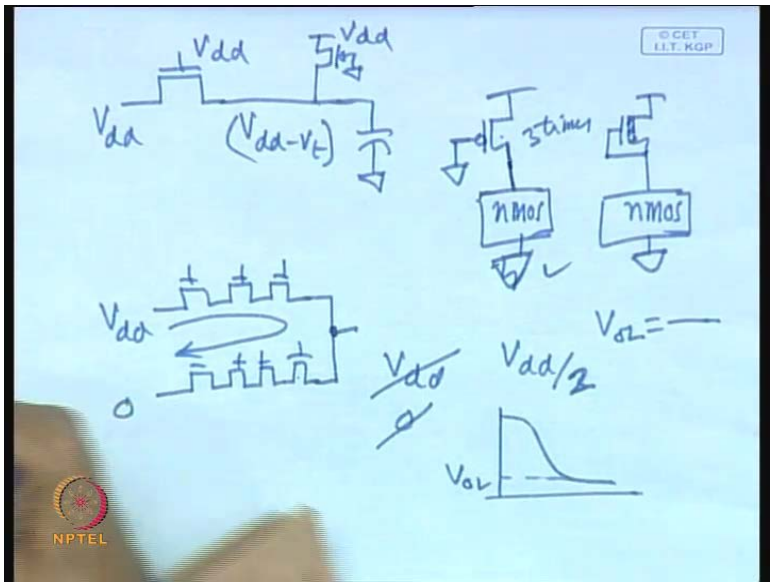


That means say you are comparing a pseudo n MOS circuit, here you got n MOS network, sorry this is connected to ground, this is connected to V d d, or another alternative is it is depletion about transistor. So, this is connected to this, and here is your n MOS network and this is connected to ground. Now, as you know the resistance of this, I mean has to be four times of the n MOS network part, so that you got a low proper low level. If they have same area, then the resistance of this will be about three times. And as you know V O L is equal to the resistance of the n MOS network, by the resistance of this plus this. Since this is more the denominator part will be higher, than the numerator, and as a consequence the V O L that is the low level voltage. As you know in this case, you do not get zero voltage at the lower level. So, V O L will be lower in this particular circuit than this one, and as consequence the noise margin of pseudo-n MOS circuit will be better than that of using the depletion type n MOS transistor as pull-up device.

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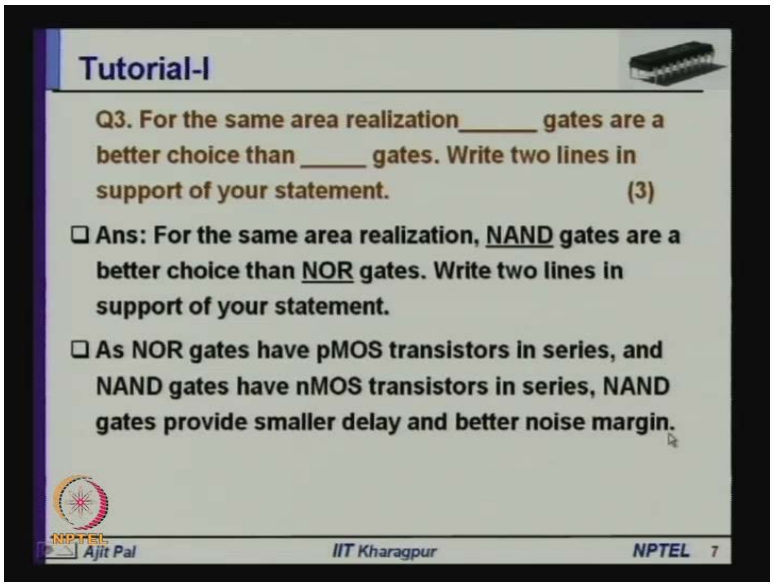


Coming to the next question, for the same area realization gates are better choice, than I mean type of gates are better choice than gates, I mean NAND or NOR. Write two lines in supportive of your question. So, which gates are better choices than other type of gates. The answer is for the same area realization NAND gates are a better choice then NOR gates, and the statement in that you have to write in support of this as NOR gate have p MOS transistor in series, and NAND gets have n MOS transistor in series. NAND gates provide a smaller delay and better noise margin as I have already explained.

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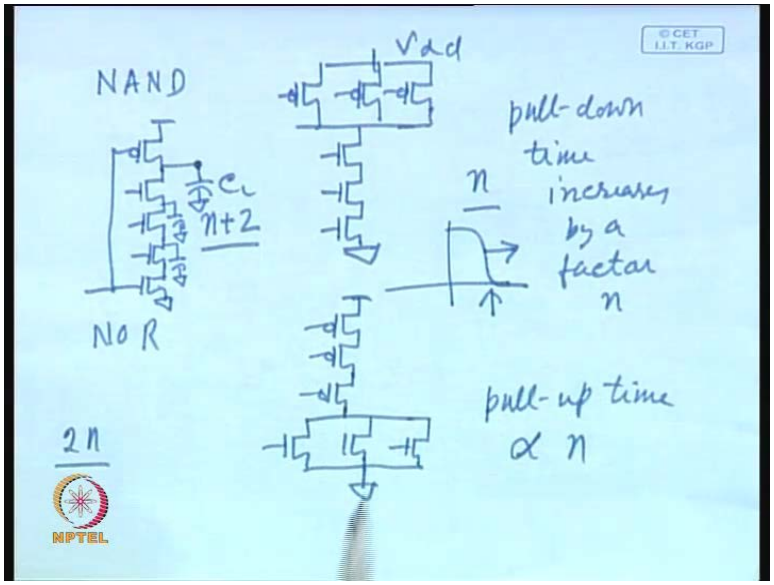

While explaining this, you know this delay of this will be more than that of this, that is number 1, and as you know the noise margin is also better here, because as the fan-in increases for the same area, initially the threshold switching, threshold voltage is lesser than V d d by 2 and NAND it moves towards V d d by 2, then becomes more than V d d by 2, as a consequence the NAND gates gives you better noise margin, and also smaller delay, and as you consequence a NAND gates are better choice than the NOR gates.

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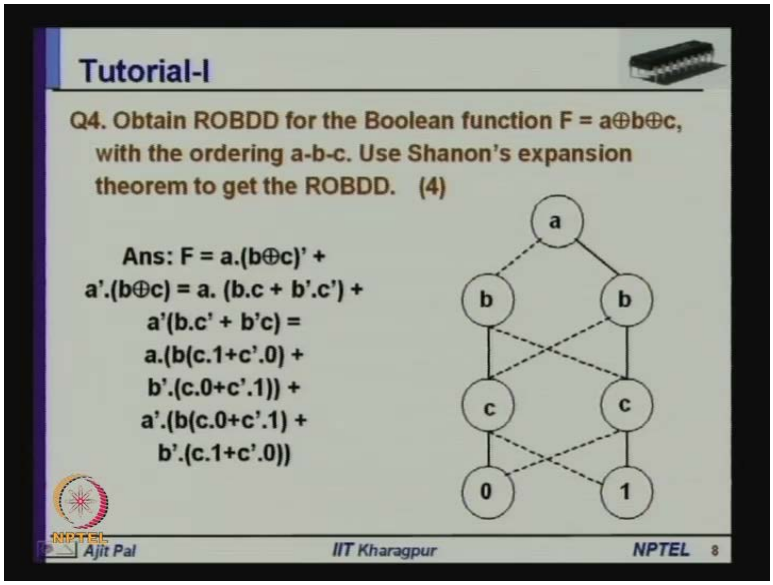


Coming to the last question, obtained ROBDD for the Boolean function F with the ordering a b c. Problem is, F is equal to a exclusive or b exclusive or c. Use shanon's expansion theorem to get the ROBDD. Here is the Shanon's expansion, and b expand it again.

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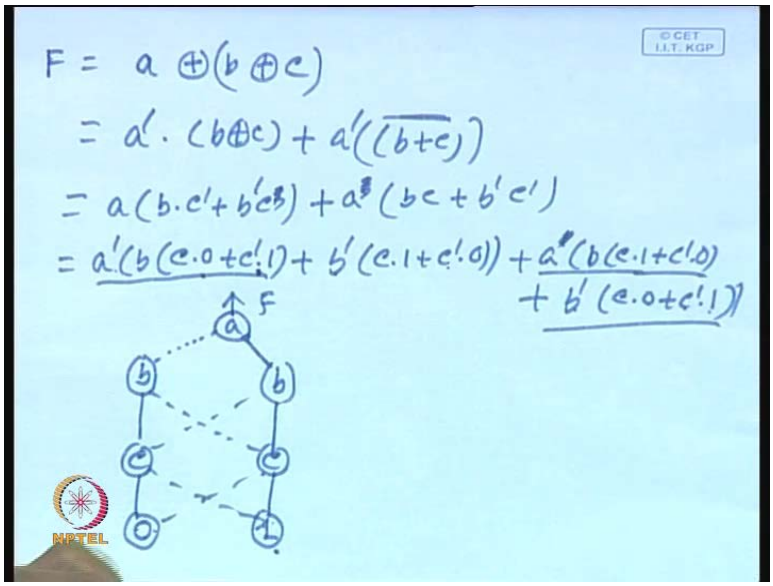


So, your F is a exclusive of b, exclusive of c. So, first you have to explain around a, then you will explained around b and c. As u know we can write it as a and b exclusive or c, plus a bar, b plus c bar, you can expand it this way. So, we see that by expanding this we get this one. So, this can be written as this. Then we expand around b, so it becomes b, b exclusive of c is b dot c dash plus b c dot, b dot c, plus a dash. So, this is essentially b c plus b bar c bar. So, expansion around b has been done. Now you can again expand around c, this will give you a b, c dash is nothing, but c into 0 plus c dot into 1, plus b dash. This is c, so c in to 1 plus c dot into 0. Then this one again you can expand, a dot, b c is nothing, but b c into 1 plus c dot into 0, plus b dot c dot if you expand it will be c into 0, plus c dot into 1.

Now, you have fully expanded, in the order a b and c, now from this you can really a draw your V d d. So, first you have to start with a, and you will have to leave nods b and b. So, this corresponds to a, and this corresponds to a bar, so this is your output f. Now, as you can see, a b goes to c, and that goes to 0, and c bar goes to a b, c goes to 0 and c bar goes to 1. So, we can write, we will have 2 more arms; c and c, 0 and 1. These are the dotted lines and this is another dotted line. So, you can see, if we follow this a b c dot, c dot 0 and a b c bar, dot 1 a b c bar a b, a b this is a, that is a bar, this is a, this is a bar, a bar actually it should be a bar, and this will be a, so I have written wrongly this should be a bar and this should be a. So, that was wrong a bar this and a this, so that was wrong thing. So, a you can see a b c into 1, a b c 1, so this is 1 path. Then a b c bar 0 a b c bar

going to 0, this path this is complete. Then a b bar, a b bar c, c goes to 0 and a b bar c that 1, a b bar c bar goes to 1. So, that is complete these two paths and.

Similarly, a bar b, a bar b then c goes to 0 this is complete. Then a bar b c bar, a bar b, c bar goes to 1, and a bar a bar goes to 1 that is complete. Similarly, a a bar b bar, this is a bar, this is b bar c, c goes to 1 and a bar b bar c bar goes to 0. So, that completes the V d d. So, this is the this is how you can generate the V d d for reading even function, I have expended by using I have shown it, how it can be done by expanding the function using Shanon's expansion. However, you can also do it by another approach, where you can start with the truth table, then you can reduce remove with full tray. You can V d d you can start the decently. Then you can remove the redounded nodes and edges you will get same result.

So, with this we have completed our discussion on the questions that you have given in my tutorial, I mean the class test one, now if u have any questions please pass on to me. So, I have the same several questions, let me discuss one after the other; first question is let me read out, superb offers what is its use number one question. Number 2 is how the characteristics will vary for transmission gate, when it is driving a large capacitive load, as it is as it drive say small capacitive load. Let me start with first question super offer. Super offer as you know, main function is to drive large capacitive load. Now, whenever driving by using say standard gates, like NAND nor. For example, let me use this diagram again, say whenever you are using say NAND gate or nor gate. We find that it is asymmetric in nature, why it is asymmetric, because this pull-out time is longer than pull-time, here pull-up is longer than pull-down time. So, this asymmetric is removed by in superb offers, how it has been removed that I have discussed in detail, that is number one, because the diving capacity is increased.

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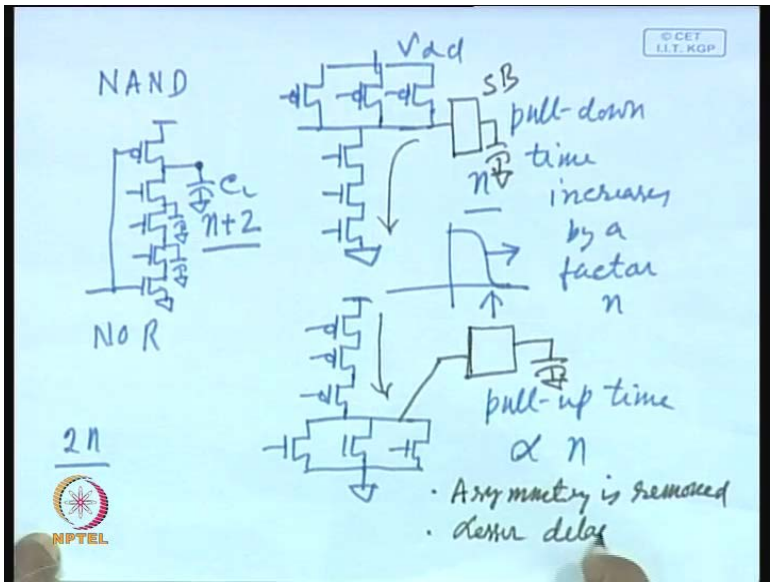


So, instead of using, I mean at the output of this you will put a superb offer that will drive a large capacitive load, so here is your superb offer. So, here you will put a superb offer, and that will driving large capacitive load. This is number one; that means, the asymmetry is removed, second is lesser delay, why lesser delay, because the delay in this case is more, because it is through a series of transistors, here also through a series of transistors, but in case of superb offer we have seen, only one transistor is there pull-up and pull-down, so delay will be less. So, because of these two reasons, the delay of the superb offer, I mean you can drive large capacitive load and delay will be small, that is the basic idea. In fact the use of by CMOS inverter is also from this same reason, that delay, it has hard driving capability, so delay will be less. That answers the first question. Second is how the characteristics will vary for transmission gate, where driving a large capacitance load, if it drives a small capacity load.

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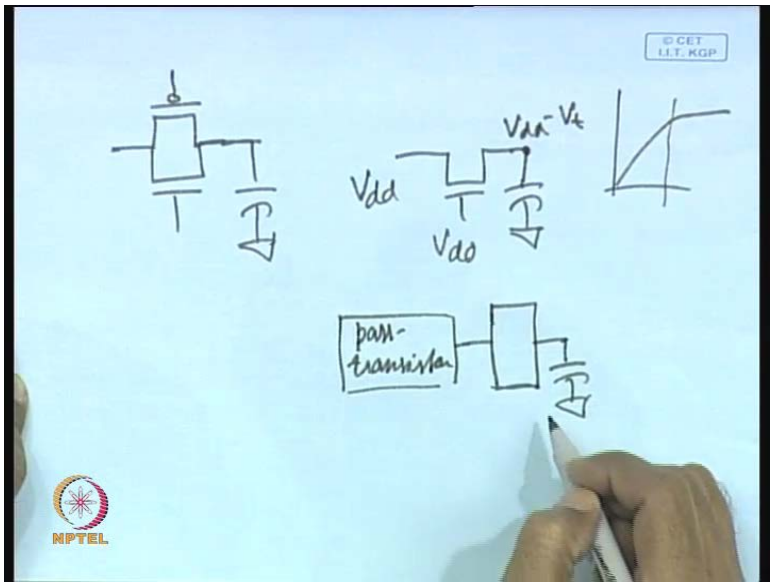


See we have already discussed the problem of driving a capacitive load, with the help of a transmission gate, say transmission gate, driving a large capacitive load and small capacitive load, what will be the problem. So, problem will be somewhat similar, whenever you drive with a pass resistor logic circuit. So, whenever you drive it; obviously, here it is more advantageous, because you have two paths, and but here it will be only through one path. So, that charging will be slower that is number one, because the charging current as the. For example if this is V d d and this is V d d, and as the charge builds up the current will keep on decreasing, because the drained voltage is reduced, as you know, as long as it is in the saturation region current drive is ok, but as it comes to the linear region, the current will gradually reduce through this, and a consequent charge will be slow and it will turn off when you know the voltage difference is here it is V d d minus V t.

So, this kind of problem will arise, whenever you are driving pass transistors, that is the reason, why always you will find, we uses instead of driving through pass resistor. We put a buffer or swing restoration logic and the output. A buffer is provided; this is the pass resistor logic. And at the output of pass resistor logic, we put some buffer and that drives the capacitive loads. We have seen the pass resistor logic family d p l, s r p l and various logic families, or the clip family, always you have seen some buffers are at the output are provided to output to drive the capacity loads. So, that problem is overcome by using capacity load.

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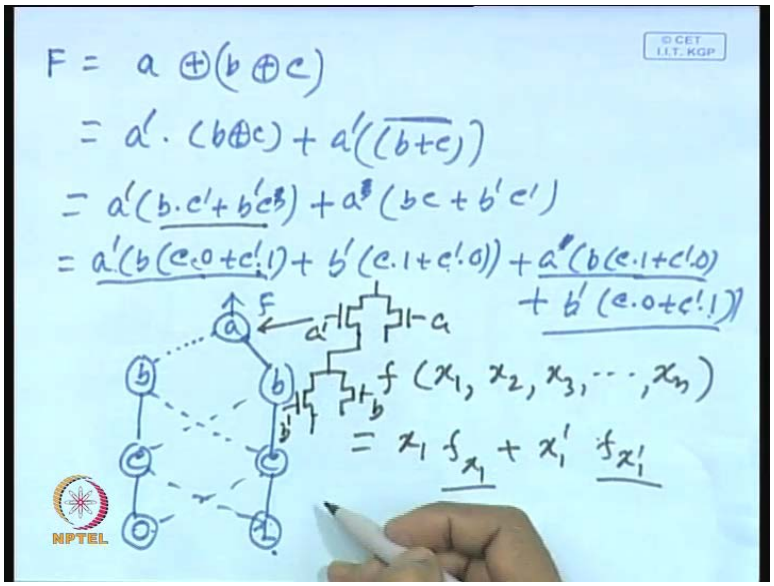


So, shanon's expansion theorem, I have already explained with the help of this example, what shanon experiment does, say there is function f f 1, f which is which is a function of say n variables x 2 x 3 x n. Now, you can write it in the form of this x 1 f x 1 plus x 1 bar f x 1 dash bar. So, what you are doing, you are expanding around the variable x 1. So, in this case f x 1 which is known as reduced function, is a function of the remaining variables. For example, here I have expanded around a. So, here you find that these are functions of the remaining variables; this is your b and c. Similarly, this is also function of the remaining variables. So, this and this will be a function of the remaining variables, and again you can further expand it as you can see. So, this was around a, this was around b and then you have expanded around c. So, you can see this is again a function of the, since only three variables are there; obviously, it will be constant, so that is what you have got.

That means, if you keep on expanding you will get ultimately constants, like zeros and ons, and this is what is Shanon's expansion. So, this shanon's expansion help us to generate the reduced function, and also it can be used to you know get the pass resistor logic network. For example, once you have got this you can map it to a pass resistance network, because you know this will act like a 2 2 1 multiplexer this will act like a 2 2 1 multiplex of this, it will be a like a 2 2 1 multiplexer of; that means, each will be represented by a 2 2 1 multiplexer; that means, this a will be applied here and a bar will be applied here and this is output. Similarly b you will put another pass transistor

network, and this will correspond to a b and this will correspond to b bar. So, this way you can form a pass resistor tree, from this say from this ROBDD and you can realize the circuit. So, this is how Shenon's experiment is done. Now, the question is, so this is a NAND gate, in case of a NAND gate.

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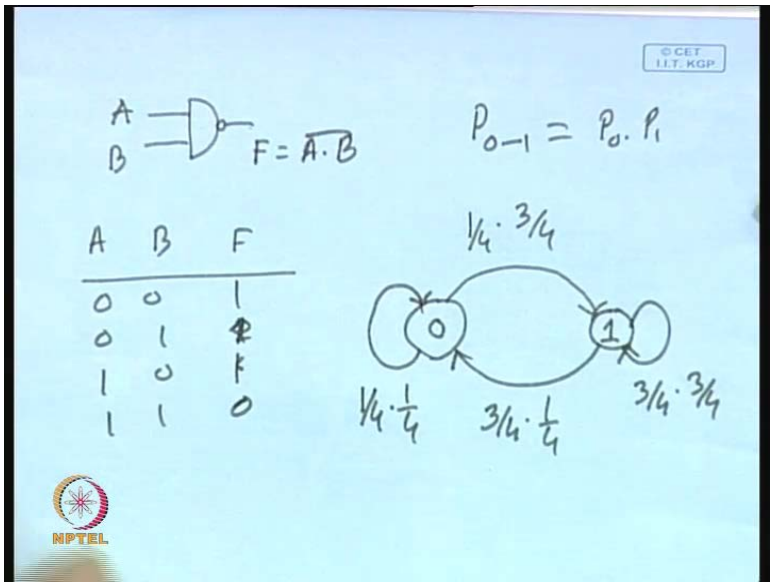


Suppose, you have 2 input NAND gate; so A and B and it is realizing a function, f is equal to A dot B bar, and as you know the truth table is A B F 0 0 1 0 1 0 1 0 1 1 1 0 so; that means, if anyone of input is 0 output is 1, when both of them are 1 or output is 0. Now, you can find out the probability of transition from one input to another input. So, output can be. There are two possible outputs 1 is 0, another is 1. You will say that this is the output state of this gate. Now, you can essentially draw a straight transition diagram and the edges will show the probability of transitions. So, what is the probability of transition from 0 to 1. From 0 to 1 you see here you have got only 1 0, and here you have got only one, one I mean 3 1's. So, the probability of transition from here to here is 1 by 4 into 3 by 4; that means, as we know p 0 to 1 is equal to p 0 into p 1. So, this is the probability, probability of 1 and the probability of 0, of remaining is 0.

Now, what about this probability 0 to 0, so, here you know it has it has got only 1 0, and again probability of going to 0 is 1 by 4. So, out of 4 possibilities, so, this is the probability that it will go from 0 to 0 output will go from 0 to 0. Similarly, from 1 to 1 (()) the probability will be 3 by 4 and into 3 by 4. Similarly, from 1 to 0 the probability

will be 3 by 4 into 1 by 4. So, I believe this is what is the question. Now, the another question is n MOS depletion type transistor, here V g s is equal to 0 force every time not in paper there is some V g s is equal to V out.

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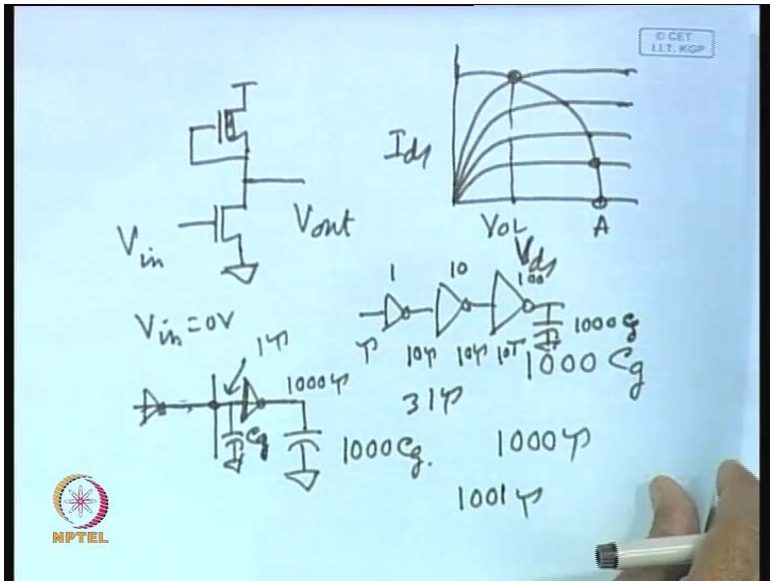


So, this is a question related to a depletion mode transistor, as pull-up device and here you have got an input, V in is applied here and you will get V out. Now, what will be the output, you see whenever this is not a pass resistor network. In this particular case, this is a n MOS depletion type, this is this is n MOS (()) type. So, if you draw the characteristics curve of this transistor, it will be like this, and so far as this transistor is concerned you have to draw the other way; that means, it will be somewhat like this. So, initially what will be the case, whenever V in is equal to 0 volt, what will be output, this transistor is off this transistor is on, so you'll get V d d at the output. So, this is I d s and this is V d s. So, initially the voltage will be here a, and as the voltage is increased, above threshold volt, as the voltage goes above threshold voltage of this transistor then it will move to this point, as the voltage increased it will move gradually, and ultimately it will reach this point, and this is the V O L, at that time both transistor are on, and you will get a output voltage, which is decided by the ratio of this two transistor.

And the question is not very clear from this writing anyway, whatever is I have understood I have explained. Here there is the question of driving large capacitive load, say 1000 C g. Now question is, this is a point coming out from a pin; say this is a pin,

from here the output is coming out, and you have connected a capacitance C g, I mean 1000 C g. Now, what will be the delay in driving this. So, if you normally we put a inverter here. Inverter; if this inverter is of unit ratio I mean single, I mean there is no increase in size, width is minimum, length and width is minimum, 2 lambda by 2 lambda, then what will be the delay. Then, as we know the delay will be 1000 tau, 1000 tau. However, you are driving this from internally. So, may say that there is some delay in driving this capacitance also, so here it will be 1000 tau. And, in driving this capacitance assuming that this is also being driven by unit gate, I mean gate delay.

So, here may be an inverter is there, driving this also will involve a delay of 1 tau, so the total delay is 1001 tau. So, this delay driving this capacitor, and delay in driving this capacitor. So, here also you have got a capacitor, which is equal to C g. So, to drive this capacitor there will be delay of tau, and to drive this capacitor there will be delay of 1000 tau. Now, if you put several stages; like say first you have put one, this one, then you have put 10 times, then you have put 1000 times, then 100 times. So, this is 1, 10, stage ratio 10 and here is 10 ratio 100. Now, you are driving this capacitance which is 1000 C g. So, what will be the total delay; in driving this capacitance there will be tau, in driving this capacitance there will be 10 tau, in driving this capacitance there will be delay of 10 tau, in driven this capacitor there will be a delay of 10 tau. So, what is the total delay, 10 plus 10 plus 10 plus 1. So, it will be 31 tau. So, this will be the delay in driving this, through these three invertors. I believe this is the question, that has been given. Is there any other question.

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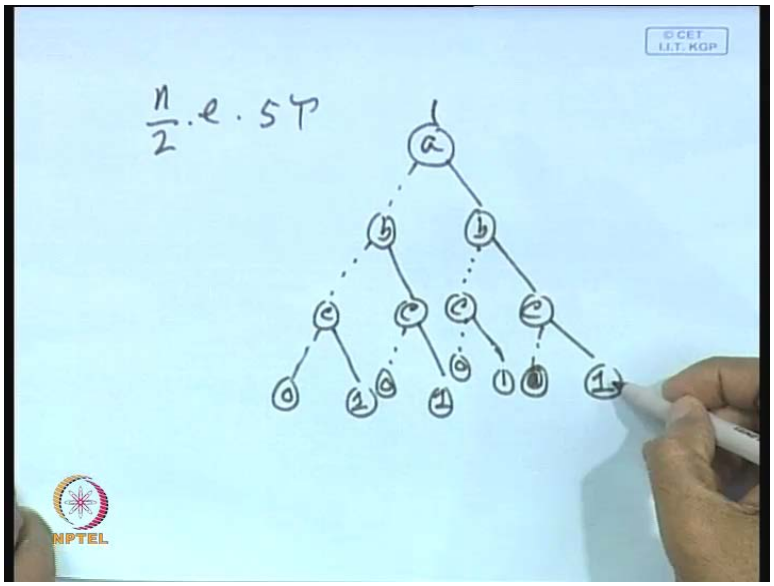


I think there is a question like this, I mean here it is written, how you are getting n by 2 e into 5 tau. Any way the question is not very clear, what has been written. So, I cannot really answer unless the question is properly known, any other doubt. You can pass on in writing. So here, there is the question about how you can simplify. Let me draw the V d d that has been given, say a b this goes to b, from here it comes to c and goes to c, c it goes to c, then here 0 1 0 1 0 1 0 here it is 1, how to simplify this. As I mentioned first step will be to merge the zeros and ones at the leaf line; that means, you have to follow a kind of bottom of approach, I mean from the leaf nodes you have to go towards your the root node.

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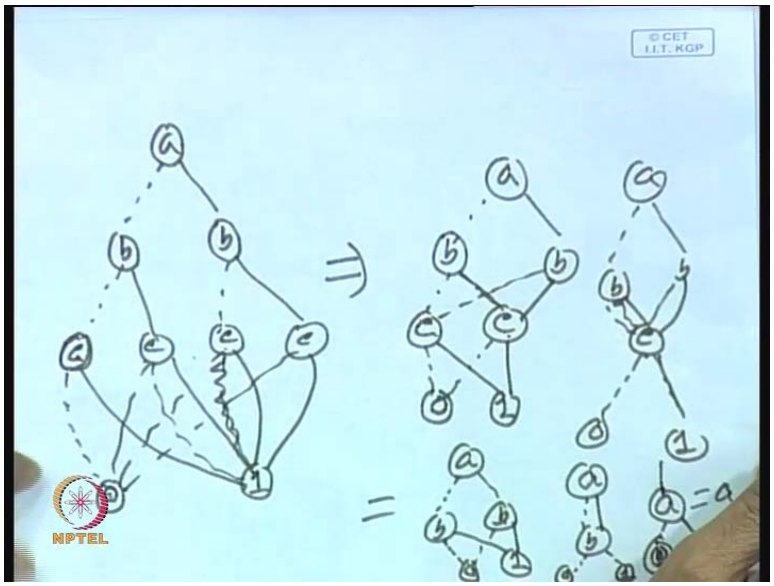


So, how will you proceed, so first step will be a b b c c c c. So, all the 0's are to be combined. So, let me write 0 here let me write 1 here. So, 0 is coming from here, 0 is also coming from here, 0 is coming from here, 0 is coming from there, and 1 is coming from here, 1 is coming from here and from this one is going to again 1, and from this it is going to 1, so this is the first step. After this first step we find that; that means, this particular 0, this is this is going to 0, this is going to 1, this is going to 0, this is going to 1, this is going to 0, this is going to 0. So, here also the last this is going to 0, and this is going to 1. So, we find that all this c are same; that means, this c, this c, this c, this c, all the c that has been given; that means, the 0 is going to 0 1 is going to 1 for all this cases.

So, this will become a b b and all this c's will merge. I mean not all there will be 2 c's, one is your dot, another is your from here it will come, here also dot, this will go here, from here also it will go here. So, this will go to both the cases 0 and 1, so 1 1 0. So, here we again find that these b's. So, this is 0 this is 1 and, so what will happened in this particular case, b this one, and this one, and this one, and this one, this c. So, this c again will merge, because you can see this are identical, so it will be same. So; that means, I have omitted one step, this will be b b. So, all of them, since these are this will merge it will become 1 c, because this and dot all are going to c, and this is going to 0 and this is going to 1. So, this will disappear, and once this disappears b will also disappear.

So, in this particular function, it will become a b b and c will be no longer will be there, because directly the c will emerge and it will come here, 0 and so that means, the solid lines will go to 1, doted lines will go to 0 this like this. Again, we find that in this case also b will merge, a b will emerge and it will become single b, dotted line going to 0, solid line going to 1. Again, it is independent of b, so it will be a, dotted line will go to 0, solid line will go to 1 and it will become a. So, we find that from this after minimization, and it is essentially equal to a. So, it is independent of b and c. So, a is 1, and when a is equal to 1 it is going to 1, and a power is equal to 1 it is going to 0, so it will realize a function a. So, this is a very redundant function. So, you find that all the edges and nodes are getting removed, because of this minimization. So, with this let us come to the end of today tutorial. Thank you