Low Power VLSI Circuits and Systems

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Module No. #01

Lecture No. #18

Switching Power Dissipation

Hello and welcome to today's lectures on switching power dissipation. We have discussed various types of MOS circuits in a bottom of approach, using a bottom of approach. We started our discursion on MOS transistors, various characteristics of MOS transistors. Then, we discussed about the realization of different types of MOS inverters, using MOS transistors. After that we have discussed different types of combinational circuits, that you can realize using MOS transistors. We have discussed gate based logic circuits, like static CMOS, dynamic CMOS and also switch based logic circuits, like pass transistor logic. Then we have covered the MOS memory devices. And in the last lecture we have discussed about finite state machine. So, that gives you a complete background of different types of MOS circuits, that you will encounter in your VLSI circuits and systems. In other words now this day is ready to discuss about low power aspects. And today we shall start with our discursion on sources of power dissipation. First lecture will be on switching power dissipation; that means, that is one of the most important components of the sources of power dissipation.

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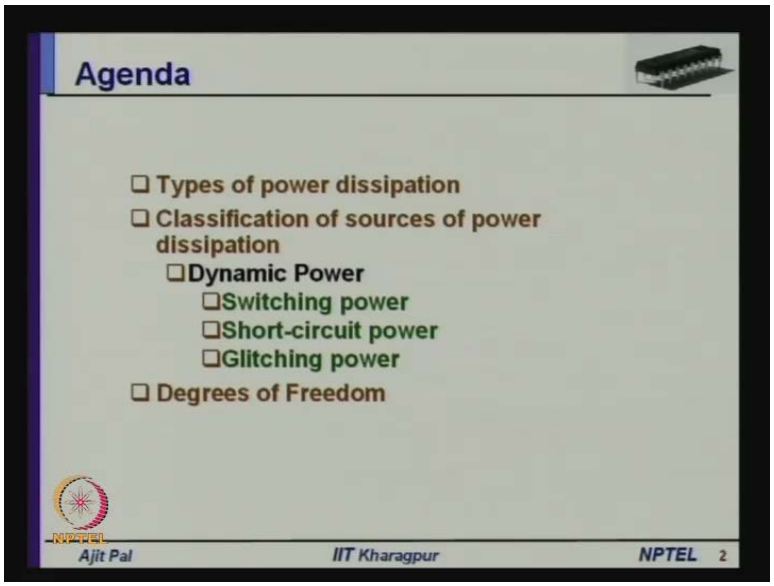

So, here is the agenda of today's lecture; first I shall give a brief introduction about types of power dissipation. Then discuss about the classification of sources of power dissipation, dynamic power. And there are three components as you know; switching power, short-circuits power, and glithcing power, and also there is another type of power dissipation that is called static power dissipation that we shall discuss later, but based on this dynamic power, what are the degree of freedom that I shall discuss, may be at the end of our discussion on different types of source.

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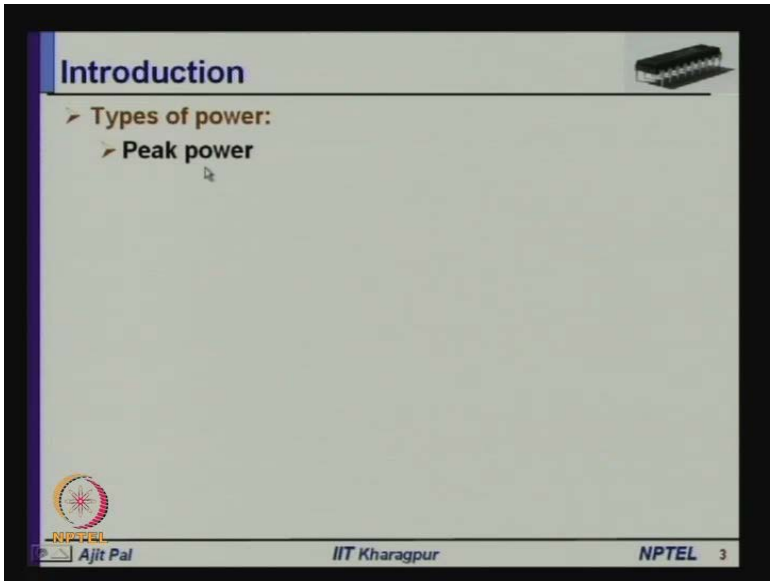

In this lecture we shall focus on switching power dissipation, but before I do that let us discuss about, what do really mean by power and what are the different types of power dissipation that you encounter in digital circuits. One of the most important source of power, important power dissipation is peak power.

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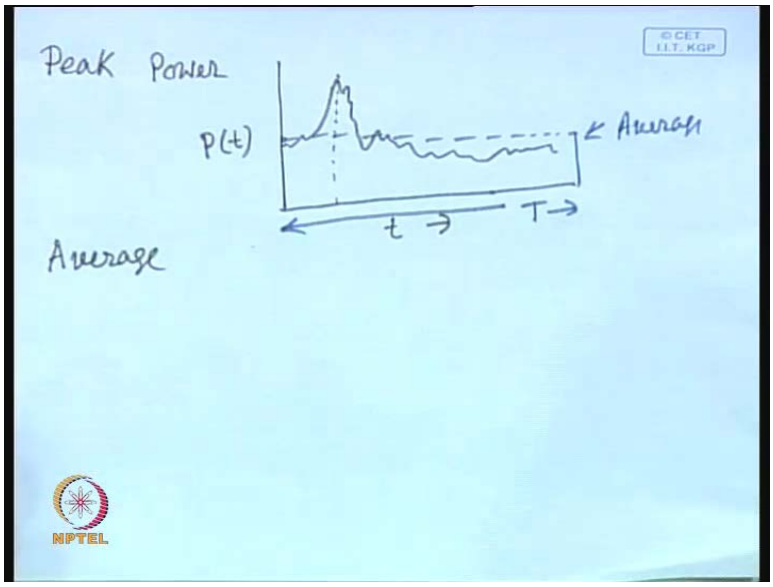

So, what is peak power. If you plot the power dissipation of a circuit, over a period of time, this is the power which is a function of time. We will find that it is not constant, so sometimes it is more sometimes it is less and so on. So, it will be somewhat like this, so it is a function of time. You may be asking why this kind of maximum power occurs. It occurs in many situation, for example when you are turning the power of a laptop, a computer, then at that point it will consume a large power. You will be asking how the peak power, which is essential in the instantaneous maximum power, that is drawn from the power source, how it affects the behavior of the circuit.

Actually wherever there is a serge in power dissipation; that means, suddenly it increases. Lot of current flows to the power lines; that means, power is drawn from the supply line and also the current passes through the ground. So, this supply and ground line, through those lines heavy current will flow suddenly. And because of that it will lead to some kind of transients on different parts of the circuits; that means, it will affect other component of the circuits; that means, it will lead to glitches, it will lead to drupes and so on. That means as a consequence of this peak power, suddenly search of power

drawn by the circuits, some bits of a computation may be erroneous; that means, some or whenever you are writing or reading from memory, you may be reading wrong data when that transient occurs. So, in other words peak power affects the circuits in terms of correct output; that means he may not get correct output. In other words reliability of the circuits is affected. So, this is this is the peak power.

Then second one is the average power, what is the meaning of the average power, for example for this particular wave form, the average power will be somewhat like this. So, may be it will be like this, this is the average power. So, this is average, over a period of time period say t, so if you average it over a P time period t then this is the power dissipation. In what way this average power is important. In fact, the average power is very important from the view point of packaging and cooling cost; that means the power dissipation over a period of time that has to be dissipated using the cooling and packaging arrangement.

So, the packaging and cooling cost is affected by the average power, not only that the average power affects the cost of the battery, because you are drawing the power source from the battery, or it may also affects the power circuits, for example regular day power supply, transformers which are used to generate the d c power. So, those will be affected, rather the weight of the system, volume of the system and the packaging and cooling cost. These will be affected by this average power dissipation. So, average power is very important, from whenever you are. Your circuit is operating from battery, because the size of the battery will be large, and it will not last for a long duration, if the average power is high. However, whenever you reduce the average power, the peak power is also reduce, that is the reason why most of the time we shall be focusing on average power, reducing the average power, and simultaneously the peak power will be reduced.

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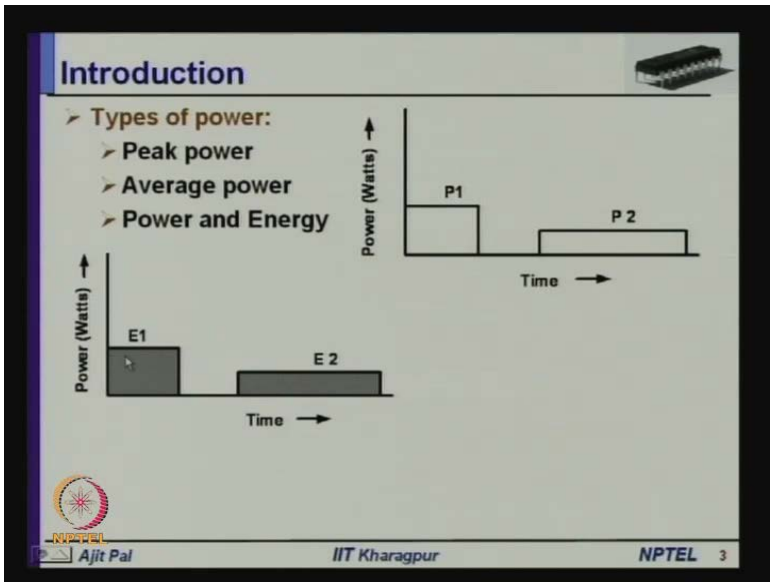

Now, here for example, the power in watts is plotted, and P 1 is the peak power for duration of time say t 1, 0 to t 1. And similarly average power dissipation P 2 is for another duration may be t 2. So that means, that peak power dissipation at this movement at this moment may be different, I mean average power dissipation at during the time t 1 or during the time t 2 may be different. Now, it is another very important concept that is energy; power and energy these two are although they are different. Sometimes we use them interchanging, in what way they are related let us try to understand. What do you really mean by energy. Energy is the actual I mean energy what is drawn over a period of time from the power source; that means, it is power into time that is your energy. For example, in this particular plot we have that power dissipation was P 1 and over a period of time t 1, so E 1 is the energy, which is represented by the area under this rectangle, area of this rectangle.

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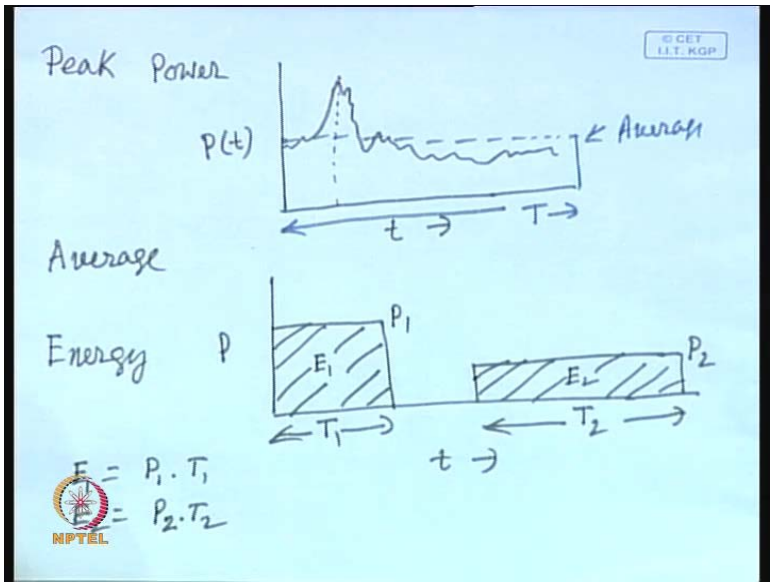

So; that means, this energy; say if this is the power dissipation P 1 average power dissipation P 1 over a period of time t 1, and say another power dissipation which I have shown, that is average power dissipation P 2 over a time period t 2. Then energy here, obviously time and here p, so energy E 1 is the area of this rectangle. Similarly the area of this rectangle is, this is your, again E 2 is area cover by this rectangle. That means energy E 1 is equal to P 1 average power dissipation into t 1. Similarly, E 2 equal to P 2 into t 2. Now, you may be asking in what way energy affects your circuits, particularly for battery operator system energy is very important, because whenever battery is fully charged, some amount of energy is transfer from the charging source. And that energy has to be used by the battery for the performing computation and other thing. So, you have to essentially minimize energy whenever you think about battery operated systems; that means, whenever we say low power, essentially we are meaning low energy, but sometimes we use this two interchangeably, although they are different.

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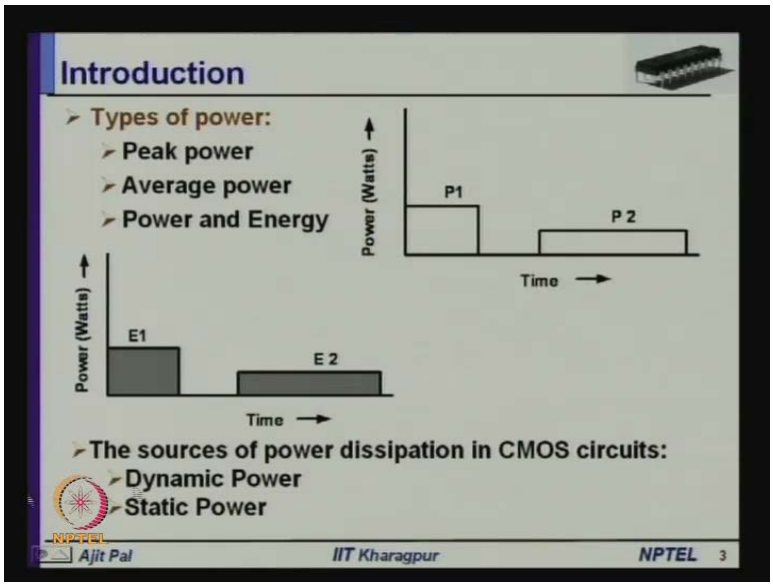

So, we have discussed about different types of power dissipation and relationship between power and energy. Now, let us focus on the sources of power dissipation in CMOS circuit. The sources of the different sources can be divided into two basic category; dynamic power and static power. So, what do you really mean by dynamic power. Dynamic power dissipation occurs, when the circuit is in operation, when the circuit is in action. You have applied a supply voltage, you have clock, you are changing the inputs, outputs are changing, that we call the circuit is in operation or in action, and that time whatever is the power dissipation we call it dynamic power. On the other hand static power dissipation is, when may be the power source is there, but inputs are not changing, clock is withdrawn, then we call it static power. And static power dissipation, as we have seen in case of CMOS circuit, it essentially leakage power dissipation.

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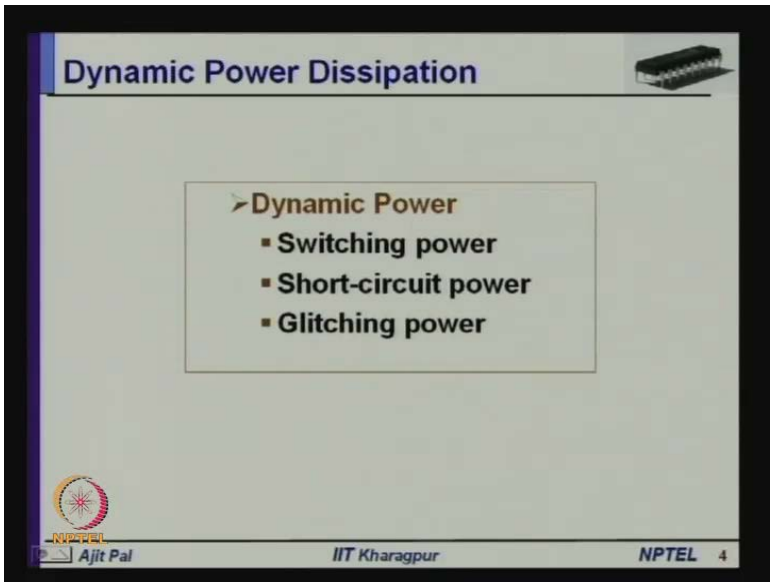

And again the dynamic power has got three components, which I mention in my first lecture, the three components are; switching power, short circuit power and glitching power. So, these three different types of power dissipation occur, when the circuit is in operation and which are categorized as the dynamic power. And switching power is the most important components which I shall discuss in this lecture.

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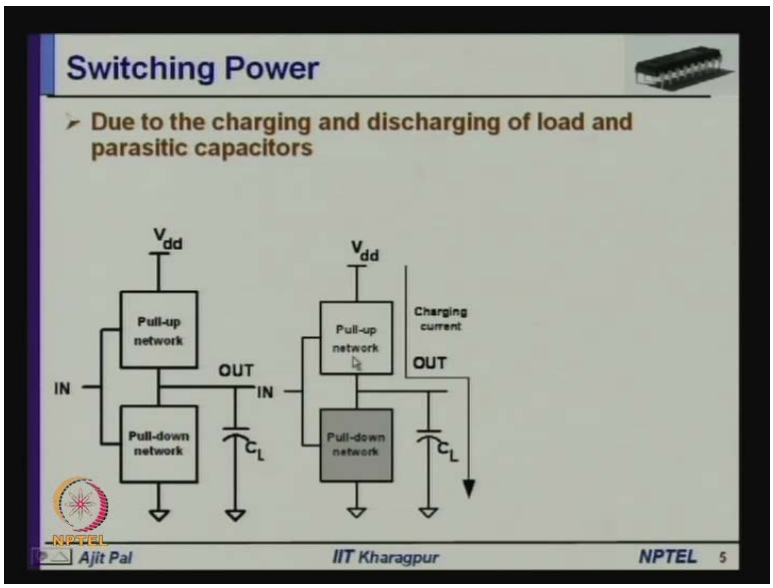

What do we really mean by switching power and why it occurs. Switching power occur due to charging and discharging of load and parasitic capacitors. As we have seen in a

CMOS circuits there are lots of capacitances; gate capacitances, NAND capacitances, interconnect capacitances and so on, various types of capacitances are present in a circuit. And those capacitances gets charge and discharge during normal circuit operations, and that leads to power dissipation, and that is known as the switching power dissipation. And let us look at a CMOS circuit, we have seen the basic, I mean the generic schematic diagram of a CMOS circuit is like this. You have a pull-up network made of n MOS, p MOS transistors, and you have a pull-down network made of n MOS transistors. And we have a load capacitances C L, that is how we model it, although C L is shown as a lump capacitors. It is essentially comprises many capacitances including gate capacitances, interconnect capacitances and various other types of capacitances. Now in this situation, how the switching power dissipations occurs. Now let us see how it is occurring, whenever the output is changing from say 0 to 1.

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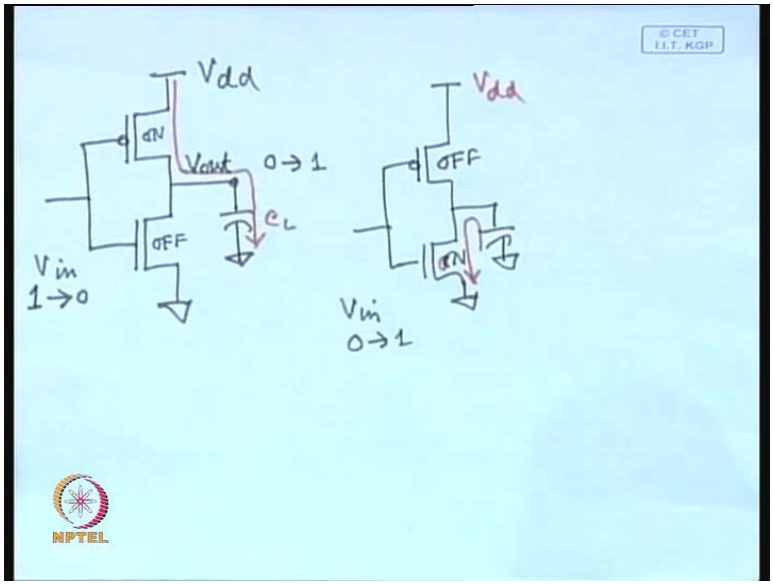

Let us consider very simple circuit; say an inverter, you have an inverter for the sake of simplicity, and this is connected to V d d and this is connected to input. Now you have a load capacitance, C L connected here. Suppose, initially the input was 1 and it has change from 1 to 0 input V in. What will happen to V out. V out will change from 0 to 1. Then what will happen; that means, initially the charge across this capacitors, charge that was stored in this capacitor was 0. Now it will charge through this transistor, because when the input voltage is 0 that time this is off and this is on. And as consequence this capacitor will charge through this p MOS transistors, through this p MOS transistors it

will charge. And while it charges some power will be decapitated in this p MOS transistor, because it is a resistive component, and out of the total energy, that is drawn from this power source, may be battery or some power supply some will be lost as form of heat, because when current passes through a resistive load, power dissipation get receipted in the form of heat.

On the other hand part of the energy will be stored in this capacitor C L, later on we shall see what is the energy that is drawn from the battery for charging a capacitors, and how much energy is stored in this capacitors. Now suppose it changes now from the same circuit, now the input changes from, V in now changes from 0 to 1. Then what will happen, this will become off and this will become on. And as a consequence as I told some energy was stored in this capacitor, that energy, that charge energy means that will stored in the form of charge, that will get dissipated through this n MOS transistor; that means, the energy that was stored in this capacitors, while after charging from V d d that will now gets dissipated through this n MOS transistor, and now the charge will become 0. That means whatever energy that was drawn from the power source, part of the energy is dissipated while charging, and part of the remaining part of the energy it gets dissipated while discharging; that means, when the output goes from 1 to 0 as it is shown in this diagram.

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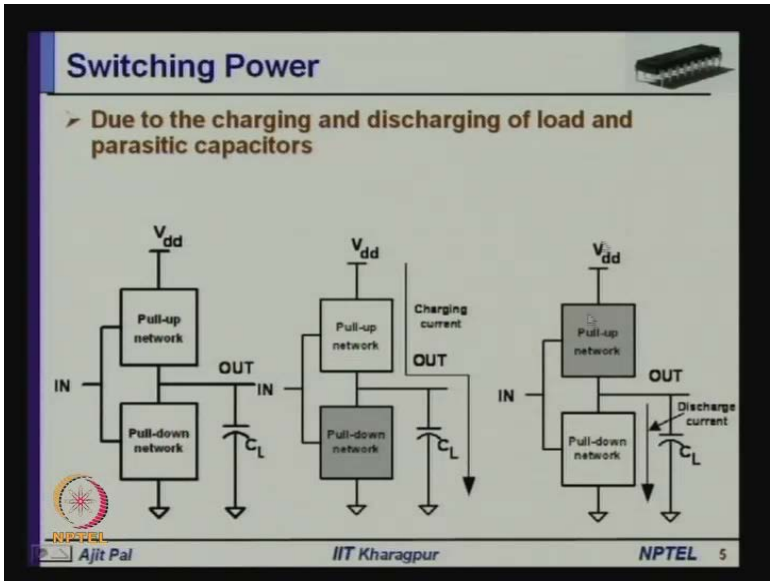

So, this is the charging current. So, for general CMOS circuits the pull up network is responsible for power dissipation while charging, and pull down network which may be a complex network, that is responsible for power dissipation while discharging. So, from the capacitor it gets discharged through the pull down network.

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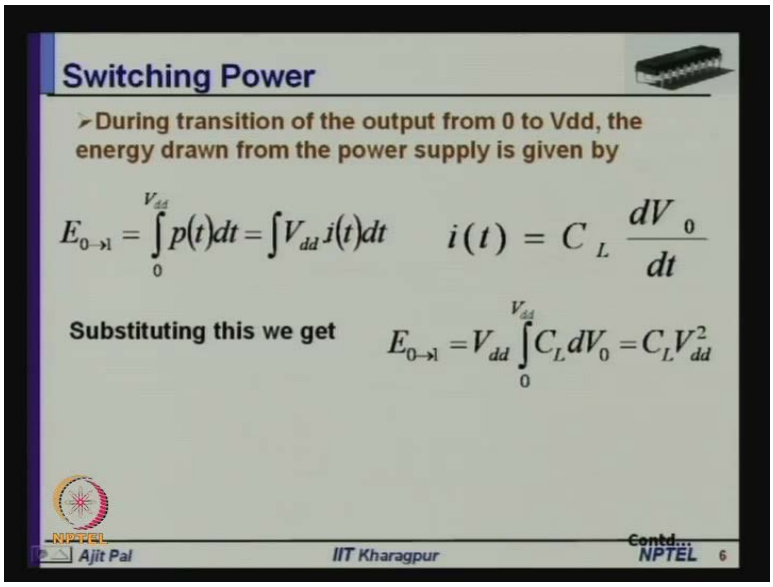

Now, we can calculate the power dissipation; let us now proceed to calculate the various power dissipation, that occurs in a circuit in this type of circuit.

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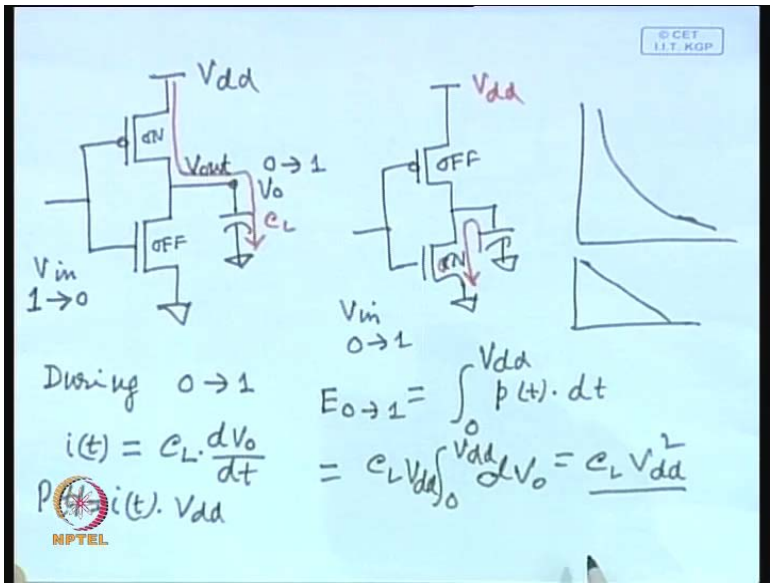

So, how much energy is drawn, so during transition from 0 to 1, how much energy is drawn from the power source. Let us find out that, so energy drawn E 0 to 1 is equal to 0 to V d d. This capacitor is charging from 0 to V d d and power dissipation, and time. The time over a period of time this is happening. And as you know current will pass through this part of the circuit, and that will lead to power dissipation. And what is the expression for current. This current is not fixed, that current will be equal to i t, and this will vary with time C L into d V 0 by d t what is d V 0, d V 0 is the output voltage.

So, rate of change in output voltage with time into capacitance value, say load capacitance is the instantaneous current that will be passing through this part of the circuit. So, if we substituted it here, then we shall get C L will come out, this will become 0 to V d d into d V 0**,** V d d. So, we shall d V 0 d t 0 to 1 V d d and it will be C L, and energy is the 0 to V d d and C L d V 0 and this will be equal to, power is voltage into current that we have missed here, so there will be V d d factor. P t is equal to i t into V d d. This is the power dissipation, so V d d will factor will be here.

So, this if evaluate, this will become C L V d d square. So, C L V d d square is the energy that will be drawn from this power source. So, we find that an energy of C L V d d square will be drawn from the power source. Now you may be asking for different types of the charging current, will this expression be same, or in other words what I am telling. Suppose, if charge is using a constant current source, from a constant current source. Will it be same whenever we do it through register as if you have done in this case. Actually as the capacitor is charge from 0 volt to V d d, this energy will be save irrespective of the way you charge it; that means, the nature of charging current can vary like this, as it happens whenever you charge through resistor or it may be linear, current will fall over period of time when it charges, so V d d. So, irrespective of that this will be the energy that will be drawn from the power source. So, that is the reason why there is no other parameter or factor.

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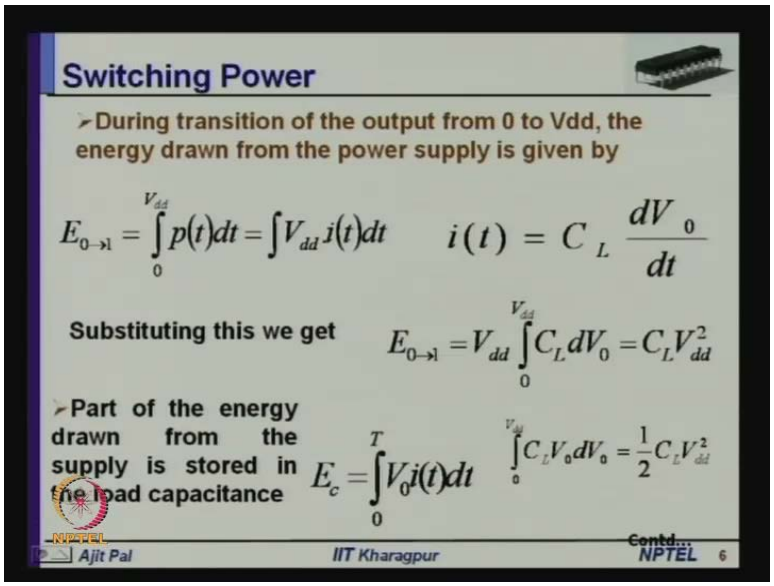

Now out of this energy how much is actually stored in the capacitor, and how much is get dissipated in that load resistance. Load resistance in this particular case is p MOS transistor network. So, let us calculate that.

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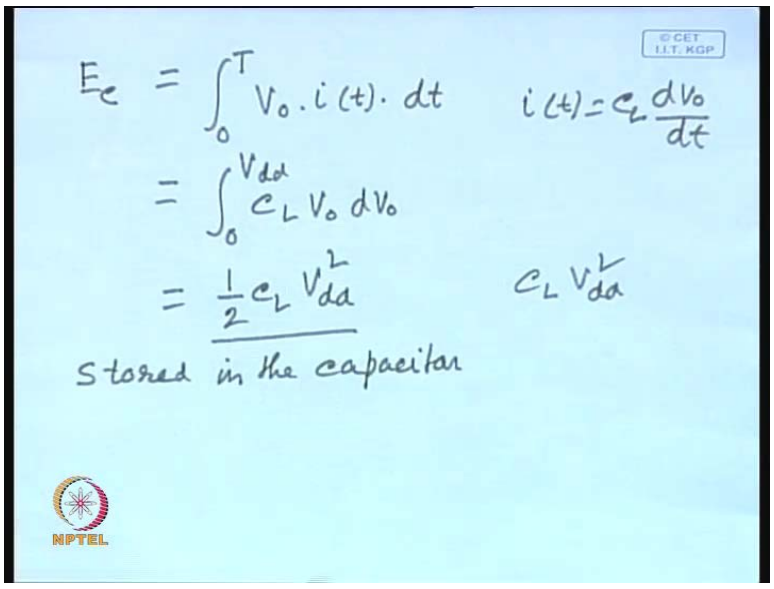

That means the energy that is being stored in this capacitor E c will be equal to. let us consider the time taken is 0 to T, is V 0 i t into d t. V 0 is the output voltage which is also the function of V 0, and current that is i t and d t. So, this we can write as 0 to V d d if we substitute i t here. It will become C L V 0 dV 0, because this d t d t will be cancel, i t as

we have seen is equal to C L dV 0 d t. So, this d t and d t will cancel out, we shall get dV 0. So, if we evaluate this, we shall get half C L V d d square. So, we find that energy that is being stored in the capacitor, is half C L V d d square; that means, out of C L V d d square, that the energy that was drawn from power source half of it is getting stored in that capacitor, that is being store in the capacitor, load capacitance and remaining half, half C L dV square, get dissipated in the p MOS transistor network or it can be single p MOS transistor in the case of the inverter. And, this remaining half of the energy will be dissipated, whenever you know the output switches from 1 to 0. So, we find that half of the energy that is drawn from the power source, gets dissipated while charging the capacitor, to raise the voltage from 0 to 1. And remaining half is getting dissipated when the output is switching from 1 to 0.

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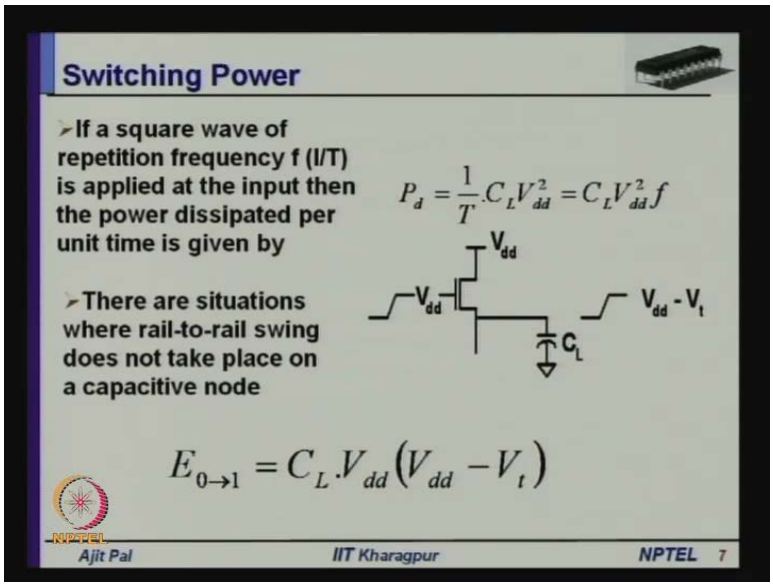

Now, there may be some there may be some situation, where if we apply a square wave to the input of **a** circuit.

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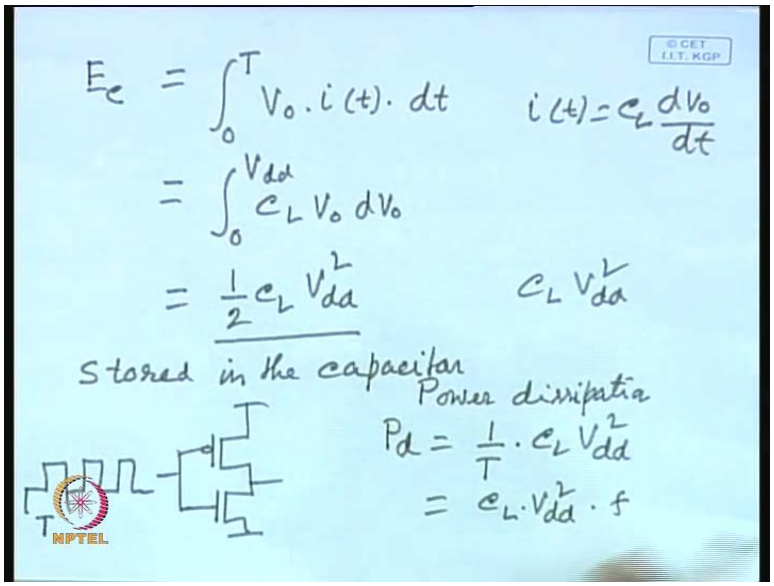

For example, we have an inverter, it is an inverter and here we have applied a clock, instead of an input; obviously, in each cycle the output will be charge, it will when the input is 0 output will be 1, and when it output is 1 it will be 0; that means, the each cycle charging and discharging will take place, so that means whenever you have applied a clock, or in other words when the output changes in each cycle of a clock, then what will be the power dissipation. So, power dissipation P d will be equal to 1 by T, because 1 by T is the time of this period. Energy was C L V d d square, so over period of time. So, whenever you calculate the power desperation it will be 1 by T into C L V d d square, or that is equal to C L V d d square into f. In other words, the power dissipation will be equal to the clock frequency, proportional to the clock frequency, so C L V d d square f that is the power dissipation that will take place.

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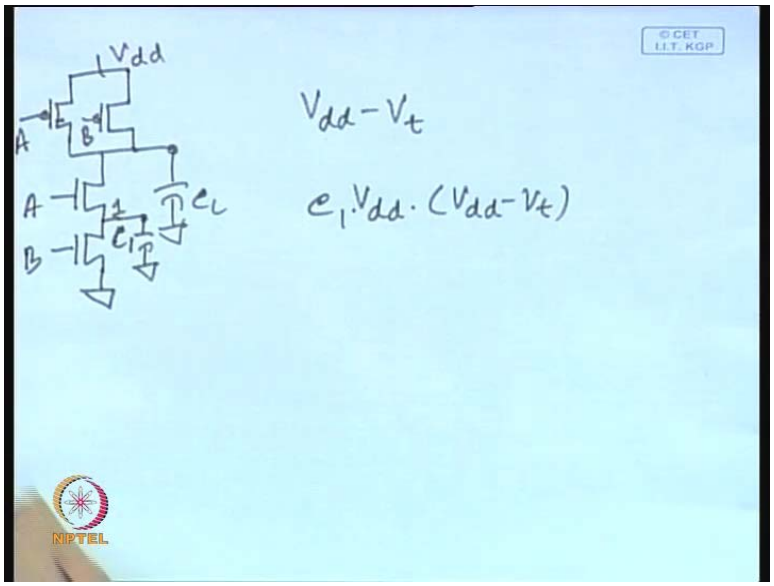

Now, you see in addition to power dissipation in the load, to be consider a circuit like this. Let us consider a simple NOR gate. So in this, in addition to this input A and B we have got. So, we have got another node this is C L and here node A, or you can say intermediate node C i, capacitance here C i, C 1 and node 1 let us assume. Now, whenever this particular node in charging and discharging, it may so what will happen this capacitor will also charge and discharge, however in this particular case, the switching will not be from 0 to V d d, because as you now whenever the charging take place through a n MOS transistor, it can charge up to V d d minus V t. So, as a consequences, the power dissipation; that means, energy that will be drawn, will be equal to V d d into C 1 into **V** d d into V d d minus V t, because it will charge, it will not charge up to V d d, but it will charge up to V d d minus V t; that mean in this expression, what we got. Here this dV 0 will not charge from 0 to V d d, but it will charge from 0 to V d d minus V t. So, as a consequences you will get here C L V d d into V d d minus V t. So, you'll be getting the power dissipation in the internal load that will not be C L V d d square, but C L V d d into V d d minus V t. So, this is what will happen.

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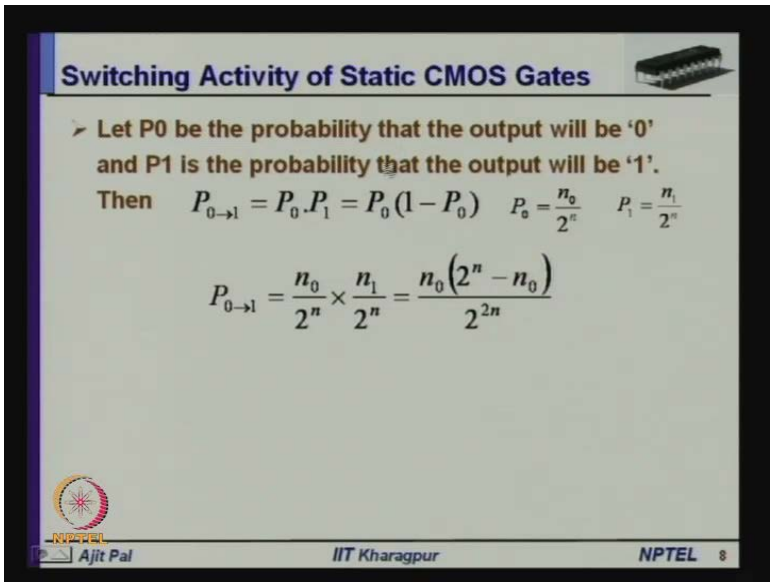

Now let us consider another very important concept that is the switching activity. Probability that the output will be 0 and how will be one, I mean when the output will be 0 and when the output will be 1, why this is necessary let us try to understand.

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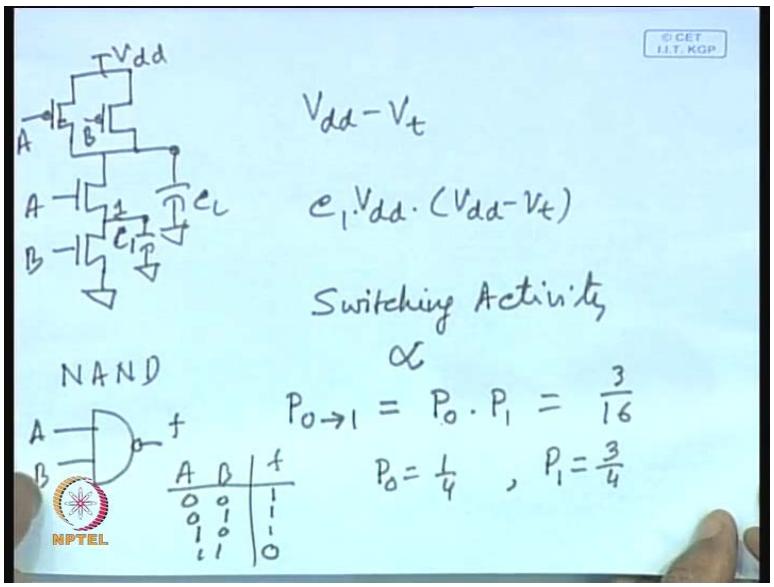

You see whenever we are considering a circuit say NAND gate, will the output change in each and every clock cycle. It will not change the output will change depending on the functionality of the circuit. So, you can calculate the probability of transition to 0 and 1, and find out the parameter known as switching activity. In this particular wherever we

derive this expression, we assume that there is transition at each and every cycle, but that will not happen, because we are not really applying the clock to a circuit. It is a complex function depending on the nature of the inputs output will change, and this will not change in each and every clock cycle. So, take into account, we have to take another factor which is known as switching activity. Switching activity; what is switching activity. Switching activity is represented by alpha. How can we calculate switching activity. Switching activity is define as probability of transition from 0 to 1, and this is equal to P 0 into P 1, what is P 0 and P 1. P 0 is actually the probability that a circuit will attain a value 0, and P 1 is a probability that a circuit will attain a value 1.

Say let us consider the NAND gate that I have drawn, we know the truth table; say A B and say f for 0 0 0 1 1 0 1 1. So, output will be 0 only for 1 1, and for all the other 3 conditions the output will be one 1, where any other input will be 0 output will be 1. Now, what is the probability of this output to have the value 0. We can find out there are four possibilities. So, out of four possibilities only once it can happen. So, in this particular case, the P 0 will be is equal to 1 by 4. And what is a value of P 1 out of four combinations, the possibilities, input possibilities; the output can have the value 1 3 times out of four. So, probability is 3 by 4; that means, if we take this over a long period of time. The switching activity or probability of transition from 0 to 1 and 1 to 0 will be equal to this 1 by 4 and 1 by 3, and this will be equal to 3 by 16. That means this switching activity will be 3 by 16, and this is the case for a NAND gate, we can generalize it.

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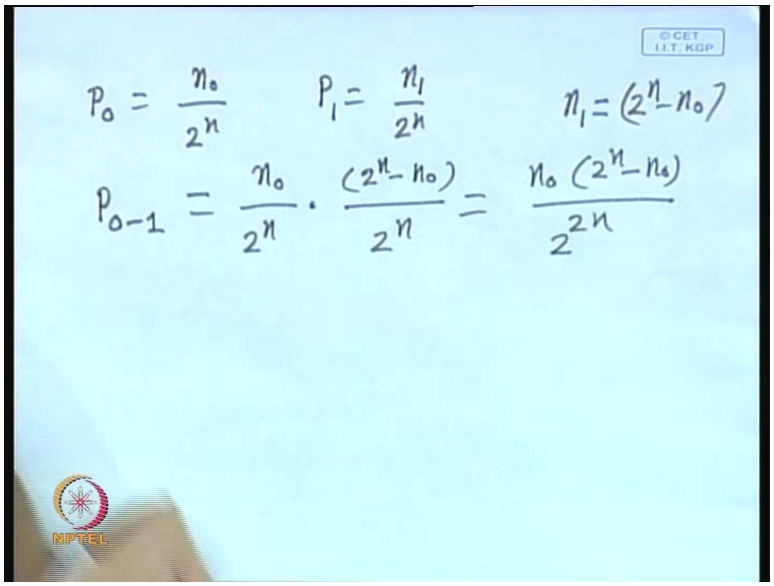

Suppose, P 0 is the probability that the output will have the value 0, will be is equal to say n 0 by 2 to the power, n 0 is the number of zeros in that truth table. You see we write the truth table, numbers of zeros in that truth table by the total number. So, that will be equal to n 0 is the total number of zeros by these are the total number of combinations. So, if P 0 is equal to n 0 2 to the power by n, and P 1 is equal to n 1 by 2 to the power n. And obviously n 1 will be equal to 2 to the power n minus n 0, because they are related. When the output is not 0 it will be 1. So therefore, P 0 to 1 for general Boolean function can be written as n 0 by 2 to the power n, into 2 to the power n minus n 0 by 2 to the power n. So, that is equal to n 0 into 2 to the power n, minus n 0 by 2 to the power 2 n. So, you find this the probability transition from 0 to 1 and 1 to 0. So, we can say this is the switching activity.

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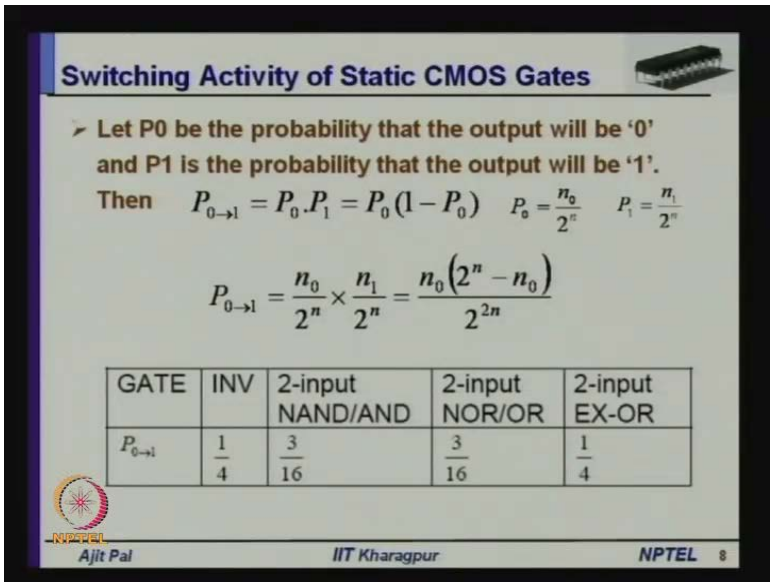

Now for different types of gates the value will be different, for inverter it is 1 by 4.

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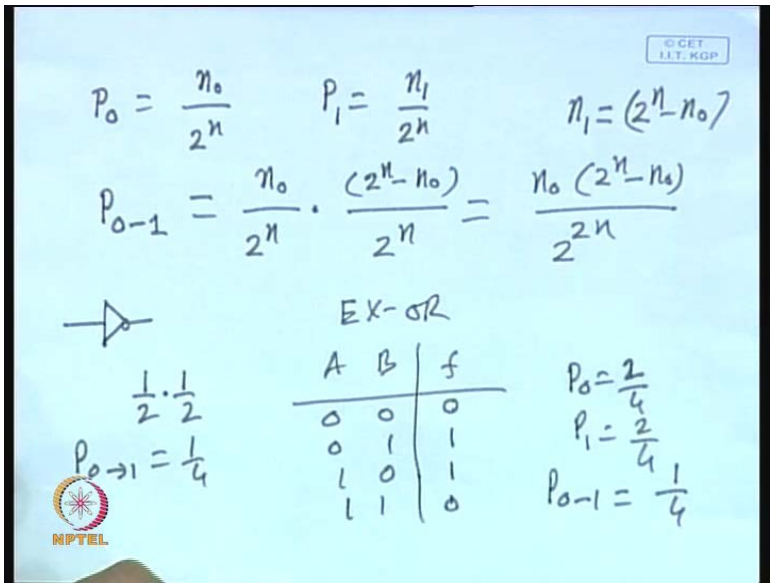

How it is 1 by 4, because in inverter as we know, you have got only one input. So, probability that the output will be 0 is half, and probability that the output will be 1 is also half; that means, P 0 to 1 for inverter is equal to 1 by 4. And for NAND and AND gates, we have already discussed it is 3 by 16. Similarly, for NAND and nor gates it will be 3 by 16. However, for 2 input EX-OR gates it will be 1 by 4 why. So, because incase of EX-OR exclusive or get, say A and B are the two inputs and this is the functions of

the EX-OR. So, 0 0 0 1 1 0 1 1 exclusive or; that means, when the output will be 1 it will be 0 here, and it will be 0 here, it will 1 here, it will be here. So, output is 0 has got two zeros and two ones, that is a reason why you are getting P 0 is equal to 2 by 4 and P 1 is equal to 2 by 4. Therefore, P 0 2 1 will be equal to 1 by 4 half into half. So, we find for exclusive or gate it will be half.

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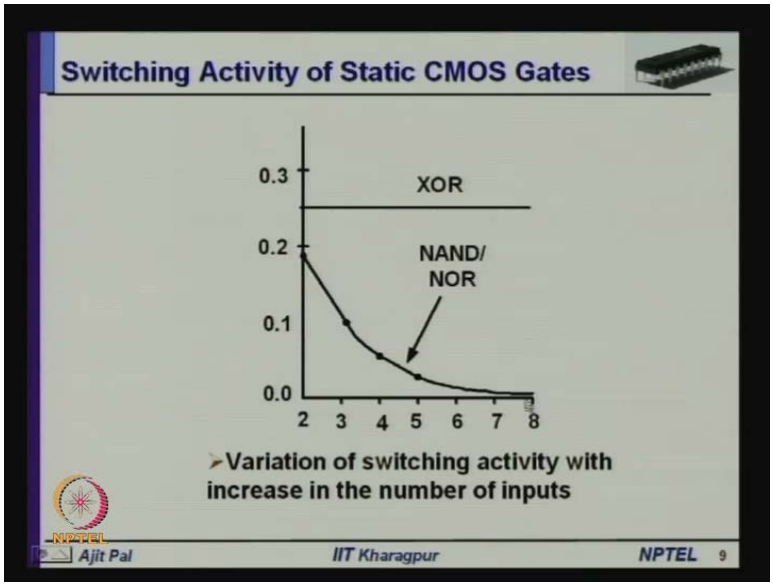

Now, let us consider how the switching activity changes with the increase in the number of inputs, as the number of inputs is increasing, how it will change. We can see for an EX-OR gate as you increase the input it remains equal to 1 by 4, that is 0.2 5, why so, because you have seen the truth table, always it will be number of 0s and number of 1s will be same, and that will be half of the total number. So, this value will be always equal to 1 by 4 EX-OR as we increase the fan-in number of inputs. On the other hand for NAND and NOR and XOR gates it will change over time. You, can see the expression that you got is this, n 0 into 2 to the power n minus n 0 by 2 to the power to the power n 2 n, and this expression as n increases it will reduced, because this factor is more. I mean this will increase ah this will have larger value compact this.

So, we find that for fan-in is equal to 2, this is little more than little less than 0.2 that is 3 by 16. And then it will be come close to 2.1 for 3 input and this way it well reduced. What message does it give. Is there any message that you are getting from this. That means, the switching power dissipations of a gate will be less if the fan-in is more; that

means, the power dissipation of the gate, on the load capacitance, charging and discharging will be less if the fan-in is more. Later on we shall see what impact it has got in realization of circuits, particularly whenever you go for a low power realization of low power circuits.

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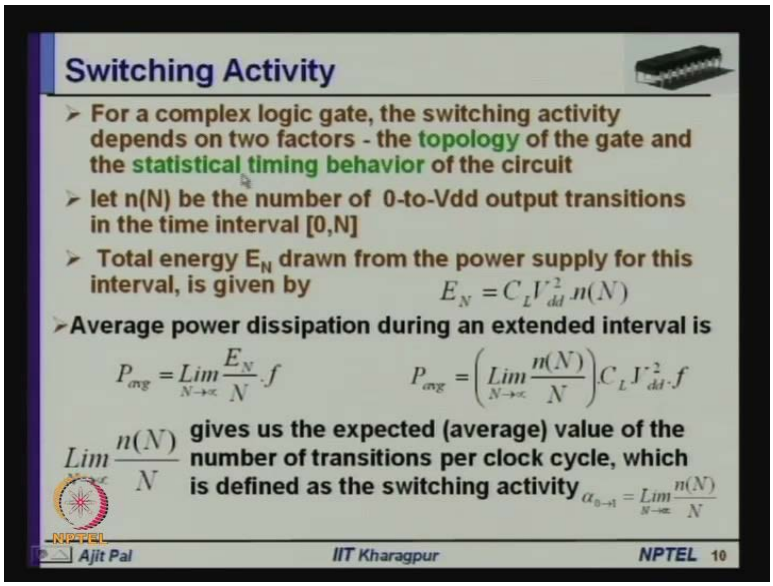

Now, so far we have seen how it happens in case of simple gates, AND gate, OR gate NAND gate, NOR gates and so on, but unfortunately in a real life the gates will not be as simple as this, it will be more complex. So, whenever it is a complex gate, then we cannot calculate the way we have found. So, for a complex gate, the switching activity depends on two factor; the topology of the gate, and the statistical timing behavior of the circuit. So, these two will affect the switching activity of the circuit. So, let us now define switching activity for a complex gate and find out an expression for it.

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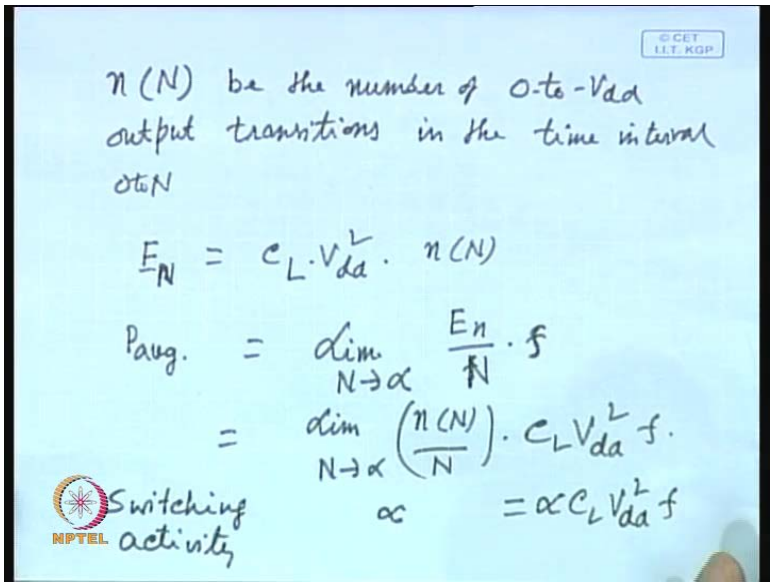

Let n N be the number of inputs, number of 0 to V d d output transitions. These are the number of output transitions that will occur in a circuit, and it in the time interval 0 to N; that means, out of n possible transitions n N is the number of transitions that is occurring from 0 to V d d. So, total energy drawn E N will be equal to, we know for each transition from 0 to 1 the energy drawn is C L V d d square. So, the total the total energy that will be drawn E N equal to C L V d d square in to n N. Now what is the power dissipation, average power dissipation, that will be equal to limit N tends to infinity, for large value of N we shall take an average E n by N into f, f is the clock frequency. So, this value of E n we can substitute here, and that will lead to limit N tends to infinity, n N by N into C L V d d square into f. This particular factor is given the simplified turn that is alpha. That means, this limit n tends to infinity n N by N this value is given the value given the symbol alpha that is switching activity. Therefore you can say that average power dissipation is equal to alpha C L V d d square and f and, that is the average power dissipation on the load capacitance C L.

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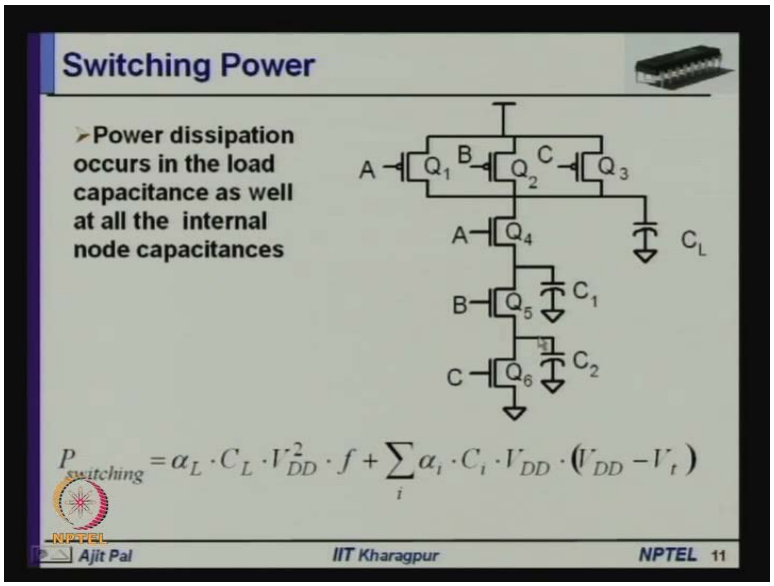

Obviously, this not the only power dissipation that will occur, there will be power dissipation in the internal loads. We find that there are various internal nodes and here A three input NAND gate is given shown. Here you can see this three input NAND gate, there are two additional nodes at this point, between the junction of Q 4 and Q 5, and between the junction of Q 5 and Q 6. So, these capacitors also will get charge or discharge.

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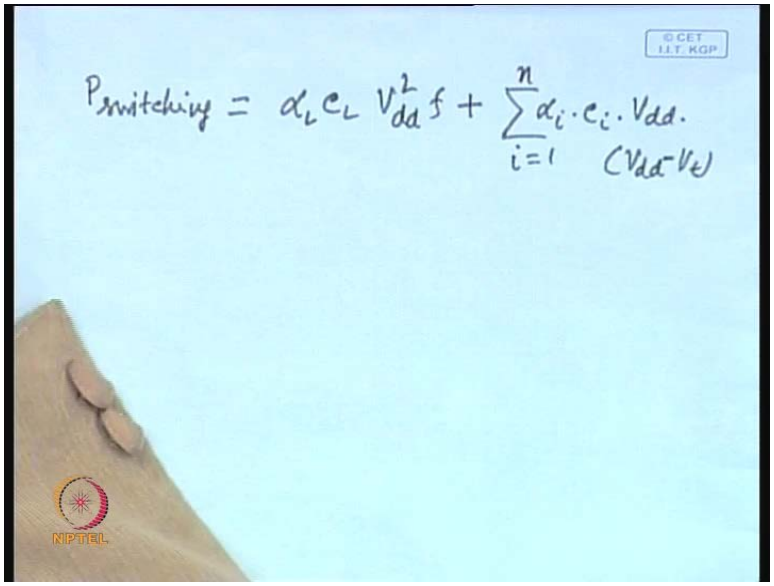

So, for generalized CMOS circuit, what is the switching power dissipation, P switching will be equal to alpha L C L. Alpha L is probability that switching activity on the load capacitance, alpha L C L V d d square f , than it mean it may have the number of internal nodes which is represented by i, two say may be n nodes are there, i is equal to 1 2 n, and you have to take summation of this power dissipation that will be equal to alpha i into C i C i is the load capacitance, alpha i is the probability the switching activity at that node, into V d d into V d d minus V t, because in this case we have seen, we have already seen that, in such situations whenever you are charging and discharging this capacitor C 1 and C 2, it will not charge to V d d, but it will charge to V d d minus V t. That is the reason why you have use the expression V d d minus V t here. So, this is the switching power dissipation in a general CMOS circuit.

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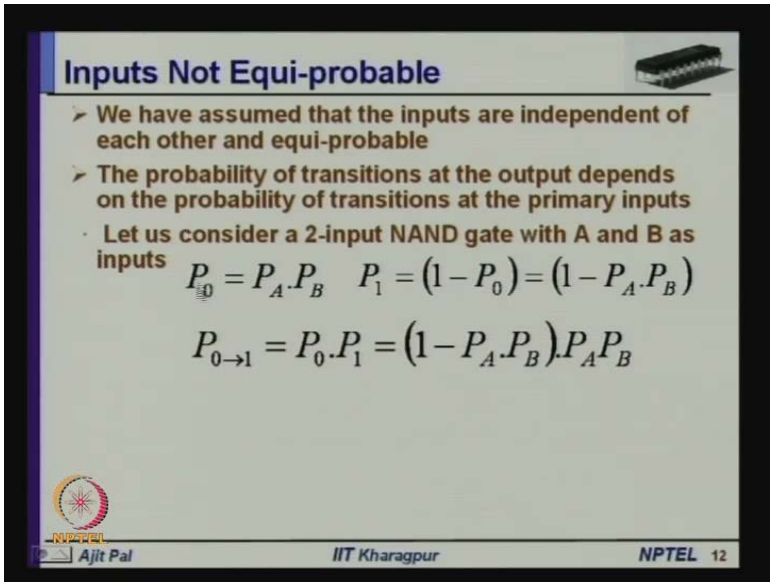

Now so, far we have assume that inputs are equi-probable, what do you mean by equi-probable; say a particular gate has got two input A and B. The probability of occurrence that we assume be same, but it will not be true in real life. Some inputs will come from one source and another input from another source, or some inputs will be generated by a complex circuit. As a consequence the inputs will not be equi-probable. Their probability of occurrence will not be same, earlier we assume they are same, or we assume probability of occurrence is one. So, in such a case how do you calculate the switching activity. The probability of transitions at the output depends on the probability of transitions at the primary inputs. So, we have to take into account, the probability of

transitions at the primary input, how do you take it into account. Let us consider A 2 input NAND gate. In case of 2 NAND gate we know that P 0 is equal to P A into P B, you know P 0 means, what is P 0 for a 2 input NAND gate.

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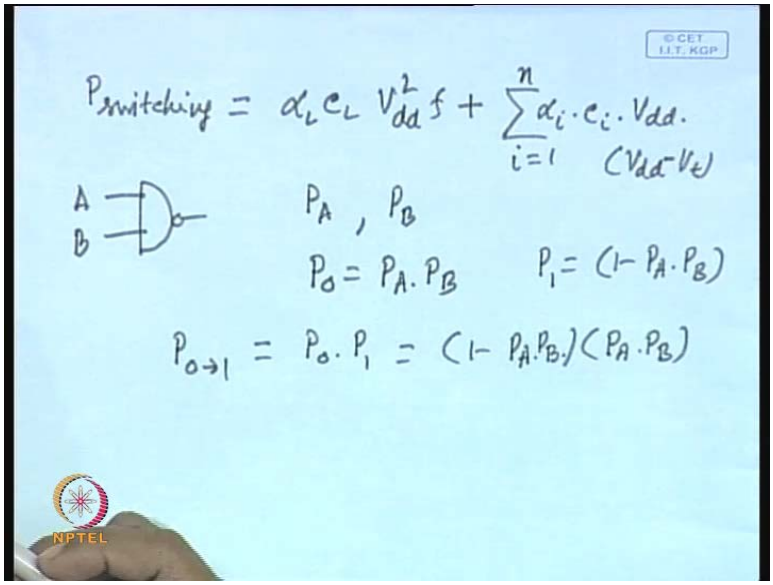

We have two input NAND gate A and B. So, P A is the probability that this node will become one, probability of transition to one, and P B is the probability of transition to one for this node B. And when the output can become 0, when both the inputs are one, therefore P 0 will be equal to P A into P B, and however your P 1 will be equal to 1 minus P A into P B. So, we find that P 0 is no longer 1 by 4 or P 1 is no longer 3 by 4 in this particular case, because it depends on the probability of transition to one, and transition of probability to zero, that will be different. Therefore, P 0 to 1 which is the switching activity, which will be equal to P 0 into P 1 for a NAND gate, will be equal to 1 minus P A P B into P A P B.

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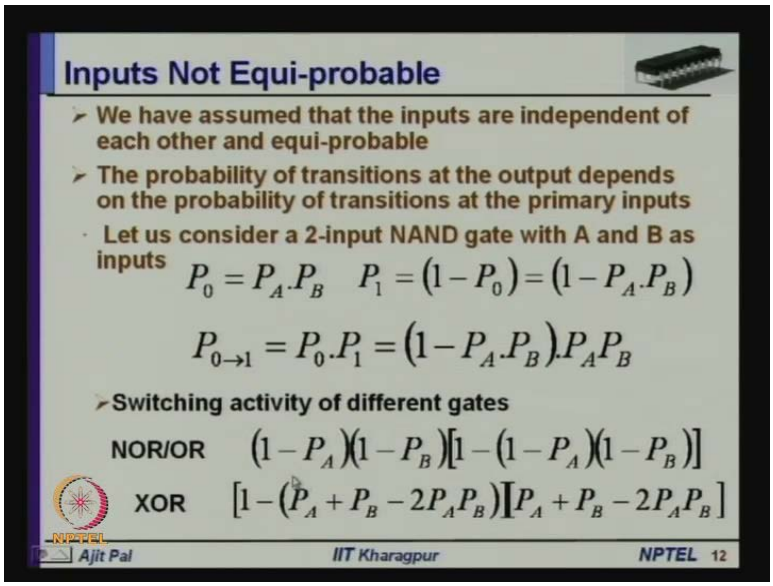

So, we find that whenever the inputs are not equi-probable in this way we can find out the switching activity. And similarly the switching activity of NOR gate, we can find out that for a NOR gate it will equal to 1 minus P A into 1 minus P B, probability of transitions to zero, and probability of transition to one, and you can multiply NOR gate, this is the situation. For EX-OR gate it will equal to 2 1 minus P A plus P B minus 2 P A P B into P A plus P B minus 2 P A P B. So, we find it is little complex, whenever we take into account the probability of transition for different inputs, coming from different sources. In fact with the help of a simple NAND gate, if the output is coming from NAND gate, we can find out the probability of transitions.

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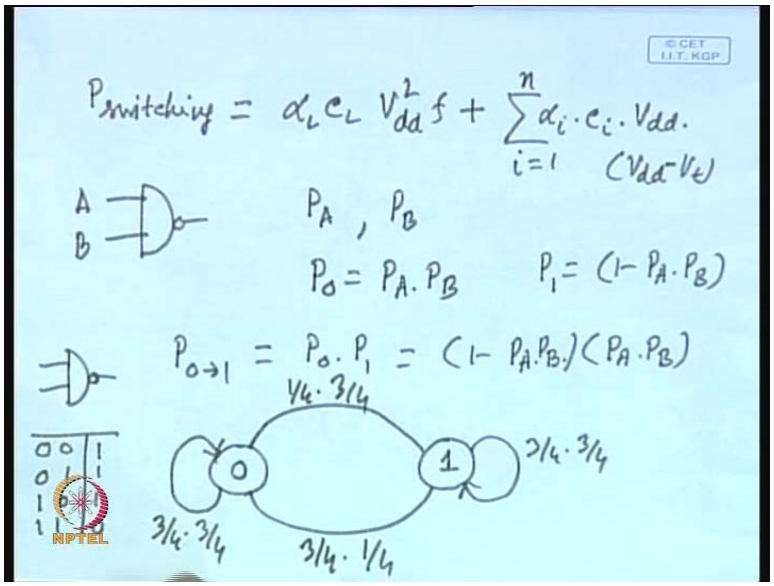

For example say, we have got a NAND gate, and as we know the inputs may be equi-probable here, but here the probability of transition to 0 and 1 are not equi-probable. So, as we know, suppose this is when the circuit is in the 0 and this is when it is 1. What is the probability of transition from 0 to 0 for a NAND gate. For a NAND gate we know that 0 0 0 1, 1 0 1 1 output is 0 only here. So, in this case these are 1. So, probability from 0 to 0 is 3 by 4 into 3 by 4, probability from for a transition from 0 to 0 be 3 by 2 for 4 3 by 4 probability of transition from 0 to 1 will be equal to from 0 to 1, it will equal to 1 by 4 into 3 by 4. Similarly, probability for transition from 1 to 1, will be equal 3 by 4 into 3 by 4, and probability transition from 1 to 0, 1 to 0 will be equal to 3 by 4 into 1 by 4. So, you find that probability of transitions to 0 1 and the output of a NAND gate is not same, 1 to 0 and 0 to 1. That is the reason why this type of probability is taken into consideration. And in a complex circuit, that computation of switching activity is not very simple. However, it can be done the way the way explained.

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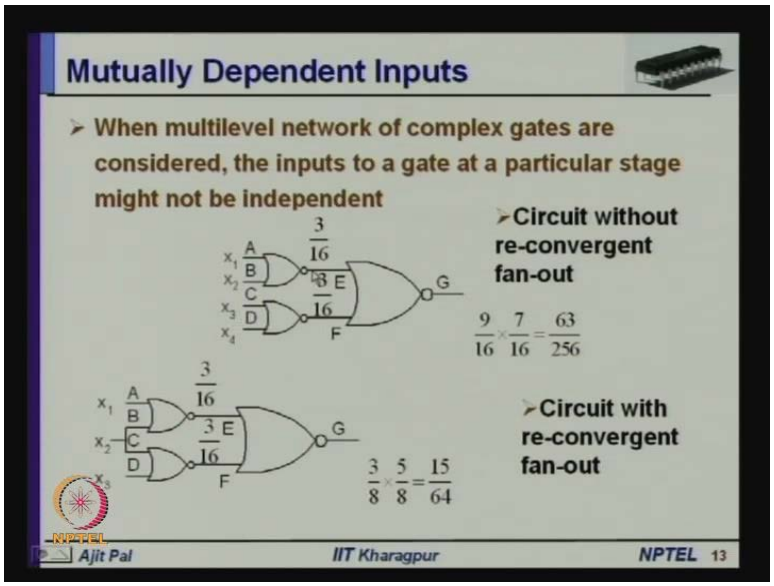

Now, there is another complexity in our circuits. Earlier we assume that all the inputs are independent. So, if the inputs are coming from different sources, and there is no correlation among them, obviously they will be independent, but in reality they cannot be solved. So, there can be some inputs, I mean some input will appear and again the function generated by it, will converge with another signal. For example, let us consider a simple circuit. Here I have taken a two level circuit, here it is a NOR gate, two input NOR gate with input X 1 and X 2, and here we have another gate with input X 3 and X 4. So, we find that the probability these X 1 X 2 X 3 and X 4 all are independent. So, the switching activity at this point will be 3 by 16.

Similarly, the switching activity will be 3 by 16, and if we consider the output the switching activity here will be 63 by 256, but suppose these two are tied together, these two are tied together, then what will happen. Then what will happen the switching activity, this output and this output, are no longer independent. Here this is main independent these two are independent input, but here these two are not independent, and as consequence here the probability of transitions will be 3 by 5 into 5 by 8, and as a consequence the switching activity becomes more, 15 by 64 and. In fact, it can be illustrated with a more simple circuit.

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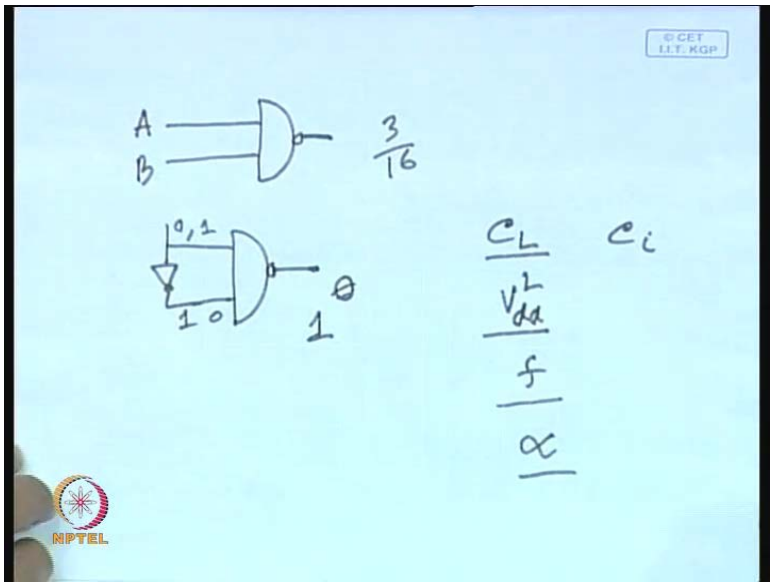

For example, we have a simple NAND gate. Now in this case we have applied two inputs A and B, and as we know the switching activity here will be 3 by 16. Now suppose what we do, we apply an inverter and apply to the two inputs. In this case what will happen, what will be the switching activity. So, in this case when ever this is 0 this is 1 and when ever is 1, this is 0. So, what will be the switching activity here. And surprisingly you will find that since A and B these two are correlated, the switching activity will be 0 here, because output will be always 0, as you know in a NAND gate, whenever you apply any input one, output will be always zero, the switching activity will be zero, output will be always remain one, so whenever you apply this kind of thing. That means, in this type of, whenever there is a convergent inputs, the convergent outputs are taken together then the switching activity increases. And in this particular case we have seen it has decreased; that means, it had become zero switching activity become zero.

So this mutually dependent inputs you have to take into account, when multilevel network of complex gates are considered, the inputs to a gate at a particular stage might not be independent. So, you have to take into account this in your circuits. With this let us come to the end of today's lecture. We have discussed about the one very important sources of power dissipation, that is your switching power dissipation in CMOS circuit, and we have seen it is proportional to what parameters. You have to consider the important parameters, on which it is depends; C L load capacitance or if it is internal

load C i then it will be dependent on V d d, and particularly we find that there is a square law dependence V d d square, and also it depends on frequency. So from this, what is our observation. Our observation, why we are studying sources of power dissipation, essentially we are trying to identify the enemies.

So, here our enemies are capacitance, supply voltage and frequency. So we find, if we want to reduce switching power, we have to reduce load capacitance, we have to reduce supply voltage, and we have frequency. So, later on whenever we shall discuss, techniques for reducing switching power dissipation, we have to focus primary level supply voltage, because the switching power dissipation heavily depends on supply voltage. And of course, the another parameter I did not mentioned, that is your switching activity. So, these are the parameters on which we shall concentrate, and we have to minimize or reduce one of these four parameters, to reduce switching power dissipation. So, with this let us come to the end of today's lecture. Thank you