Low Power VLSI Circuits and Systems

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Lecture No. # 13

MOS Dynamic Circuits-II

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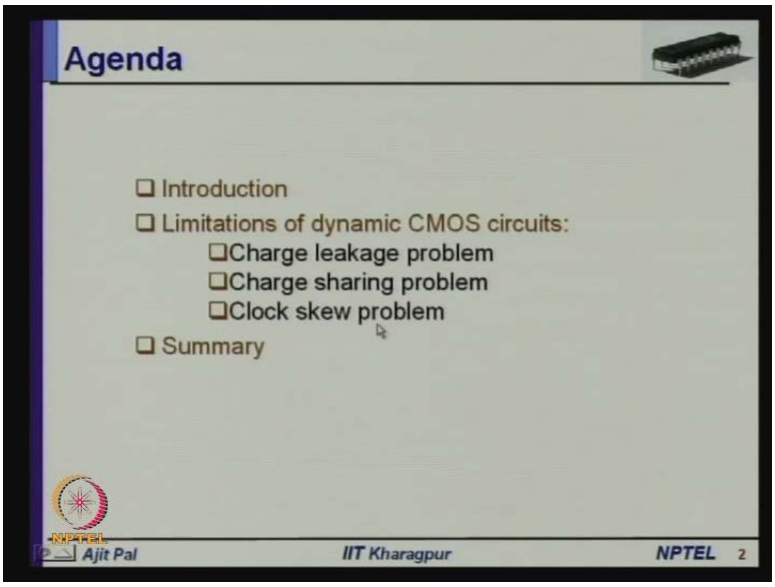

Hello and welcome to the second lecture on MOS dynamic circuits, and here is the agenda of today's lecture, after a brief introduction where I shall recapitulate what has been discussed in the last lecture in brief. And then we shall discuss about various limitations of dynamic CMOS circuits in this lecture, as we have mentioned in the last lecture there are three serious limitations; number one is charge leakage problem, second one is charge sharing problem, third is clock skew problem. And we shall discuss how these problems can be overcome with the help of additional circuits. Finally, I shall end my talk with a brief summary.

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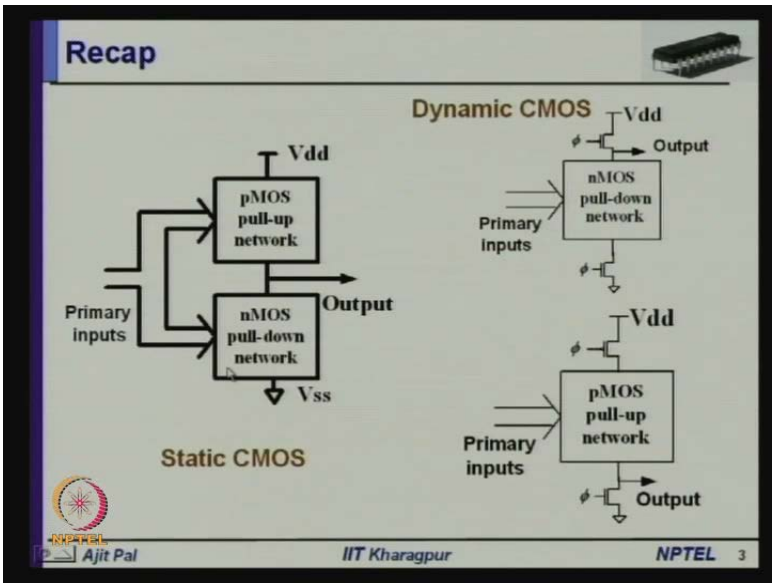

Here, is a brief recap about what we discussed in the last lecture, as we know static CMOS circuits can be realized, by using a pMOS pull-down network, and a pMOS pull-up network, and a n-MOS pull-down network, and inputs are applied to both of them and output is taken from the middle of these two points. And we can realize dynamic CMOS circuits, either by using the nMOS pull-down network, as you can see in this diagram only the nMOS pull-down network is used. Of course, we have got two additional transistors; one is footer transistor, which is a nMOS transistor, and a header transistor which is a pMOS transistor. So, these two transistors are there where a common clock is applied, and as usual primary inputs are applied to the nMOS pull-down network and output is taken from the source of the pMOS transistor.

Similarly, we can use only the pMOS pull-down, pull-up network part, and you can see the header and footer transistors are there as usual. However, in this particular case output has to be taken from the top of the footer transistor. So, instead of taking the output from the source of the pull-down pull-up transistor, that is pMOS transistor, here you are output taking taking the output from the drain of the pull-down transistor. So, as you can see, we are not duplicating pMOS and nMOS network only one of them is used as a consequence.

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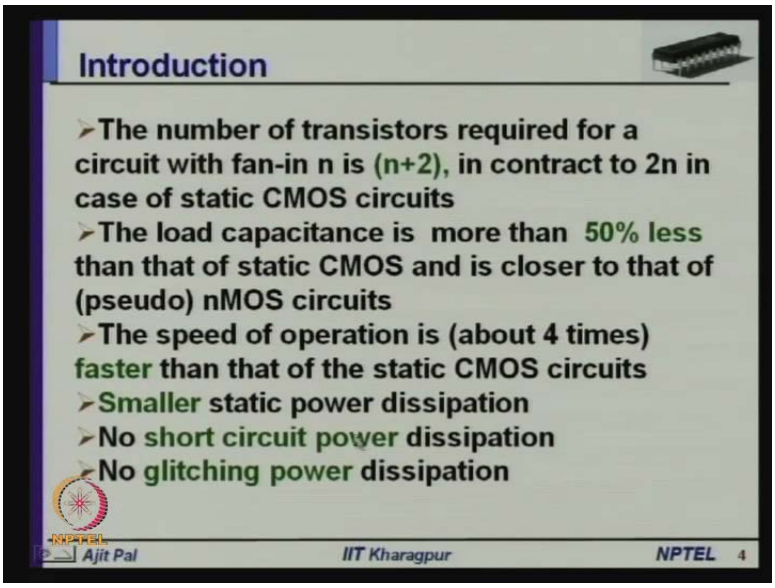

It has got many advantages as I mentioned, number one is; the number of transistors required for a circuit with fan-in n is n plus 2 in case of static CMOS circuit, I mean n plus 2 in contrast to 2n in case of static CMOS circuits. We have same in case of static CMOS you will require n transistors here, n transistors here. So, 2n transistors are required, where as you require n transistors here and two more. So, you require n plus 2 in this configuration, as well as here also you will require two additional transistor and n transistor, so n plus 2 in both the cases.

And the load capacitance is more than 50 percent less than that of static CMOS, and is closer to that of pseudo nMOS. This is because you can see this output is will go to a next stage, where both pMOS and nMOS transistors are present here, but in case of dynamic CMOS circuits the output will be going, only to the to the n-MOS network or pMOS network as a consequence the capacitance will be less than 50 percent that of static CMOS circuits, and as a consequence the circuits are faster and as I mentioned the speed of operation is about fourth times faster than that of static CMOS circuits.

So, we get very high speed of operation, and also the static power dissipation is very small. The reason for that is there is no short circuit path, I mean at no point of time there is direct path from V d d to ground, because either this transistor is on or this transistor is on, and as a consequence there the static power dissipation is not there. Moreover, there is no short circuit power dissipation as it is present in static CMOS circuits. we know that

in case of static CMOS circuits when the input is changing from 0 to V d d in the region between V t n to V d d minus V t p, there is a short circuit path through the pMOS and n nMOS network, but in this particular case that does not arise, because you can see it has got two phases and as I mentioned pre-charge and evaluation phase, and one of the two transistors is always on and as a consequence at no point of time, there is current path from V d d to ground. So, there is no short circuit power dissipation in both these configurations.

Finally, there is no glitching power dissipation as well in case of dynamic CMOS circuits. The reason for that is, in case of static CMOS a circuit depending on the change in the inputs. If the input keeps on changing in a multi-level network, the inputs can arrive at different points of time, that may lead to change in the output from 0 to 1, 1 to 0 before settling down to a final value. So, the output may keep on changing, before the output is finally settled down after a certain delay. There can be many changes, that may lead to what is known as glitching power dissipation, but that is also not present in case of dynamic CMOS circuits, because as you know in the pre-charge phase the output is pre-charged to high level, and only transition that can occur after the, I mean in the evaluation phase is in this particular case 1 to 0, no two or three times change is possible here.

Similarly, here the only change that can occur in the evaluation phase is from 0 to 1 or it may remain 0. So, only one transition is possible. So, there is no glitching power dissipation in dynamic CMOS circuits. So, you may argue that the dynamic CMOS circuits has have so many advantages, why everybody is not realizing circuits using only dynamic CMOS circuits, that question may arise, but as we shall see there are some limitations as well, and those limitations are very serious and in my last lecture I mentioned about these limitations.

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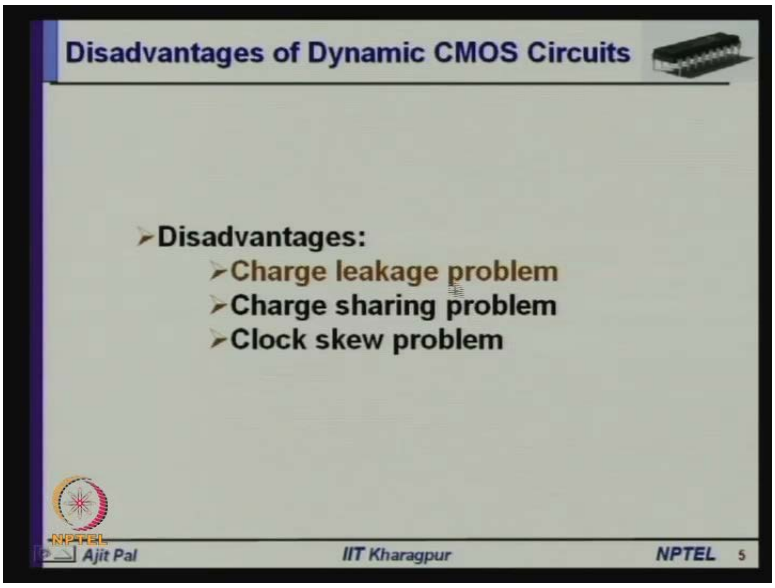

These limitations are; number one is charge leakage problem, second is charge sharing problem third is clock skew problem. So, in this lecture I shall discuss about these limitations one after the other and we shall also see how these problems can be overcome.

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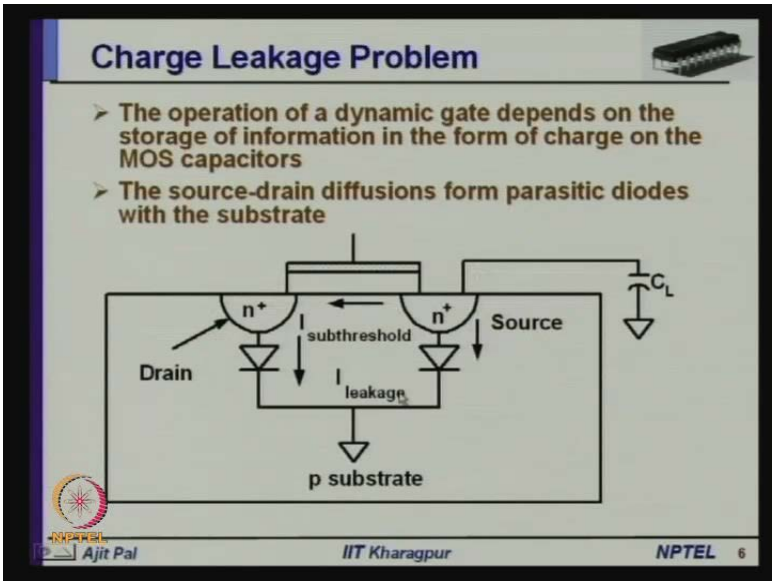

First, let us consider the charge leakage problem. As you know the operation of a dynamic gate depends on the storage of information in the form of charge on the MOS capacitor. So, as we have seen you are in a dynamic CMOS circuit.

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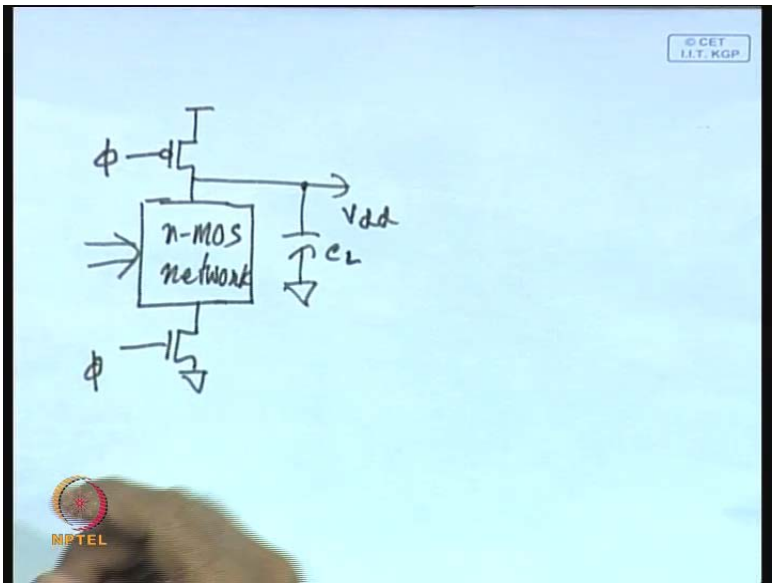

Let us assume, it is realized by using the nMOS network, and you have got a n-MOS network, and you have got two transistor, this is the footer transistor this is the header transistor, you are applying clock phi, you are applying clock phi here and inputs are applied here and output is taken from here, and there is a capacitors, let us assume this is the load capacitance. Of course, this is there is no discrete capacitors that is connected this is essentially, the intense capacitance of the next change that acts as a storage element. Now, during the pre-charge phase this is charged to V d d, and during evaluation phase if there is no path through the n-MOS network, then this voltage is retained, but how long it will retain.

Suppose, the clock period is too long, in such a case what will happen? The capacitor will discharge through this through this n-MOS network path, but as I mentioned the n-MOS network is off, but unfortunately although it is off, you know there are diodes, which are reverse biased and through this reverse biased diode this capacitor will discharge, and there may not be just one reverse biased diode. There may be a number of reverse biased diode connected to this point, and as a consequence as you know there is a diode has a reverse biased current, and that current may not be very small and if it occurs for a long duration, that capacitance will discharge, I mean that capacitor will discharge leading to degradation in the output level.

So, this source to drain diffusions from the parasitic diode with the substrate, as it is shown here, and through that diode this capacitor will keep on discharging. And it may happen that the output will degrade to such a level that next stage will treated as a low level. So, you have to prevent this. Normally you are familiar with you know dynamic ram; in the dynamic ram also you use capacitors to store information. So, what do you do in that case there also you will face the same problem. In case of dynamic CMOS what you normally do you keep on refreshing at regular interval. There is a built in refreshing circuit and which keeps on refreshing about regular interval, before the output level goes down below certain threshold level. So, this is what is done in case of dynamic ram.

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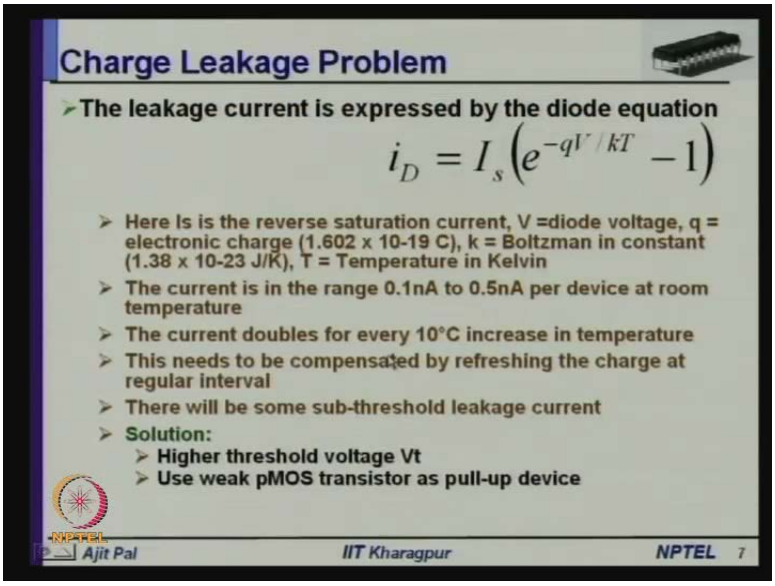

But in this particular case what we can do, we shall discuss, and here some here is some estimate about the diode leakage current. This is the reverse saturation I mean reverse biased current expression i d is equal to is into e to the power minus q V by k T minus 1. As you can see these parameters, q is the charge of electron, k is the Boltzmann constant T is the temperature absolute temperature in Kelvin, and then V is the diode voltage reverse biased voltage that is being applied this V. And this current has been found to the order 0.1 nano ampere to 0.5 nano ampere at room temperature, but because of the presence of this temperature parameter in this expression, the current doubles for every 10 degree increase in temperature. So, you know if the device becomes hot, then leakage current is larger, and for every 10 degree increase in temperature, this leakage current

doubles. So, you have to take precaution about it, particularly when the chip is getting is will become little hot.

Now, how can you really compensate this, what can be done, whatever loss in charge occurs that can be refreshed, by charging at regular interval. Another alternative is there will be, I mean in addition to that current, this reverse biased diode current. Nowadays, some current flows through this channel as well, which is known as sub-threshold leakage current that too also is not very small, in the present day technology, particularly deep submicron technology. Sub-threshold leakage current is also substantial, and as a consequence you have to minimize these currents or you have to make arrangement to replenish them. The sub-threshold leakage current can be minimized by using a transistor of high, higher threshold voltage V t.

So, as you know the sub-threshold leakage current is dependent on the threshold voltage of the device. If the threshold voltage is high the sub-threshold leakage current will be very small, and as a consequence it is recommended that the threshold voltage should be on the higher side to reduce this leakage. Third is use of weak pMOS transistor as pull-up device, weak pMOS transistor can be, this use of weak pMOS transistor as pull-up device. I shall explain while discussing the next limitation, because this weak pMOS transistor is used to overcome the second limitation that we shall discuss. So, we shall discuss it together very soon. So, coming to the second problem that is your charge sharing problem, what is charge sharing problem.

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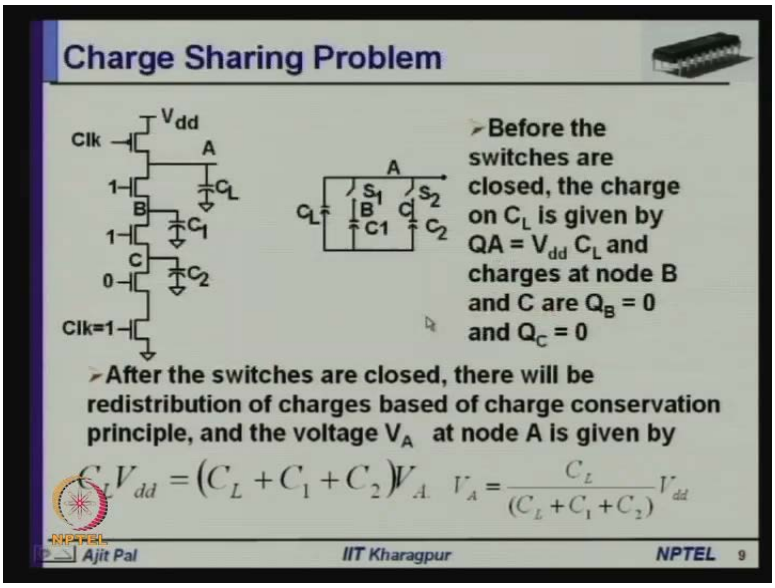

Let us try to understand with the help of this diagram, let me redraw this to explain in little more detail.

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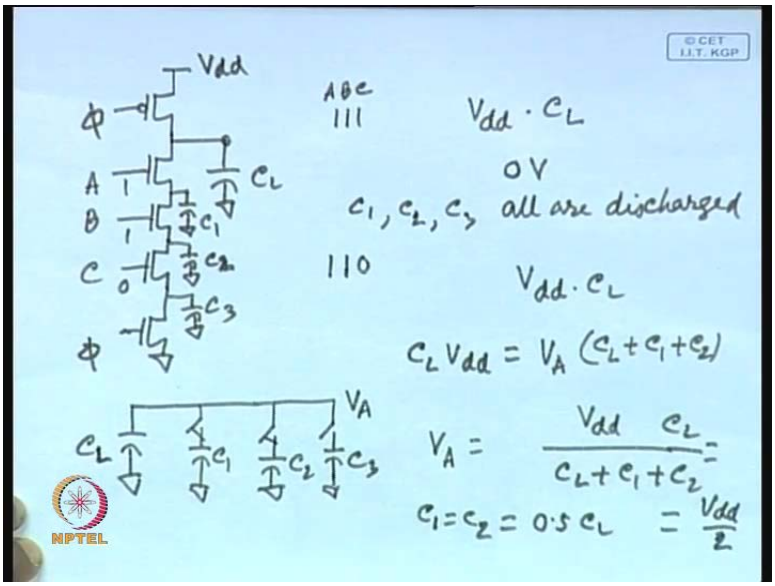

Let us assume we have a simple circuit, a three input NAND gate is realized. So, it is a three input NAND gate. Of course, this is the dynamic version of three input NAND gate here you have got three inputs A B and C, and here is the footer transistor connected to ground header pMOS transistor connected to supply voltage V d d, and you have applied clock phi, clock phi to these inputs, and here is the typical load capacitance that we

considered, in addition to that each each of this junctions will have some capacitance associated with it, and here also there will be some capacitance associated with it. Let us assume this is C 1 this is C 2 this is this is C 3.

So, initially let us assume the input is 1 1 1, what will happen; whenever the inputs are 1 1 1; that means, A B and C all are 1, in that case it can be modelled as you know in this case what will happen. There will be a in the evaluation phase, during the pre-charge phase this capacitor will charged to V d d. So, it will have a charge to V d d level. So, it will have a charge equal to C d d into V l that is the amount of the charge it will be holding.

Now, then during the evaluation phase when 1 1 1 is applied what will happen, this capacitors will discharge, these capacitors will discharge C L C 1 C 2, all the capacitors will discharge, because this is connected to ground, this is also shorted, this is also shorted and so on. So, as a consequence at the output you will get 0 volt after evaluation, the 0 volt and also this capacitor, this capacitor C 1 C 2 C 3 all are C 1 C 2 C 3 all are discharged during evaluation. Now, let us assume that we are now applying another input during evaluation, this input. We are changing the input from 1 1 1 to 1 1 0.

So, in this case during pre-charge, this capacitor will hold an amount of charge which is equal to V d d into C L. Now, C 1 C 2 C 3 were not having any charge, now the input is applied here is 1 1 and 0. So, what will happen, these two transistors will turn on and these two transistors will turn off. So, we can model the situation by this as if this is now off, so this need not be connected, we have three capacitors C L, this capacitor is connected through a switch, so there is a switch, this is C 1 and another switch, another capacitor C 2. However, in this particular case this is off, and also we have got another transistor is there, another capacitor is there. So, this is also connected to ground C 3.

Now, what is happening, now we are closing this switch closing this switch for this input, but this is off. So, the charge that was accumulated in this capacitor C L we will now get redistributed in C 1 and C 2. So, what we can say that now C L V d d will be equal to. Let us assume after redistribution of the charge it attends a voltage V A. This is the node let us assume. This is this is the voltage here will be V A. So, V A into, now the same charges distributed. So, this will be equal to C L plus C L plus C 1 plus C 2, because these are the three capacitor same voltage, now these are connected. So this

charge and this charge will be same, because of the law of preservation, we can say that the charge amount will remain same, but it will get distributed instead of in one capacitor, it will be distributed in three capacitors. Now, what is the output voltage V A is now equal to V d d by here is C L by C L plus C 1 plus C 2.

So, let us assume that C 1 is equal to C 2 is equal to 0.5 C L. Then if we substitute it here what will happen, then this will become equal to with this value, this will become equal to V d d by 2. So, we can see that after distribution of the charge redistribution of the charge the output is becoming V d d by 2, but ideally it (( )) may remained at V d d. So, what is happening in this case, what is happening, because of the parasitic capacitances present in the internal nodes, the charge that was the load capacitance was holding at the time of pre-charge will get redistributed in other those parasitic capacitances, leading to reduction in the output voltage, and that output level can be so low, that it may be treated as a low level not high level. So, this is the problem of charge sharing problem. So, we have explained it and we are getting a lower voltage, how this problem can be overcome.

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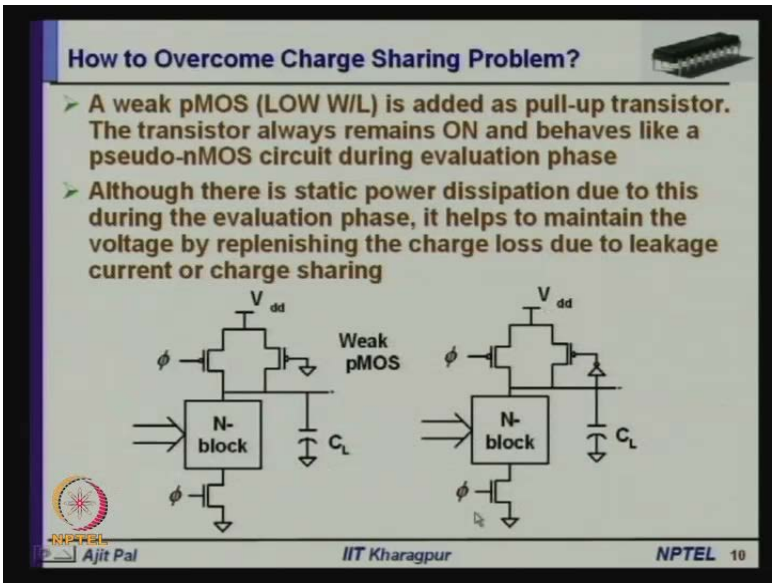

This problem can be overcome by using a weak pMOS transistor as I explained, as I mentioned in the last case. This is also used to overcome the problem of charge leakage problem. So, a weak pMOS is added as pull-up transistor, this transistor always remains on and behaves like a pseudo n-MOS circuit during evaluation period. So, it will be somewhat like this.

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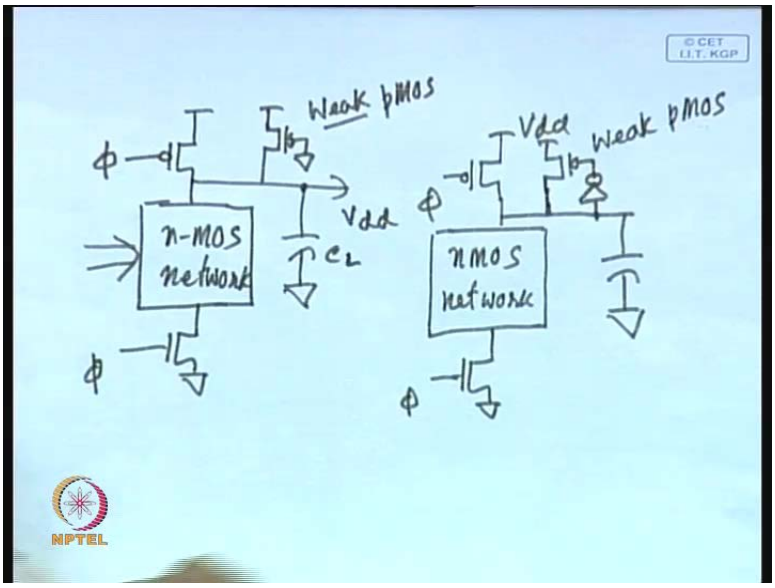

So, what you are doing, you are essentially. So, this is the standard dynamic CMOS circuit, we will be you'll be adding one additional transistor here. This is a weak pMOS what do you really mean by weak pMOS. This weak pMOS transistor is always on, because it is grounded. So, it is acting like a pseudo n-MOS circuit during evaluation, because during evaluation this transistor is off, but this part is on. So, it is acting as a kind of pseudo n-MOS circuit, and this by weak I mean that resistance is very high. In other words the current that it will supply is very small, when the resistance is high current that will be, it will supply to the load capacitance will be small, and as a consequence it will replenish the charge that is lost; either due to leakage problem or due to charge sharing problem; that means, it will you know replenish the charge, that that can get lost due to charge sharing and charge distribution problem, charge sharing or charge leakage problem. So, this is one solution that can be used.

However, you know during evaluation phase, as we can see the output will not be exactly V d d, because there will be some drop across it, but drop across it, because the. Of course, high level voltage we are not concerned about high level voltage will be charged to V d d, low level voltage in any case will be maintained. So, it will not really affect the operation of the circuit. The reason for that is the output will be discharged through this path, and since this is a stronger this n-MOS network is much more stronger, the output will be pull-down to almost 0 level. Now, one disadvantage is that during the time when

this output is supposed to be 0, this is also on this problem can be overcome by making little modification, what we can do, we can add one inverter at the output.

So, this is your n-MOS network and this is phi, this is connected to V d d. Now, the weak pMOS transistor is there, but weak pMOS transistor is connected, not I mean the gate is not grounded, but there is an inverter and which is connected to the output. So, that means, during pre-charge phase this is one, so this will be 0. So, this will be on; that means, during pre-charge phase, this will help this transistor and during evaluation phase, when the output is going down to 0, this will become 1. So, this will turn off so; that means, during evaluation phase this will not fight with the current, that will pass through this n-MOS network. So, that this is the advantage of applying a using a inverter connected to the gate, but you require two additional transistors to realize the circuit.

So, you will be having a weak pMOS as usual, but with an inverter. So, we we can see that, a weak pMOS with low W by L is added as pull-up transistor. The transistor always remains on and behaves like a pseudo n-MOS circuit during evaluation phase; that is one possibility. And although there is static power dissipation due to this during evaluation phase. There will be static power dissipation as I mentioned, whenever this output is low it helps to maintain the voltage by replenishing the charge loss due to leakage current or charge sharing, both the problems are solved; however, whenever you are adding an inverter, then this problem is overcome, you know that when the output is 0, then this will be 1, this transistor will turn off.

So, in such a case that static power dissipation will not be there; that means, the static power dissipation is also overcome by adding that inverter. So, this is how we can really overcome the charge sharing problem, and also the leakage current problem of dynamic CMOS circuits. Now, let us consider the third problem; clock skew problem, clock skew problem arises in dynamic CMOS circuits, particularly whenever you are realizing multilevel circuits. Normally, you cannot realize a circuit by using a single stage; you have to use multi stage circuit; that means you will be using several stages.

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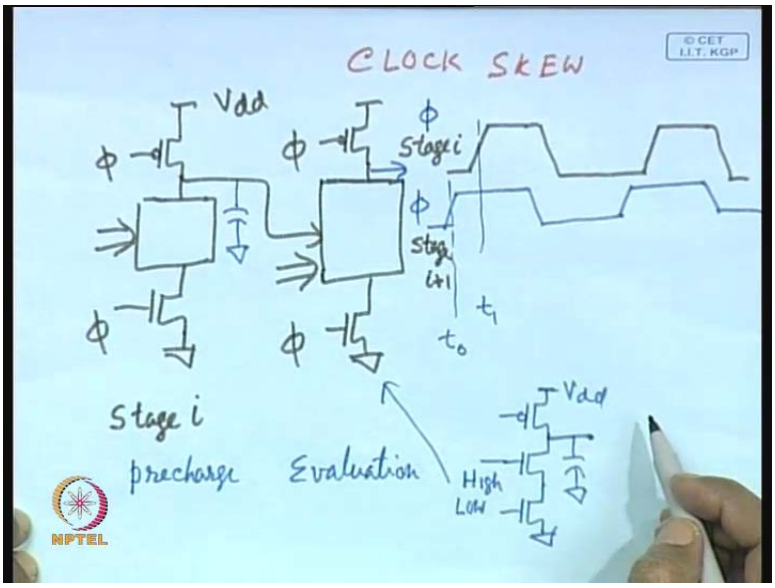

For example, you will be using let us assume, this is one stage, this is one stage. This output will be applied to next stage. Only two stages are shown here, there can be multiple such stages. So, in addition to the output coming from this stage there will be some primary inputs to the next stage as well, and this is connected to ground, this is connected to V d d . So, in this particular case as you can see the output of one stage is applied to the as used as input to the next stage. Now, whenever this is being done, this clock skew problem arises, clock skew, why does it arise. Clock skew problem arises, because you have to distribute the clock throughout the entire circuit, but the depending on the clock tri-network, the clock signal can reach different points of the circuit at different points of the time, different points of time, because of different amounts of delay of the clock tree network.

So, although we are assuming that clock is reaching at the same instant to different points in the circuit. So, here is you have used phi, here also you have used phi here you use phi, here also you have used phi. So, all of them are supposed to receive the clock at the same instant of time, but in reality that will not be so, the reason for that is you know there will be some inter connect, it will have some finite parasitic capacitances and resistances and as a consequence there will be some delay. S

o, it may so happen that the clock that will arrive to the first stage will come later than the second stage, it may so happen like that. So, let us assume, this is the clock, this is

the clock of the stage, let us assume this is your stage i. So, this is the clock of stage i and. So, this is the clock of stage i plus 1, what I am telling what can happen the clock about stage i plus one has reached I mean the clock has arrived earlier to stage i plus one than stage i so; that means, if we draw here. So, it will come little earlier shifted in time.

So, what is happened you can see here this at this time t 1, it is reaching at stage i at time t 0 this is reaching next stage, what is the consequence of this, what problem can arise, because of this. This is the clock skew problem, what is the outcome of this clock skew problem; you may note there that when this phi is 0, clock is 0. This is both are phi, but at different instant of time they have reached the different points of this circuit. So, when phi is 0 that time a particular stage is in pre-charge phase, we know that. At that point of time output is charged to high levels; that means, during pre-charge phase this point will be charged to V d d, but when phi is equal to 1, that time it is the evaluation phase of the next stage; that means, here this is the evaluation phase of the next stage. So, here we are doing pre-charge, here we are doing evaluation, actually, ideally, simultaneously pre-charge and evaluation should take place, but it is not happening, because of the clock skew.

So, let us assume that is the next stage is a very simple circuit, it is an inverter. So, let us assume this is simply an inverter, this is an inverter. So, this is applied from the previous stage, it had come here and this is high, because in the pre-charge phase it will be high or it will be V d d, and this is V d d and this is ground. So, because this is high, because it is be getting pre-charge, this value is coming here, it will come down to, this output will this capacitor will discharge during pre-charge. Now, during evaluation what can happen this goes down to 0, so this becomes 0. So, it it switches to low level.

Now, when it switches to low level you are supposed to get high here during evaluation, but unfortunately during pre-charge itself it was discharged, because during pre-charge the input was high. So, it was discharged, it was discharged to this path, because it was in the evaluation phase. So, what will happen you will get incorrect output at this point here; that means, because of the overlapping of the pre-charge phase with the evaluation phase of the next stage, pre-charge phase of the first stage with the evaluation for the phase of the second stage, you will get, you may get, I am not telling always you will get, but you may get incorrect output. So, this is arising because of the clock skew problem.

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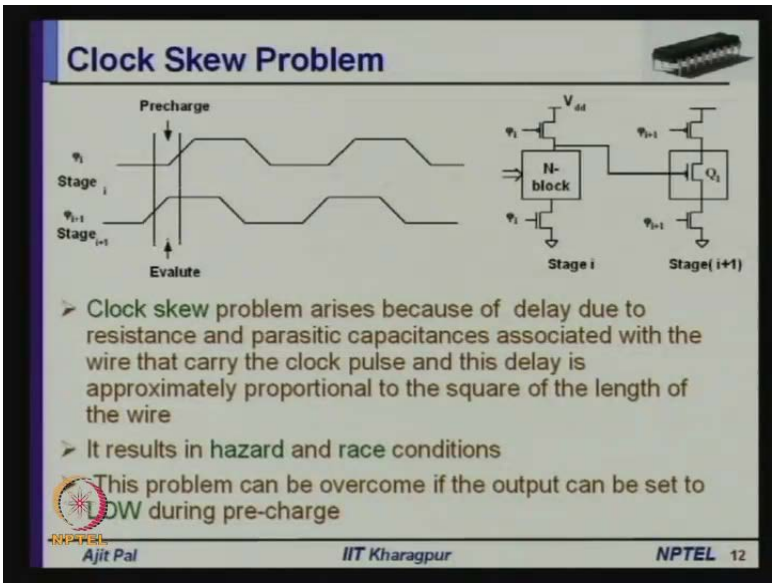

The question naturally arises, this is same thing is shown here. You can see the evaluation is going on for the second stage and this is the pre-charge phase. So, clock skew problem arises, because of delay due to resistance and parasitic capacitances associated with the wire that carry the clock pulse, and this delay is approximately proportional to the square of the length of the wire. It has been found that you know that wire length plays a very important role in deciding the delay, that clock will suffer to reach different points of the circuit. And this clock skew problem may lead to error, and this is typically known as hazard and race conditions, how can it be overcome. This problem can be overcome, if the output can be set to low during pre-charge.

So, this is the clue that can be used to overcome the problem to come up with a solution; that means, what I am suggesting during evaluation, we are holding this output to low high level, instead of that if this output is held to low level then it will not disturb the next stage. So, no not disturb means there cannot be discharge. You know a n-MOS network input, I mean high level transit on, but input is low level it will not disturb, there is no question of the I mean getting the capacitor discharge during pre-charge evaluation phase.

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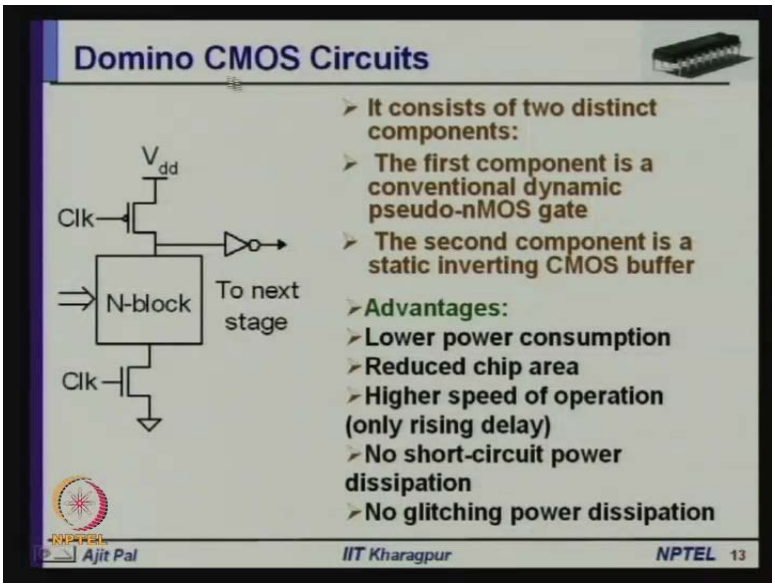

So, that has led to one solution known as domino CMOS circuit, a class of network circuit know as domino CMOS circuit. So, here as you can see, each stage is provided with an inverter at the output. So, you are taking the inverted output to the next stage; that means, during a pre-charge, this output is one, so this output will be low. So, it consists of two distinct components; number one is the first component is a conventional dynamic pseudo n-MOS network, this is this part, and second component is a static CMOS inverter buffer. So, this is the static CMOS inverter buffer. Now, what is the outcome of this, this overcomes the problem of clock skew, how it is overcoming that can be very easily explained.

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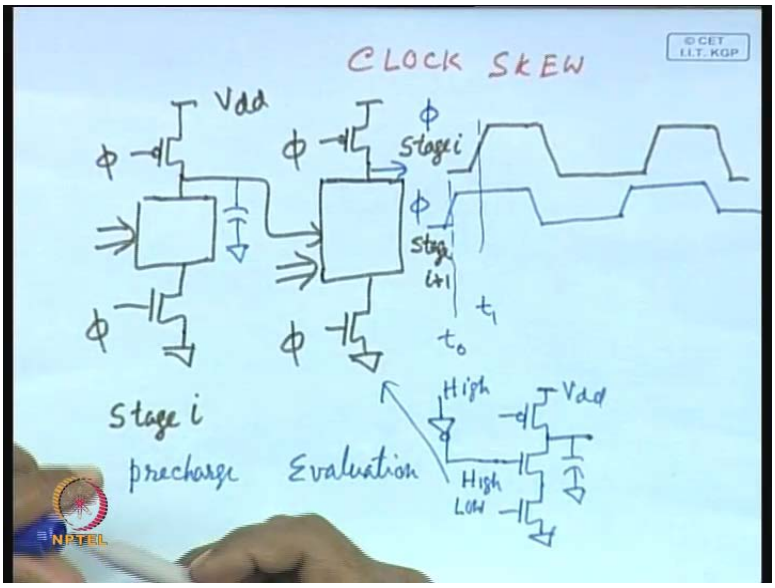

For example, during pre-charge you are applying a inverter here. So, when it is high, then this is low. So, this cannot really discharge and then you can realize the circuit without I mean it will always get correct output irrespective of this delay in irrespective of this clock skew problem so; that means, even if the clock arises late to the first stage, it will not lead to premature discharge of this capacitor during evaluation phase of the stage and pre-charge phase of the previous stage. So, in addition to this there are several advantages of this domino CMOS circuit. This name domino has come, from one resemblance of a real life situation.

Actually in a domino circuit what can happen, if the inputs switches is from one to 0, it may lead to a number of stages, discharging one after the other and following 1 to 0, 1 to 0, 1 to 0, just like falling dominos, this can happen in your bicycle stand, you push one bicycle it leads to falling of another bicycle, it leads to falling of another bicycle it that is the domino effect, that kind of thing can happen in a multistage domino CMOS circuit.

So, that means, that falling to high level to low level that can happen in in your evaluation phase. So, that may lead to a number of stages output may fall from high to low one after the other, like the dominos fall in practical real life. Second is reduced chip area; reduced chip area is essentially the, it has inherited, because it is a dynamic CMOS circuit, because it also uses only one block; N-block or N-block. So, it will require smaller chip area compared to static CMOS, and higher speed of operation I have already

explained and only delay that occurs is rising delay. Rising delay is essentially due to charging during the pre-charge phase, but you know it is controlled by clock. So, clock is decided that way, and there is no short circuit power dissipation as I have already explained, and there is no glitching power dissipation. These two, it has inherited from the basic structure of a dynamic CMOS circuit and these are the advantages of a domino CMOS circuit.

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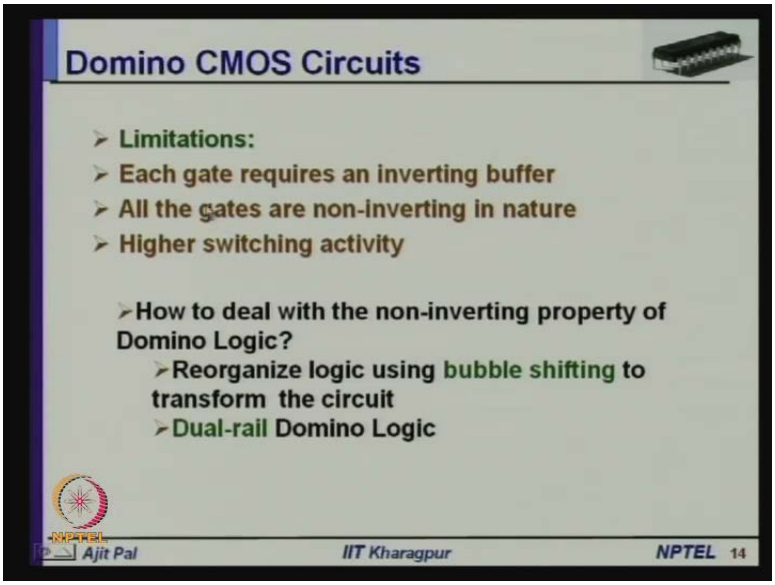

Unfortunately, here also there are some limitations, what are the limitations each gate requires an inverting buffer as we have seen, you have to provide an, you know this is a static CMOS inverter. So, one pMOS and one n-MOS transistors are required, this is an additional requirement. And, all the gates are non-inverting in nature; that means, what is happening, you know the output will become as I mentioned this is a N-block. So, if you consider the output in terms of the input, this output is a negative function, but because of the presence of this inverter this is becoming a positive function, so this is a serious limitation. So, all the gates are non-inverting in nature. In other word its realize a positive unit function; that means, the domino CMOS, each domino CMOS stage can realize only a positive unit function; that means, as you know you cannot really realize any general Boolean function, either using n gate or or gate which are positive unit functions.

So, you can realize any Boolean function by using NOR gate or by using NAND gate, which are negative functions. So, you require some kind of inversion, and this is the limitation, we shall see how it can be overcome, then higher switching activity. It has got higher switching activity, because later on we shall see always during pre-charge phase you are charging it to high, then it may go discharge or not discharge; that means, that output is always switch in each clock to high level. It may switch to low level may not switch. So, this will lead to higher switching activity, higher switching activity means, the dynamic power dissipation will be larger. Later on we shall discuss about it in more detail. So, how do you really overcome the problems associated with domino CMOS, reorganize logic using bubble shifting to transform the circuit. Let me explain what is really meant by bubble shifting.

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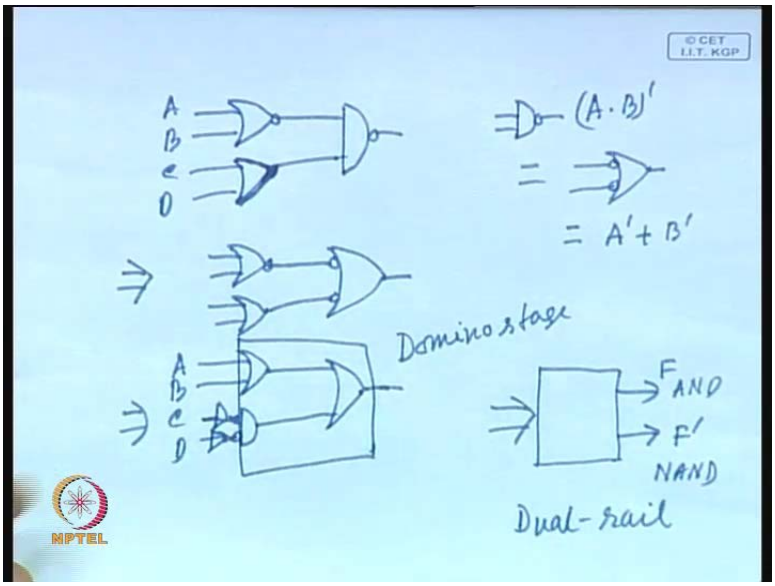

Say suppose, you have a network like this, so let us assume, this is or not NOR, so A B then C D, and this function you have to realize. Obviously, this is not a positive unit function, but this cannot be property of this, say this is equivalent to or and with inverted inputs; that means, this is a NAND gate, NAND gate means A B bar, and this is equal to A bar or B bar; that means, we have applied this bubbles means A bar and here bubble means B bar and this is an or gate. So, this property can be used to shape bubble from the output to the input, so from here to here from here to next stage. So, let us see we can how you can transform it. So, this will get transformed into inverter and two bubbles at the input, this is a NOR gate and you have got. So, after first bubble shifting we get

equivalent circuit. Now, this bubble, this bubble cancels out. So, we get again and this bubble can be again shifted to the input of this.

So, here you will have or, or, and this, this is an NOR gate, so it can be considered as a NAND with two bubbles at the input. So, A B C D and here you get the output; that means, what has been done, this is equivalent to putting an inverter here, putting an inverter here, and this part, this part is now a positive unit function. So, this can be realized by a domino stage, and this can be done by using the bubble shifting property, and we can convert any network having NAND gate, NOR gate inverter in to a positive unit function; that means, in network of NAND or gates. And after that it can be realized by a single domino stage, and of course you have to apply you have to apply the inverter output, that can be done, because inverters in inputs may be available in inverted form, or you will be applying additional static, CMOS static inverter are the primary inputs. So, this is how it can be done.

Second technique that can be used is dual rail domino logic. Normally, what we are doing, we are applying input and producing F, in addition to F you will be also realizing F bar; that means, you are converting a dual rail circuit; that means, basic domino circuit can be modified to realize F as well as F bar simultaneously. Then it will be you know wherever inverter is required will be applying inverter. So, it is no longer realizing only positive unit function, because it is realizing positive unit and its compliment; that means, if it is a AND then this will be NAND output. So, it is essentially a dual rail logic dual rail implementation. Later on again I shall discuss about it in more detail, this is how the dual rail logic can be realized, domino CMOS.

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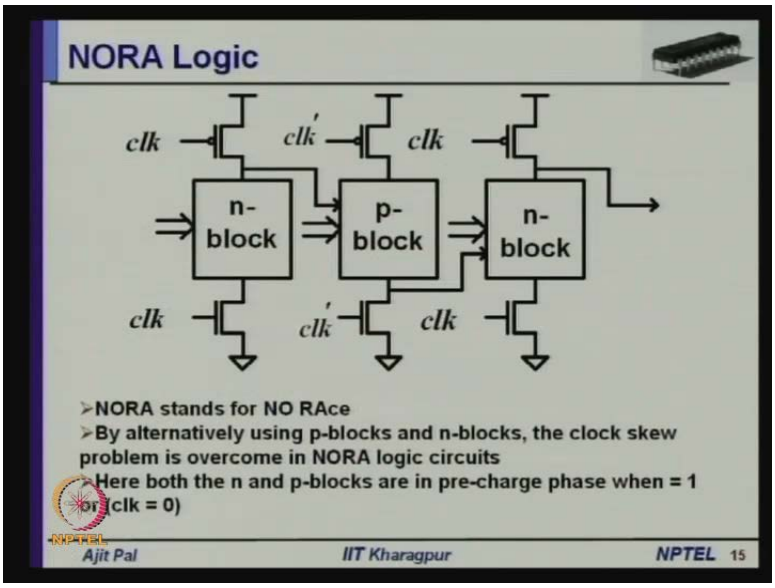

Now, there is another way of overcoming this problem by using NORA logic, what you do in NORA logic. We are using a n-MOS block followed by a pMOS block. So, what we are doing here, earlier we have seen that the, when during pre-charge the previous stage is disturbing the next stage if it is in the evaluation phase. Now, if it is a pMOS transistor, then a high level output will not disturb it. So, what we are doing, we are using alternatively a n-MOS block followed by pMOS block, followed by n-MOS block and. So, on; that means, you are realizing multi-level circuits, but we are not using only n-MOS block in the realization we have already discussed about it, that we can use both pMOS and n-MOS block in the realization.

So, n-MOS followed by p-block followed by n-block. This will not disturb it, because whenever this is high and this is in even it is in the evaluation phase, as you know now high level input to a pMOS transistor does not turn it on, and as a consequence the it will not affect the the next stage. So, this is known as NORA logic, where from the NORA has come, name NORA has come. NORA is the name is not the name of any person, actually it has come from no race; no race, NORA. So, these two have been added no race, as we know normally whenever you have multi-level circuits, because of clock skew problem res condition arises, leading to different kinds of problems, including malfunctioning inaccurate output and, so on that problem is overcome by using this logic. So, NORA stands for no race.

By alternately using p-blocks and n-blocks, the clock skew problem is overcome in NORA logic circuits. Here, both the n and p blocks are in pre-charge phase, when one clock is one or clock is zero. So, you can see we are applied, you know here you are applying clock and here we are applying clock bar; that means, both the stages are in the pre-charge phase simultaneously, and evaluation phase simultaneously, and as a consequence you can realize circuits in this manner. In fact, this type of configuration can be used to realize pipeline circuits, pipeline implementation of different stages, alternatively alternately using n-MOS block followed by pMOS block followed by n-MOS block and, so on. So, this technique can be used to realize pipe lined multi-level circuits.

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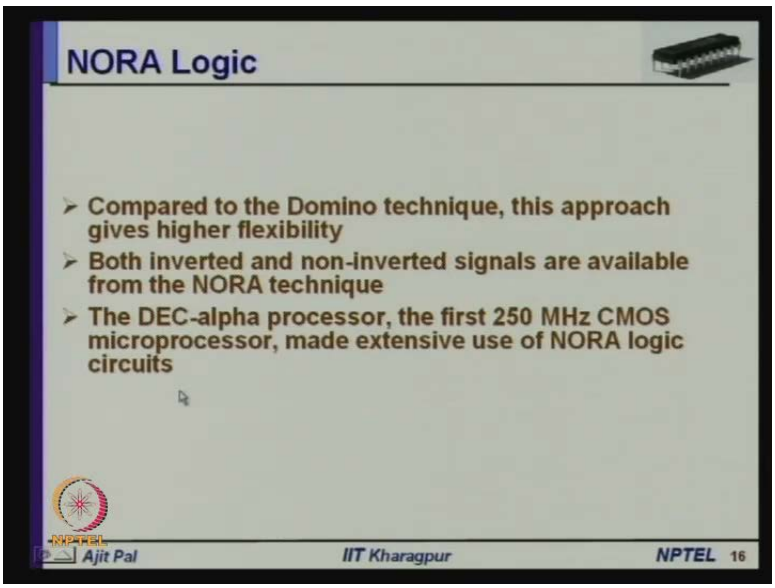

Let us not going to the details of that, but let me illustrate this u, it with the help of an example, but before we illustrate with the help of an example, here is some comparison compared to domino technique this approach gives higher flexibility, both inverted and non-inverted signals are available from the NORA technique. Actually what you can do, you can apply an inverter here and if this stage has to drive a n-MOS block, you can put an inverter here. Similarly, if this stage has to drive a another stage which is p-block, you can put an inverter here.

So, in this way it gives you more flexibility, and particularly this DEC alpha processor, the first two-fifty megahertz CMOS microprocessor made extensive use of NORA logic

circuits. I mentioned about it earlier you know that DEC alpha was the fastest processor at one point of time, and they implemented this with the help of extensive use of NORA logics in their circuits, in their implementation, particularly about thirty percent of the logic circuits were realized by using dynamic NORA logic, remaining of course, by using static CMOS.

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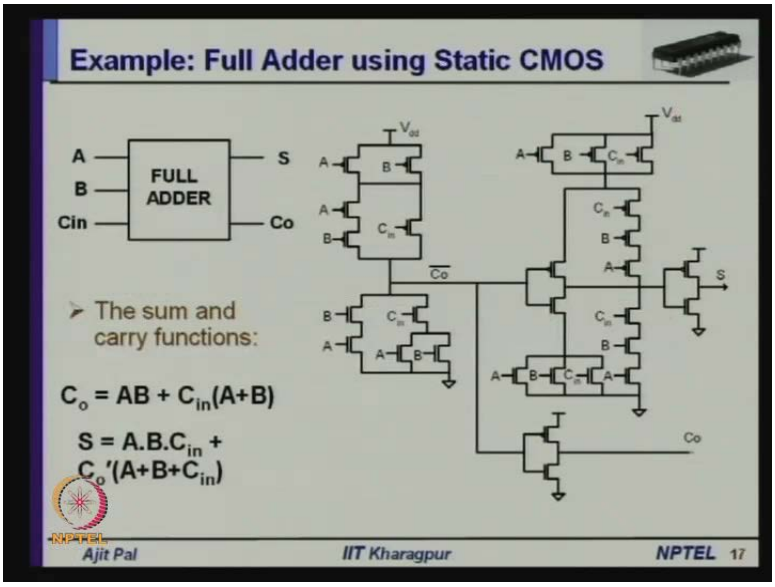

Let us now come to an example, this is that full adder using static CMOS I discussed in my last lecture, as you know a single full adder cell can be realized by using static CMOS approach, and as you know this requires both n-MOS network pMOS network for both realizing the carry as well as some functions, and the total number of transistors that is required in this particular cases 28, as we know.

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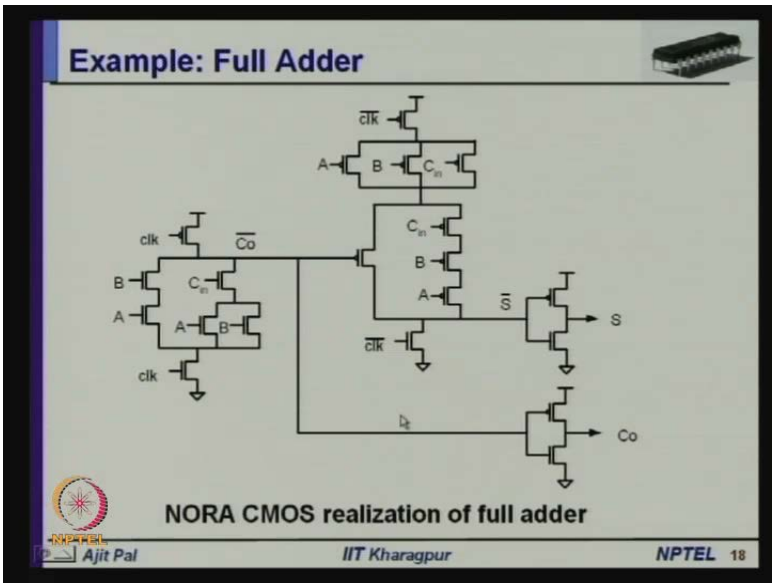

Now, let us see how we can convert it in to a NORA logic circuit. It can be very easily transformed in to NORA logic, only thing that you have to do, you have to remove the pMOS n-MOS network this pMOS network is removed. So, first stage is realized by using only a n-MOS network and with one pMOS header and n-MOS footer, as it is shown here, pMOS header n-MOS footer and the n-MOS network. So, instead of 10 transistors now you require uh seven transistors, so three transistors less. Moreover, you can see your output is going to only pMOS only one input not p and n and that also reduces the capacitance. Again, the next stage is realized by removing the n-MOS network, because we are realizing a NORA circuit.

So, this n-MOS network is removed and it is realized by using pMOS network, and so this is the NORA stage and I mean NORA logic circuit, where n-MOS followed by pMOS network is used for realizing the next stage, and here as you can see output is taken from here, and of course you will require two inverters, like the previous case two inverters are there, static CMOS inverter to drive the next stage and that is how you realize the NORA CMOS realization of full adder.

So, what is the total number of transistors here, instead of 28, here you have got 7 plus 1 2 3 4 5 6 7 8 9, here 9, 9 plus 7 and then of course, 16 plus 2 plus 2, 20. So, you have got 20 transistors instead of 28, but in not only there is reduction in the number of transistors. Also you know the each stage is driving one transistor instead of two. There

is no need to drive both pMOS and n-MOS transistor as it is necessary in case of this, as we can see you are driving each output is driving a pMOS and a n-MOS, but here you have to drive only a pMOS, and if it is coming from the the previous stage will drive only the n-MOS. So, there also there is significant reduction in capacitance and as a result, this is pretty fast as I mentioned it will be about fourth times faster than the static CMOS implementation.

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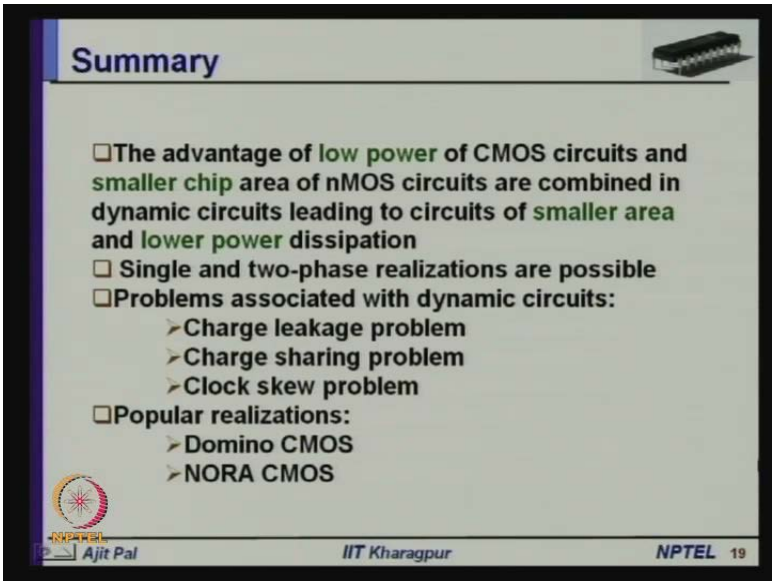

So, we can summarize what we have discussed so far. The advantage of low power of CMOS circuits and smaller chip area of n-MOS circuits are combined in dynamic CMOS circuits, leading to smaller area and lower power dissipation. And we have also discussed single and two phase realizations of dynamic CMOS circuits. And, we have discussed various advantages and also the disadvantages in this lecture, the charge leakage problem, charge sharing problem, and clock skew problem and we have discussed how these problems can be overcome. Finally, we have discussed about two popular implementations domino CMOS and NORA CMOS, which are used in realizing dynamic CMOS circuits.

So, with this we have come to the end of today's lecture, and in the next lecture we shall discuss about how circuits can be realized by using switched logics, not gate logic you know, so far we have discussed about gate logic, static CMOS as well as dynamic CMOS, where you are applying your input to the gate, taking output from source or

drain. And we have already discussed about the use of transistor as a switch, and in the next class we shall discuss about how that concept can be extended to realize combination on circuits by using switched logic, essentially those are known as pass transistor logic. Thank you