Low Power VLSI Circuits and Systems

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Lecture No #10

Static CMOS Circuits – I

Hello and welcome to today's lecture on static CMOS circuits; this is the first lecture on this topic. And in two lectures, I shall cover different aspects of static CMOS circuits. In the last four lectures, I have discussed about various aspects of MOS inverters, how different types of inverters can be realized, their characteristics, static, dynamic and so on. And as I mentioned earlier, you are following bottom of approach. So, starting with MOS transistor we have discussed MOS inverters, now we are discussing more complex circuits realized using static CMOS circuits, static CMOS technology.

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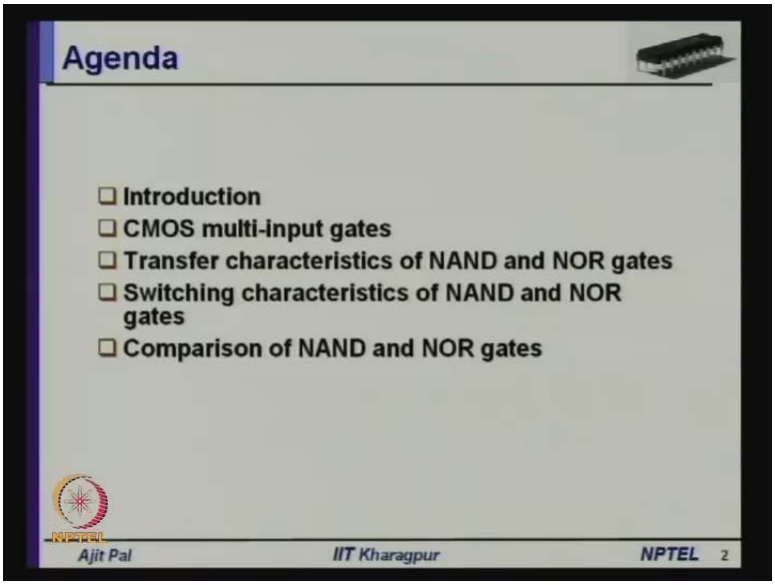

Here is the agenda after every introduction, which will also include some recap of the previous lectures. I shall discuss about CMOS multi-input gates; we shall see how multi-input gates can be realized by extending the idea of MOS inverters. Then we shall discuss transfer characteristics of NAND and NOR gates, and after that we shall discuss

switching characteristics of NAND and NOR gates. And finally, we shall compare the characteristics of NAND and NOR gates realized using static CMOS technology.

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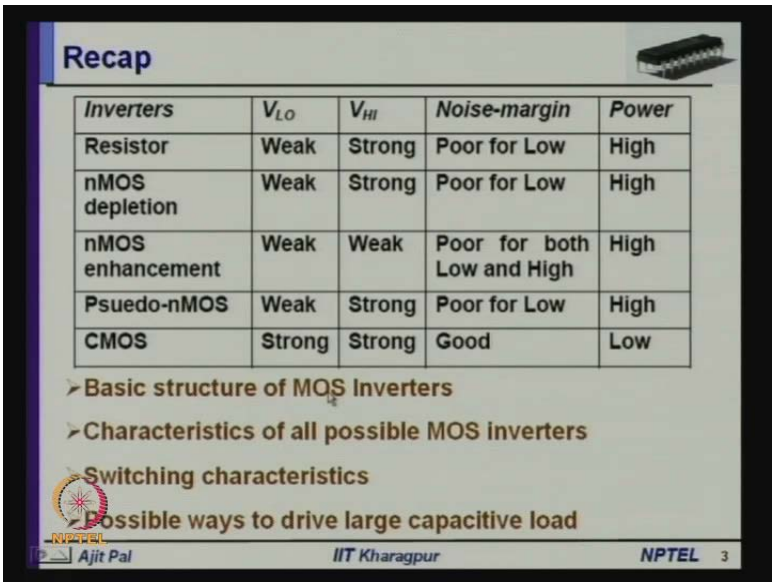

Here is a brief recap about what we discussed in my last four lectures, we have discussed about different types of inverters, that can be realized by using MOS technology we have seen pull-down device is always in MOS transistor, but pull-up device can vary it can be a passive resistor, or it can be some active devices particularly nMOS depletion transistor nMOS enhancement transistor pseudo-n MOS circuit, where a pMOS transistor is used as pull-up and also in CMOS a pMOS transistor is used as pull-up. And we have seen except for CMOS where the low level is strong for all the other cases we have seen the low level is weak and as a consequence the noise margin will be poorer; that means, the noise margin a low in m L will be weak poor for all these inverter configurations.

On the other hand we find that only for nMOS enhancement transistor the high level is weak for all other cases high level is strong. So, noise margin for nMOS enhancement type pull-up device is inferior, and as a consequence nMOS enhancement type transistor is never used in realizing inverters and other types of circuits. So, but we find that in terms of all these features noise margin it is good for CMOS power dissipation is also low, and and also the low and high levels are strong. As a consequence the CMOS is the choice of present day VLSI circuits and that is a technology that is used for realizing

present day MOS circuits VLSI circuits. So, henceforth we shall continue our discussion primarily on CMOS

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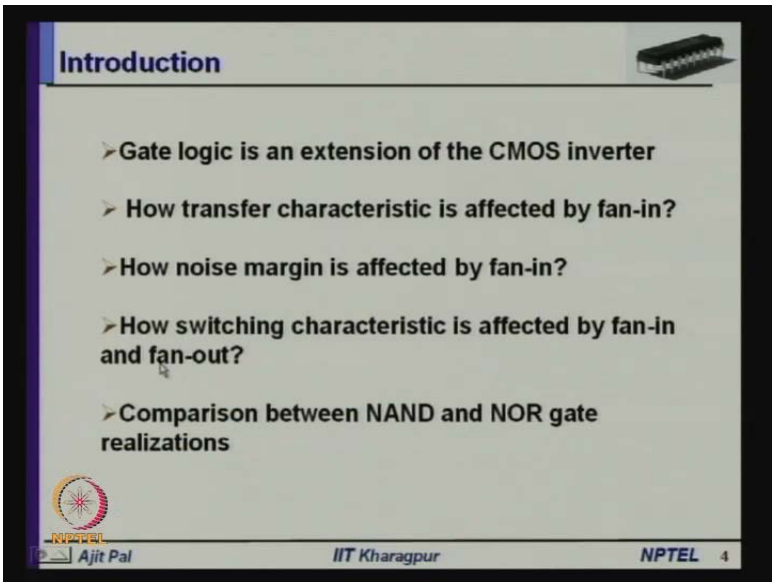

And we shall see in this lecture, how different types of gates particularly NAND and NOR gates can be realized by extending the basic concept of CMOS inverter, and we shall see; that means, whenever we are making it NAND or NOR gate essentially we are increasing fan-in I shall elaborate about it what is fan-in and how the transfer characteristic is affected by fan-in that we shall discuss in detail. Then I shall also see we shall also discuss about the impact of fan-in on the noise margin, because fan-in affects the noise margin that we shall see. Then how switching characteristic is affected by fan-in and fan-out that also, we shall discuss finally, we shall end our lecture by comparing NAND and NOR gate realizations their compare that various characteristics.

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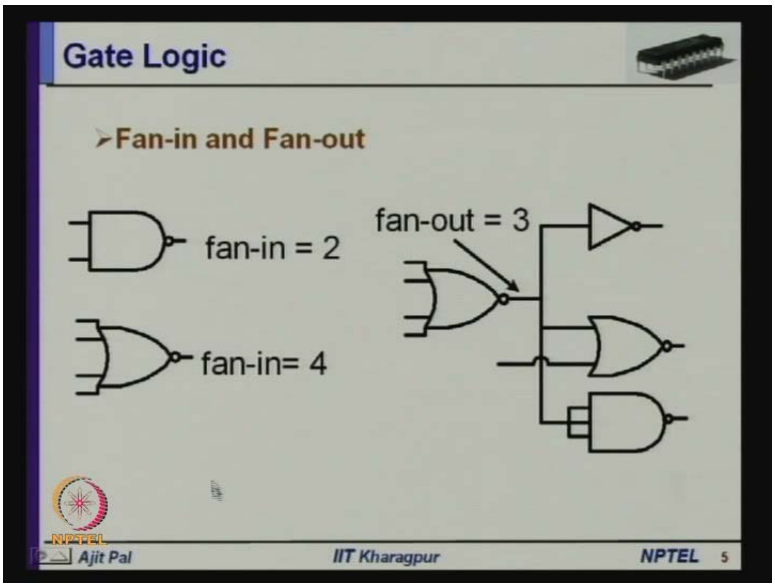

First let us focus on fan-in and fan-out. So, let us consider what is fan-in fan-in fan is essentially the number of number of inputs.

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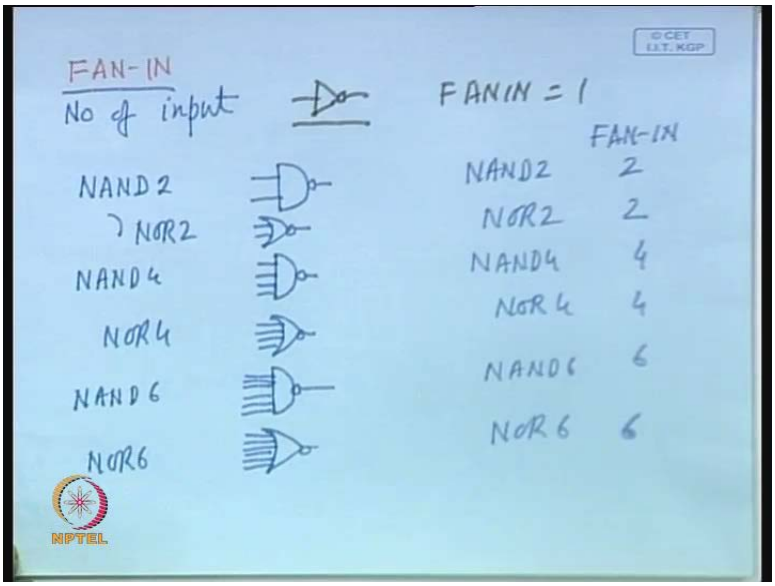

That can be applied to a gate without affecting its operation; that means, it should behave like a gate switching device you know that is. So, produce high level output low level output and the fan is essentially is number of inputs. So, let us consider different types of gates first let us consider NAND gate. NAND gate NAND 2 where we have got two inputs. So, here fan-in is two. So, NAND two fan-in is two then we can have four input

NAND gate NAND four where the number of inputs is 1, 2, 3, 4 and you can have NAND 4 fan-in is equal to 4 you can also have say NAND 6 where the number of inputs is 6, 1, 2, 3, 4, 5 and 6. So, here for NAND 6 fan-in is 6. So, see we can fan-in is essentially the number of inputs similarly, we can have NOR gates 2 input NOR gate NOR 2 NOR 2 again will have fan-in of 2 NOR 4 will have fan-in of 4 4 input NOR gate will have fan-in of 4 similarly, you can have say NOR 6, 1, 2, 3, 4, 5, 6. So, NOR 6 and NOR 6 will have fan-in of 6.

So, not only NAND and NOR gates are used other types of gates are also there for example, and gate or gate excusive or gate. So, these gates are also used and which are considered to be part of the standard say library, but we are discussing the characteristics of NAND and NOR gates primarily, because it is very natural to realize NAND and NOR gates by using MOS technology. The other gates can be realized using NAND and NOR gates later on we shall discuss about that. So, here is the concept of fan-in. Now let us consider the concept of fan-out what do you really mean by fan-out.

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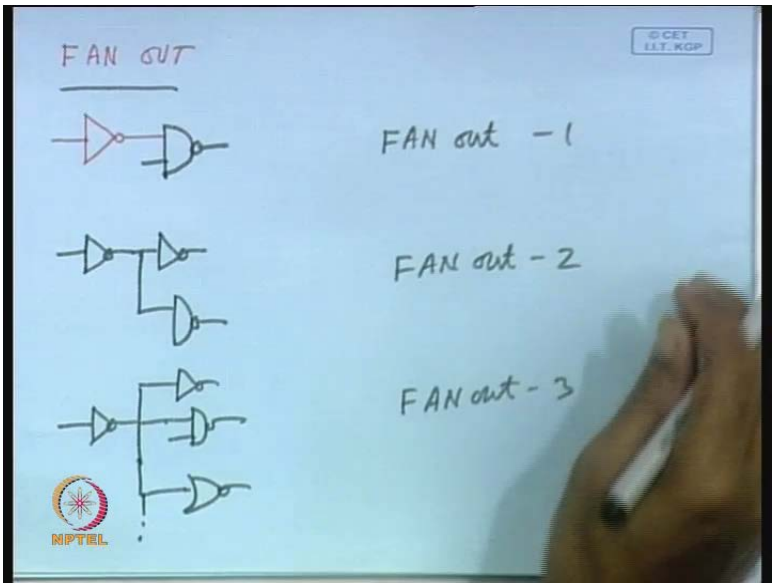

So, fan-out fan-out is essentially the number of gates the a particular gate is driving for example, this inverter may be driving several gate say it can drive only one gate it is going to one input of a NOR gate. So, in this case fan-out is equal to is one or it can drive more than one gate say, it is driving an inverter as well as it is driving one NAND gate. So, in this case the fan-out is equal to 2 similarly, it can drive a several gates for

example, an inverter a NAND gate or it can drive it a NOR gate and different types of gates. So, fan-out in general fan-out in this particular case 1, 2, 3. So, fan-out is equal to three. So, if it goes to other more number of gates fan-out will be more. So, whenever we add more and more gates at the output where particular gate, we have to see that performance of the circuit is not degraded and also the correct correct output is produced. So that that will be our study how fan-in and fan-out affects a particular circuit. For example, when we are extending the basic concept of inverter and inverter can be considered as a fan-out fan-in having fan-in is equal to 1. So, inverter is essentially a gate having fan-in is equal to 1, but other types of gates with 2 input 3 or 4 input have fan fan-in of more than 1. And how whenever you add more number of inputs, how the circuit behavior is changing that we shall discus in terms of transfer characteristics switching characteristics noise margin and so on.

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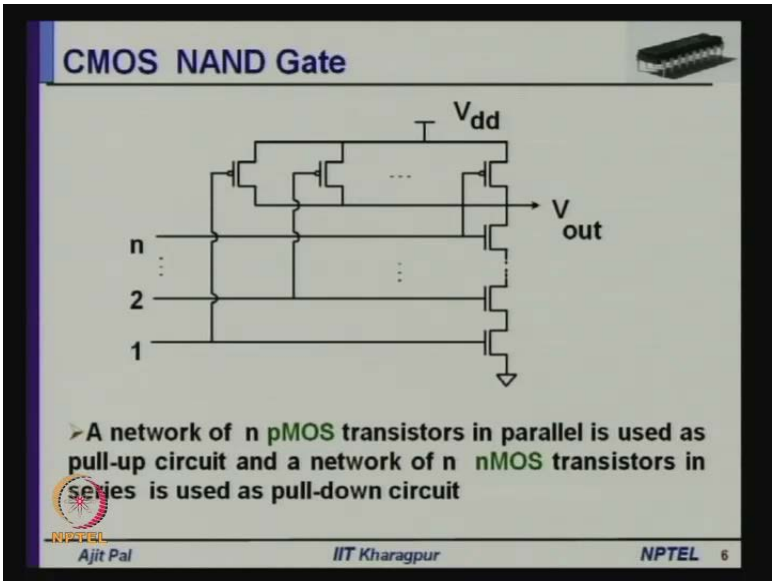

So, after discussing fan-in and fan-out let us consider a basic realization of a NOR gate or NAND gate let us start with NAND gate NAND gate.

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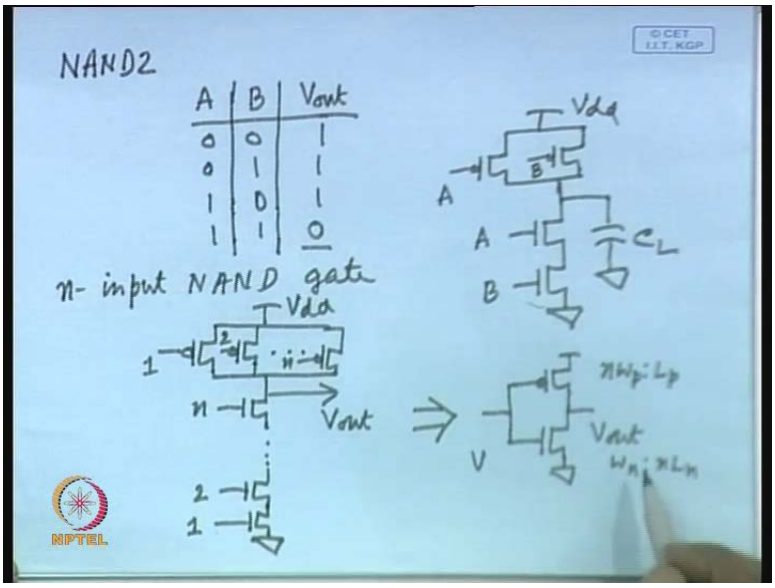

So, a NAND function let us consider two input NAND function NAND 2. So, it has got let us assume 2 inputs A and B and it produces say output V or we can say V is produces V out. As you know it for 2 inputs there are four possible combinations, that you can apply to the gate 10 0 0 1 1 0 1 1 and sorry in this case the output for NAND gate will be whenever both of them are one only then it is 0 for all other cases it is one this is how it can be realized. Now how you can realize a NAND 2 gate NAND 2 gates can be very easily realized by having 2 nMOS transistors in series. And connecting it to ground, because you know as we know the role of the nMOS transistors nMOS transistor network is to pull down the output to low level and when in this particular case is pulling down when both of them are 1, as you can see when both of them are 1 this C L can be pulled down.

Now what is the role of the pMOS transistor is to produce 1; that means, role of nMOS network is to produce 0 and the role of the pMOS network is to produce 1. So, you can see here the 1 is produced when any of the input is 0. So, that can be realized by having two pMOS transistor in parallel. So, whenever any of them is 0 as per this then this Vdd will be connected to this I mean, apply to this load resistance and it will be charged to high level. So, it will become 1. So, this is how you can realize a 2 input NAND gate and in this way you can extend this concept to realize say n-input NAND gate. So, an n-input NAND gate will have n pMOS transistors n pMOS transistors in parallel and nMOS transistors in series we can see here. So, this is connected to ground this is connected to

Vdd. So, you can say this is input 1, this is input 2, this is input n similarly, this is input 1 this is input 2 this is input n and output is taken from here V out. So, this is the general structure of a n-input NAND gate where we have got n pMOS transistors in parallel connected to Vdd and nMOS transistors in series which are which is connected to ground. So, this is how you can realize a n-input NAND gate.

And similarly, you can have n-input NOR gate realization. So, you can also realize n-input NAND gate, but NOR gate, but before we do that we shall study the characteristics the characteristics of this n-input NAND gate; that means, whenever you add more than one input; that means, whenever it is become multi-input means, input is 2, 3, 4 then how the transfer characteristic is affected that we shall discuss. So, here as you can see there are n transistors in parallel here n transistors in series. Now, this can be simplified you can consider it. As if all the n pMOS transistors are tied together gates are tied together and it is represented by single pMOS transistor similarly, all the gates are of the nMOS transistors are tied together, and it is represented by a single nMOS transistor. And then you have connected it to V in and here it produces V out. How the L by W ratio is affected I mean, is changed whenever you convert it into a single inverter by tying all the inputs together; that means, 1 to n all are tied together and then it behaves as if it is an inverter. So, in that case we shall see how the transfer characteristic is affected

So, here as you can see since n pMOS transistors in parallel, as if n resistors are in parallel. So, there or you can say that the you know that W their widths are tied are parallel. And So, the W by L ratio will be n W p and L p similarly, L by W ratio of this particular transistor will be equal to that W n will not change, but the length will change, because you can see these are in series as if you have connected n series n transistors in series. So, they are lengths are tied together to form n L n they are in series. So, L by W w by L ratio for this particular inverter which are essentially realized by tying all the inputs together we get this.

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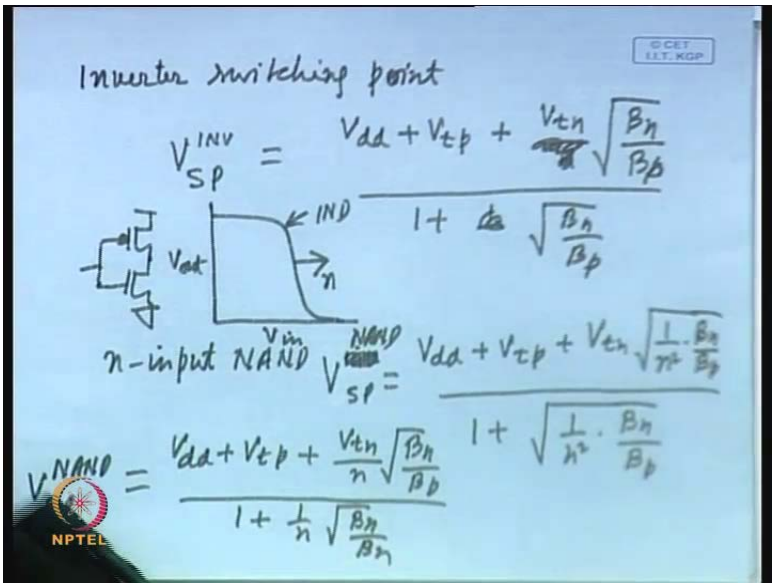

Now, what is the expression for that switching point inverter switching point? We know that inverter switching point or inverter threshold voltage in that particular case, what is the expression for that V s p switching point of inverter. We know that that expression is Vdd plus V t p where V t p is the threshold voltage of the pMOS transistor, plus V t n by n root beta n by beta p by 1 plus 1 by sorry in particular for inverter this n will not be there. So, it will be one plus root beta n by beta p. So, we find this is the case of an for simple inverter where you have got only 1 nMOS transistor, pMOS transistor and 1 nMOS transistor, but in this case in case of n-input NAND gate we have connected n transistors in parallel for the pMOS network, and n transistors in series how they are beta n by beta p is affected. You have already seen they are the ratio will be affected in this way n W p L p width of the pMOS transistor is increased, and length of the nMOS transistor is increased.

So, this if we substitute then for a the switching point V inverter switching point will be equal to Vdd plus V t p this part is not affected, but beta n by beta p sorry beta n by it will be beta p beta n by beta p that ratio is affected. And since the length of the this W by L in this particular case, it is in the L that L is increased and here, W is increased W p is increased. And as a consequence it will be equal to V t n root 1 by n square beta n and beta p that corresponds to an inverter. Similarly, here it will be 1 plus root 1 by n square into beta n by beta p. So, if we simplify this will be equal to Vdd plus V t p plus V t n by

n root beta n by beta p and at the denominator it will have 1 plus 1 by n root beta n by beta p.

Now, if we plot this is this is this is not this is the case not for inverter for NAND gate for n-input NAND gate. So, this is V SP NAND that was the case for inverter how it is affected. So, if the switching point of an if we consider the switching point of an inverter in what direction it will go. So, let me plot the transfer characteristic here. So, this is the transfer characteristic let us assume this is your V out and this is V in and let us assume this is the transfer characteristic for inverter. And here as you can see this value as n increases in the denominator this is 1 by n beta n by beta p into 1 by n. So, value of the denominator will increase, and as a consequence this will move in this direction. So, for higher n as increases the switching point will move towards right towards Vdd. So, later on we should see how much it is increased for different values of n, but for the time being we can say that for a NAND gate, this switching point moves toward Vdd. Whatever is the inversion inverter switching point from that that NAND switching point NAND gate switching point will move towards.

So, this will indeed affect the noise margin, because ideally it should be at Vdd by 2, but if it moves towards right then the noise margin of high level will degrade, and if it moves in the left direction then noise margin of the low level noise margin will be affected, but for the time being we find that for NAND gate n as n is input the inversion point moves towards right and as a consequence the noise margin will be affected

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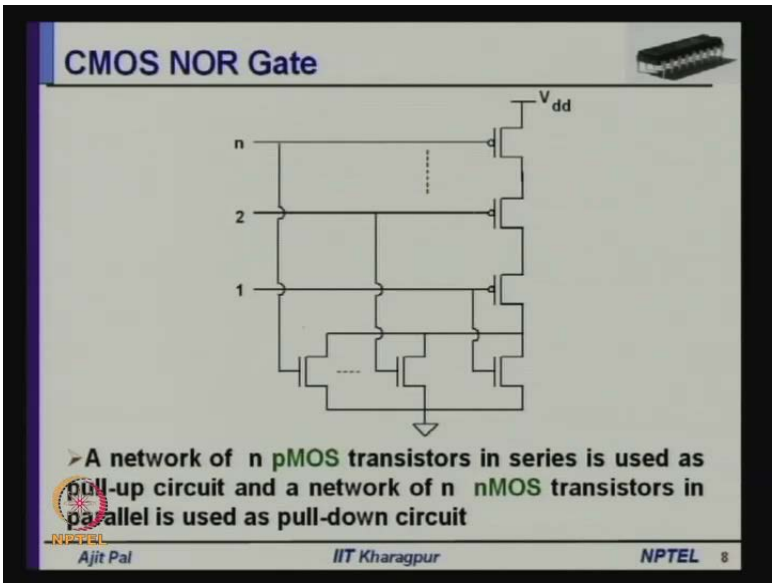

Now, let us consider a NOR gate in a similar manner. So, a NOR gate what is the realization by extending the same concept of NAND gate a NOR gate as you know if we real show the function if we it has got 2 inputs.

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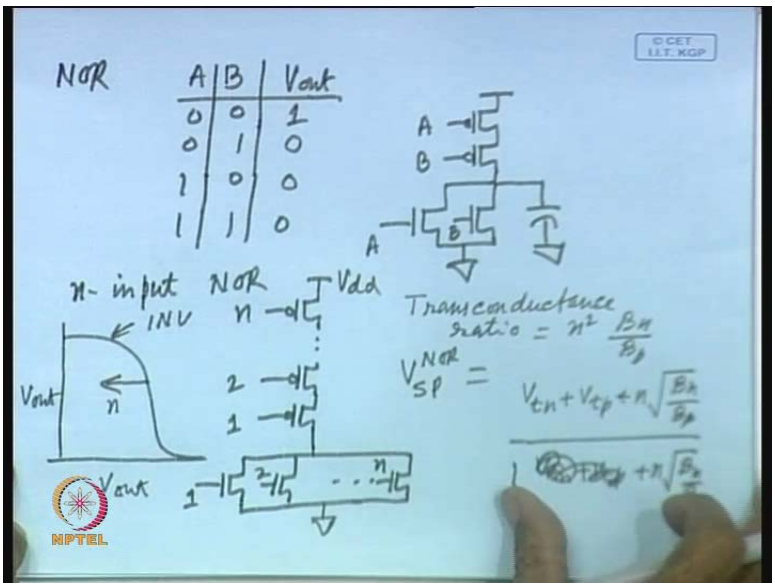

So, 0 0 0 1 1 0 and 1 1 and V out for NOR gate when it will be 1 it will be 1 for as you know for or gate the for these three output is 1. So, in this case this will be 0 and only for 0 0 outputs will be 1 that will be the case for NOR gate. So, how that can be realized? So, when both of them are 0 then output is 1 so that means, what you have to do we have

to put 2 2 pMOS transistor in series. So, when both of them are 0 then this path is closed. So, we shall get one at the output and what about the NAND gate network as you can see when when any of them any any of the input is 1 then output is 0. So, that can be very easily implemented by having 2 nMOS transistors in parallel and connecting the source of them to ground. So, this is here it is a, and here it is b. So, this is how a 2 input NOR gate can be realized and the idea can be extended to realize a n-input NOR gate.

So, an n-input NOR gate will be having n pMOS transistor in series. So, 1 2 n and nMOS transistor in parallel in this case. So, 1 2 n, so n nMOS transistors in parallel and the source the common this all the resource points will be connected to the ground and the that series connected pMOS transistor is connected to Vdd this is how a n-input NOR gate is realized.

Now, in this particular case what is the value of this V switching point NOR for n-input NOR gate. In this particular case we find that this the value of the trans conductance ratio that beta n by beta p is equal to that trans conductance ratio trans conductance ratio is equal to n square beta n by beta p, because in this particular case as if n MOS pMOS transistors in series; that means, there width will be in series; that means, their length will increase for the pMOS transistor and width of the nMOS transistor will increase, and that is the reason why it is n square beta n by beta p. So, the V switching point for the inverter will be equal to V t n plus V t p this part remaining same here, it will be n root beta n by beta p. And in the denominator it will have V t n plus V t p plus n root sorry it will be 1 plus n root beta n by beta p. So, if you plot this what you find that the denominator value since n is here as n increases the denominator value increases.

So, for an inverter if the transfer characteristic is somewhat like this, this neither is for an inverter for NOR gate it will move towards left, because in the denominator value is increasing and this part is actually will be smaller than this. So, it will move towards as n increases, the inverter inverter switching point will move towards left.

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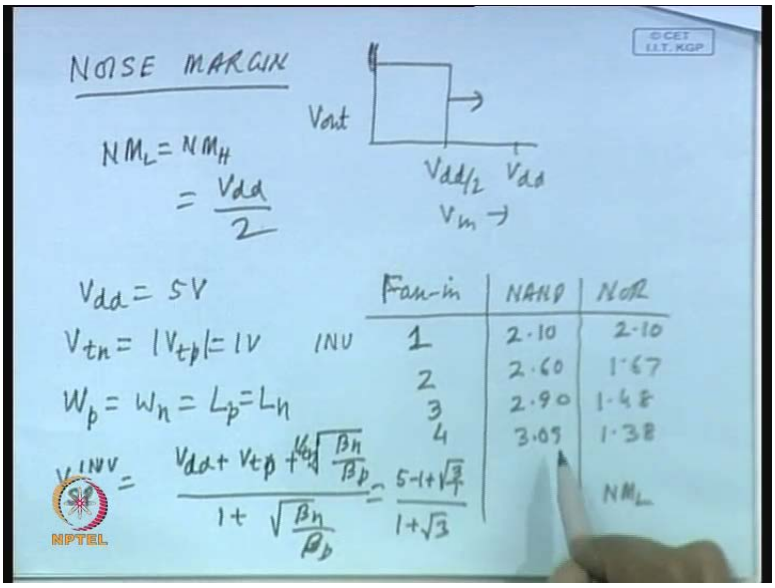

Now, let us consider the noise margin of the for the 2 cases noise margin. How noise margin is affected as we know ideally the transfer characteristic should be like this, the switching point is at Vdd by 2 and this is Vdd and this is your V out, earlier by wrongly I have written V out it V in. So, V in again as V v output plot is done and the if the if the switching is done in the middle then noise margin noise margin low will be equal to noise margin high is equal to Vdd by 2, but if it moves towards right then the noise margin high will decrease, if it moves if the switching point moves towards left then the noise margin low will decrease. Now let us plot the let us find out the value of the switching point for different values of n and other parameters.

Let us assume Vdd is equal to 5 volt then V t n is equal to absolute value of V t p is equal to 1 volt, because V t p will be is equal to minus 1. So, you have taken the absolute value and also let's assume W p is equal to W n is equal to, L p is equal to L n. So, here we are assuming the width and length all are same in such a case for fan-in fan-in is equal to 1 that is the case of inverter; that means, this is a case of an inverter. What is the switching point the switching point will be equal to 2.10 volt 2.10 volt for the inverter switching point. So, how you are getting it actually V switching point inverter as you know is equal to V Vdd plus V t p plus root of beta n by beta p into V t n by 1 plus root beta n by beta p.

So, in this particular case what will happen this V t p Vdd is 5 V t p is 1. So, V t Vdd minus it means, that will be 1 this will be equal to 5 minus 1 plus 1 plus root beta n by beta p will be equal to 3 by 1. And similarly, this will be also equal to 1 plus root 3. So, if you simplify it you will get 2.10. Now, so whenever we are concerning inverter there is no difference between NAND gate and NOR gate these are essentially same. Now let us consider fan-in of two in that case for NAND gate as we know it will move towards right for NOR gate for NAND gate, and for NOR gate it will move towards left. So, this becomes 2.60 volt it is moving towards right it is increasing on the other hand it will be not 1.67 for NOR gate.

So, we can see it is decreasing this is increasing for 3 input NAND and NOR gate the corresponding values are 2.90 and 1.48 and for 4 input the value will be 3.09 and 1.38. So, what we are observing is that since it is starting with lower value then the midpoint by increasing it is becoming closer to the midpoint then of course, it is increasing, but noise margin is definitely better for NAND gate than NOR gate, because in this particular case we see, the low that n m L noise margin low is very bad I mean, instead of 2.5 it is 1.38, but here it is not that much affected it is affected definitely, but you can see whenever the fan-in is 2 or 3 then it is very close to the middle there is small difference. So, noise margin low noise margin low or high is not affected much. So, in other words the noise margin of a NAND gate, is less affected than the noise margin of a NOR gate whenever you increase the fan-in.

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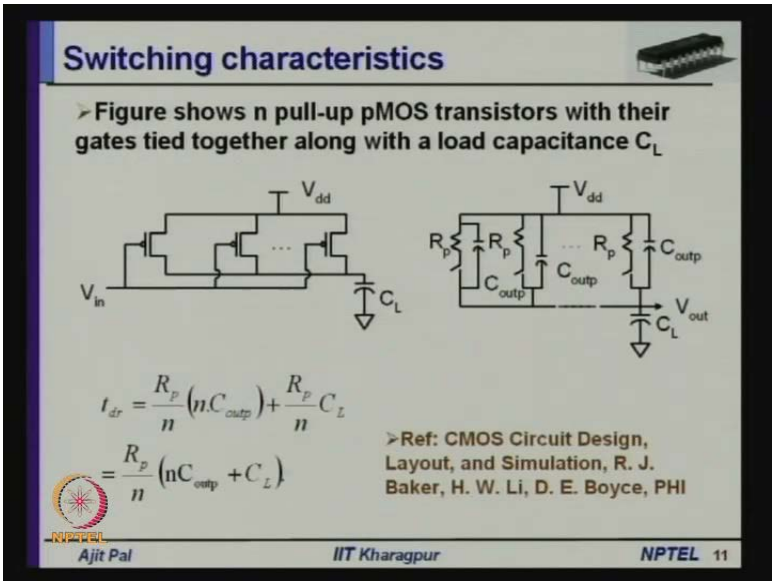

So, with this conclusion in mind let us now move to discuss about the switching characteristics. So, whenever we consider the switching characteristics, the figure shows n pull-up pMOS transistors with their gates tied together along with a load capacitance C l. So, for the sake sake of simplicity what we have assume, as if all the NOR gates are tied together pMOS transistors are tied together, that is the difficult NAND configuration and this is connected to C L.

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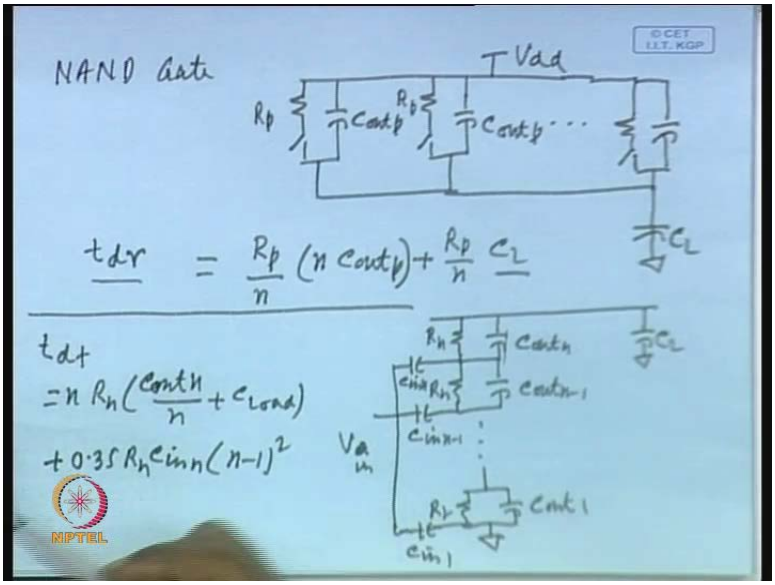

So, in this particular case the equivalent circuit for NAND gate will be pMOS network for NAND gate n-input NAND gate will be as if R P and there is a switch and a capacitor that is your C out p and we can have we have such n such transistors. So, R P a switch representing the transistor depending on or off this will be closed or not closed, and again you have got C out p these are tied together. And in this way there will be n such resistors and capacitors which are in parallel and for then. So, far as the resistance is concerned they are in series with the resistor I mean, a switch is there in series and capacitor is connected and this is connected to the load capacitance C L. So, considering this, the t d r rise time time delay rise time will be equal to it can be derived R n R P this is your R P recharging through R P this is connected to Vdd. So, it will charge through r p. So, rise time will be dependent on R P C output.

So, it can be derived that is equal to R P by n into n C out p plus R P by n C L. So, we find that has got 2 components, the first component is essentially for charging different

output capacitances. And this the second term is essentially to charge the load capacitance. And this particular verification you will find in this reference CMOS circuit design layout and simulation by baker and Boyce published by prentice-hall of India. So, this is the case for charging the capacitor. So, t d r what about the t d f fault time; so to do that what we can say that as if n transistors are in series. So, we can say that this is your load connected then we have got n transistors in series. So, and gate is the input is connected here, and another transistor again input is connected here. So, in this way you have got n pMOS nMOS transistors in series. So, representing R n r n these capacitors are C out n C out n C out n minus 1 and finally, you will be having another resistor and capacitor C out 1 R n and a capacitor connected here this is connected to ground. So, these inputs are tied together and here you are applying V in and this is your load capacitance.

So, the discharging take place through this path and input is applied through these capacitances. As you know you are applying it to the gate, and that is being represented by C in n minus 1 and this is C in n and this is C in 1. So, it is applied to the gate and these are the capacitances of the gate which is represented and these are the output capacitances. And the expression for t d f t d f will be equal to, n R n C out n by n plus C load these are essentially to charge the load capacitance, and the output capacitances which are in series since they are in series they that is the capacitance value equivalent capacitance is C out n by n. And another term will be there that is for charging these input capacitances. So, this this value is 0.35 R n C in n and n minus 1 square. So, these are this is the expression again this has been taken from this reference CMOS circuit design. So, the rise time and fall time can be represented by these expressions.

Now, when the value of C L is large then other factors can be neglected. So, t d r will become equal to this part R P by n into C L. And of course, in the worst case when only 1 transistor is on remaining transistors is off this will be equal to R P into C L similarly, the t d f will be will be equal to n R n C load the other factors can be neglected when n is very large.

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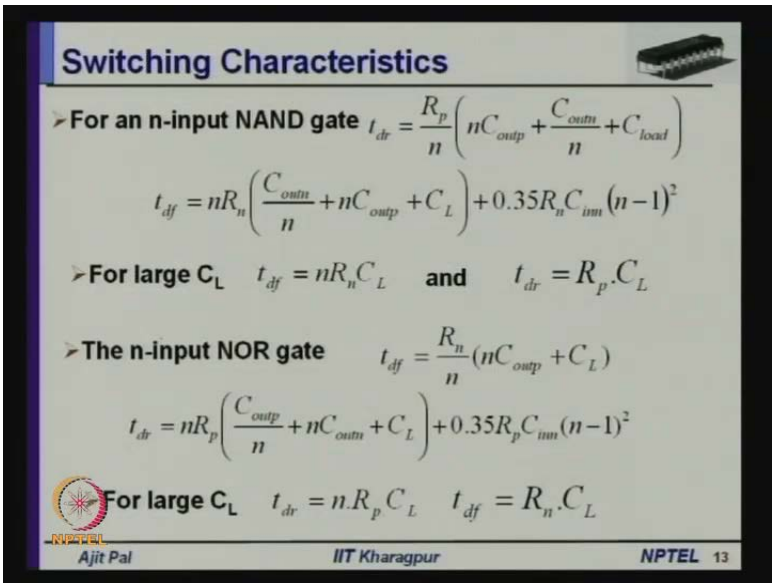

Now, let us focus on the NOR gate in a similar, way we can derive expressions for NOR gate. And this is the summary of the switching characteristics of the NAND and NOR gates. So, t d r for NAND gate is equal to R P by n into n C out p plus C out n by n plus C load. So, here not only output capacitance I mean, for the pMOS transistors output capacitance of the nMOS transistor has also been taken into consideration. So, we find that as the fan-in is increased this rise time will also increase; however, worst case rise time will be equal to R P into C out p plus C out n plus C L only when 1 transistor is on; that means, although n pMOS transistors are in parallel in the worst case the delay with the rise time will maximum only only when 1 of them is on similarly, the fall time is n R n into C out n by n plus n C out p plus C L.

And again in this case when the and also that expression for charging the input capacitance is given here this is the expression. And when C L is large the t d f is equal to n R n C L and t d r is equal to R P CL. So, here we find that the fall time for the NAND gate is affected and it increases linearly with the value of n for large. And the rise time is not affected much it is very it is very similar to that of an inverter.

Similarly, for the NOR gate we find that t d f is equal to R n by n into n C out p plus C L in this case you know p n pMOS transistor are in series that is the reason why the fall time will not be affected much and in for n is equal to I mean when only when one of the transistors is on then it will be equal to R n C L R n C L as you can see; however, the rise

time will be affected with the value of n it. So, t d r is equal to n R P C l. So, for large C L load capacitance it will be proportional to the fan-out is affected by the I mean, the for delay that t d r will be affected by the number of inputs so n R P C L.

So, this is how the delay times are affected, because of fan-in is demonstrated not only fan-in, but also it shows it is proportional to C L; that means, the delay characteristics switching characteristics is affected not only by fan-in, but also by the fan-out or load capacitance. You see whenever the fan-out is increased essentially the load capacitance increases.

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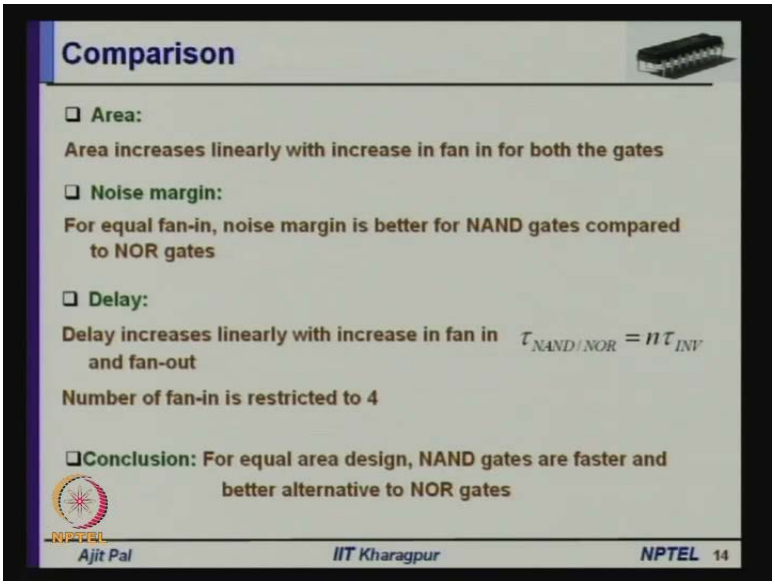

So, here is the comparison of different parameters. We find that the area increases linearly with increase in fan-in for both the gates. That you have already seen, because we are increasing the number of transistors we have seen that as the fan is in increased the number of transistors is increased, for 2 input it becomes double that of an inverter and for n-input there are n pMOS and nMOS transistor. So, area increases linearly as the value of n increases. What about noise margin for equal fan-in noise margin is better for NAND gates neither compared to NOR gates. That you have already seen how the noise margin is affected based on this particular table particularly, we find that the noise margin is I mean; good I mean neither is better for NAND gate compared to NOR gate for equal area. So, in that particular case we considered minimum area.

What about delay increases linearly with increase in fan-in and fan-out? And particularly for NAND gate and NOR gate with respect to the inverter it is proportional to n, Where n is the fan-in of any NAND or gate NAND or NOR gate in addition to that that. So, n is the fan-in it has it has dependence on fan-out as well and that is the reason why the number of fan is restricted to 4 although gates are available with fan-in starting from 2 to may be 8, but whenever you realize practical VLSI circuits of reasonable performance then, fan there is some restriction on the fan-in is usually restricted to 4; that means, whenever you will choose standard gates from the library you will choose gates with fan-in less than equal to 4.

And you will realize multi-level circuits using gates with fan-out fan-in is equal to 2 or 3 or 4 not more than 4. So, what neither is the conclusion conclusion neither is that for equal area design NAND gates are faster and better alternative to NOR gates. So, this is the conclusion that we can make from the comparison of area noise delay and other parameters.

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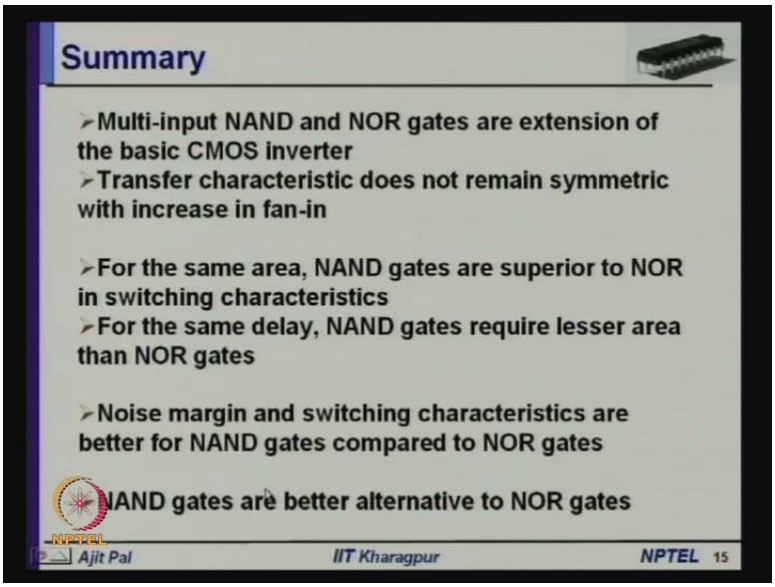

So, here is the summary of different types of whatever we have discussed today. So, multi-input NAND and NOR gates are extension of basics CMOS inverter we have discussed. How the how the multi-input NAND and NOR gates can be realized by extending the basic concept of an inverter, by adding more and more number of transistors as the fan-in increases. And we have seen the transfer characteristic does not

remain symmetric with fan-in. So, transfer characteristic is affected with the fan-in that we have discussed in detail. Now for the second third conclusion is for the same area NAND gates are superior to NOR in switching characteristic, another very interesting point that we can consider we have seen that the switching characteristics is becoming asymmetrical as the fan-in is increased.

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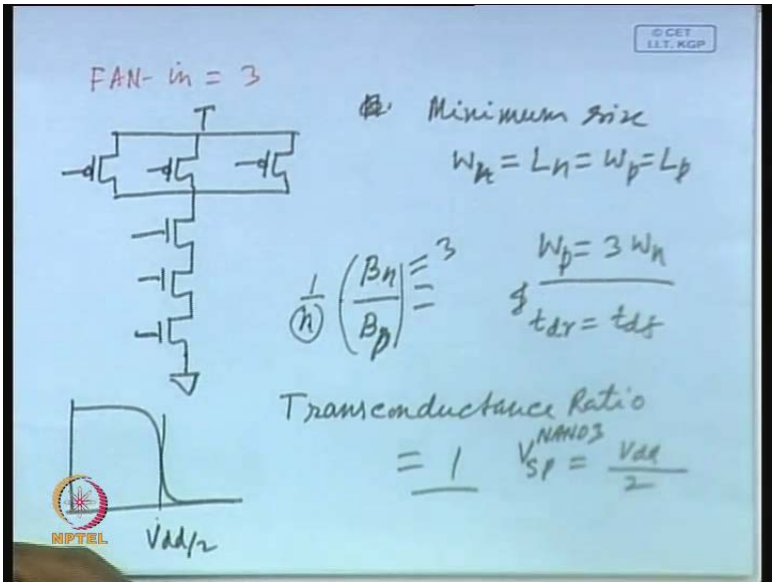

But if we consider say fan-in is equal to 3 let us consider a NAND NOR NAND gate. In case of NAND gate we know that we have 3 pMOS transistors in parallel and three nMOS transistors in series. Now in this particular case if we consider minimum size minimum size then; that means, W L is equal to W n is equal to L n is equal to W p is equal to L p. So, in such a case what will be the switching characteristics of this particularly the beta n by beta p ratio in this particular case, will be equal to how much. As we know since they are of the same length and width, we know that for n for n for a for this particular configuration beta n by beta p corresponding the equivalent beta n by beta p will be is equal to 1 by n. What is n n is the number of inputs in this case.

Now, we know that beta n by beta p these value is also 3 in this case n is also 3; that means, we can say this the this trans conductance ratio is equal to 1, because beta n by beta p is equal to 3 and n is also 3. So, this makes it 1 so that means, for a 3 input NAND gate the inverters the switching point will be exactly at Vdd by 2, because the equivalent

beta n by beta p trans conductance ratio beta n by beta p is equal to one we know that when this is 1 then the beta the V s p say NAND 3 will be equal to Vdd by 2.

The reason for that is denominator will become 1 plus 1 and also numerator will be the t p and t n will cancel it will be Vdd. So, it will be Vdd by 2. So, we find that for this particular case it is becoming perfectly symmetric, but that will not be situation for NOR gate. And that is the reason why our conclusion is for the same area NAND gates are superior for NOR gates in switching characteristic particularly, the fan-in is the noise margin is better. And also for the same delay NAND gates requires lesser area than NOR gates. We know that if we want to have the rise time and fall time identical, then the W p has to be 3 times that of W n. So, this is the requirement this is the requirement for equal rise and fall time. So, t d r is equal to t d f if we want this then this is the requirement. So, in such a case the area increases that is the reason why we can say that for the same delay NOR gates require lesser area than NOR gate NOR gates and for the same area NAND gates are superior to NOR gates in switching characteristics. The noise margin and switching characteristics are better for NAND gates compared to NOR gates that we have already discussed in detail and NAND gates are better alternative to NOR gates.

From all these discussion this neither is our conclusion NOR gates are better alternative to NOR gates. So, although this is our conclusion from the by considering the noise margin, delay characteristics, area NAND gates are superior, but in practice we shall be using both NAND and NOR gates together. So, you will see that whenever you are you will be realizing multi-input, multi-out multi multi-level gates, multi-level circuits, multi-level multi-input circuits. Then you will find that we shall be using both NAND and NOR gates, because in that case, overall area, overall delay characteristics is important rather than individual area or delay characteristics.

So, our conclusion is that we shall be using both NAND NOR and other types of gates in realizing circuits, but if possible, we shall choose NAND over NOR whenever it will be permitted by by the realization technique. So, with this, we have come to the end of today's lecture; in the next lecture, we shall continue our discussion on the same topic that is your static CMOS circuits, and we shall consider, how we can realize other types of gates and more complex types of static CMOS gates thank you.