Embedded Systems – Design Verification and Test
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Lecture – 30
Testing for embedded cores

Hello everybody and welcome to the ~~third~~ 3rd part of the course on testing which is the part of our total course on entire system embedded system design verification and test. And now as we are looking for the last few weeks we are dealing with embedded system testing. So now, also we have covered the first module on the testing part which was on the basics and after that we have started covering some very important topics which are more focused to embedded system best tests.

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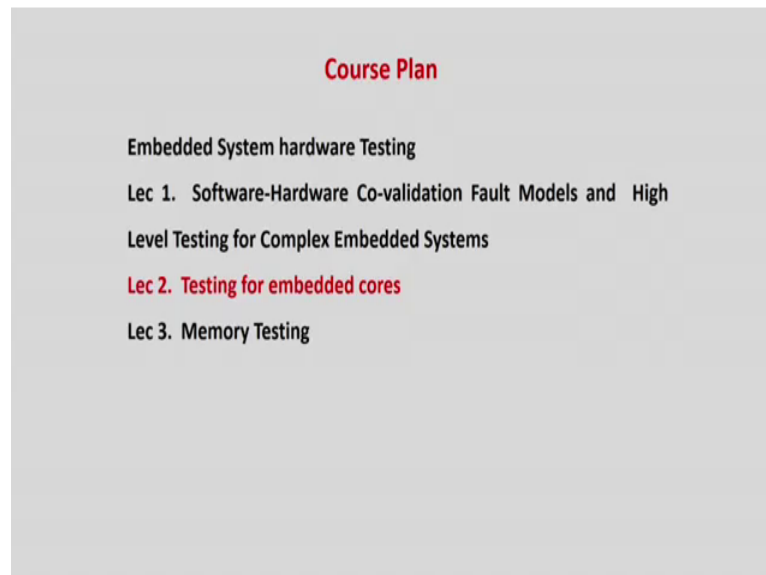

Again the last lecture we have seen how basically high level or functional fault models are used for testing of complex embedded systems.

What we are going to see today, we are going to see today there how you can access the points of testing in embedded cores. Let me make this story a little connected to whatever we have learned in the first few I mean first few preliminary lectures that if you

want to test a system you have to first find out the vectors and then you have to apply them.

For doing it basically there is something called an ATE or some equipment from which you can apply the tests, but in case of embedded system design we generally have a large number of ICs or in other words they are called cores which are in a bigger system. So, it something like a system of systems, like in this say like system of hardware modules. So, there can be a larger module inside that module there can be small hardware modules which are fabricated in a chip.

So, we call that embedded cores why the concept has come basically the concept has come because one vendor cannot be expertise in manufacturing or designing all kinds of IP cores. Like one person can be more dedicated towards graphic processing one can be more dedicate toward generally designing of processors one part we can one vendor can be more expertise in design or on chip memories and so forth.

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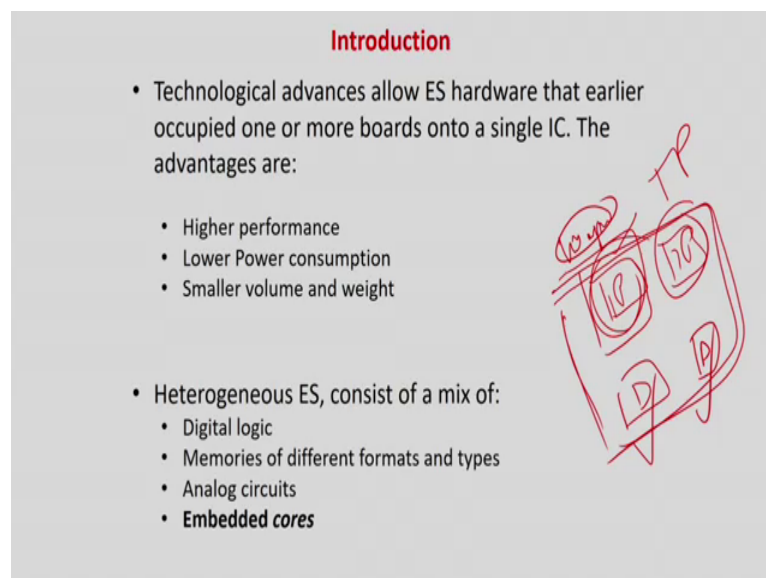

So, what a person does if you have to design an entire embedded system hardware you will design some of the modules and other modules you will procure directly from some vendor who is expert on that and put them together on a single die and give it to fabrication. Because embedded system hardware when we say in that fashion or a system of chips or basically network on chip it is not like that you buy individual discrete components and collect in a board that will make things word frequency will come

down, because you know that whenever we have multiple systems in a PCB the interconnecting wires etcetera take the most amount of dealing.

So, better with that we purchase all the cores, cores means the hardware design or design in a hardware level, it can be at the register transfer level code it can be at the gate level or it can be even at the layout level with purchase those codes and put it in the die according to the placement requirements. And then also we put our logic blocks whichever we have design and finally, give the chip for manufacturing. So, that is what is called the embedded system core base design.

Now, what happens? So, if you have such a system. So, in which case for some of the cores which I have design I have entire knowledge I can put my DFT requirements how where to put scans, etcetera; and I can make my life ease for testing. But think of the other cores which I have purchased some other vendors they may not be actually if they are called IP cores because nobody will tell you about the internal details of their design. They said that is the processor they will give me the processor, they will tell me that what are the test vectors required to test the processors, what are the routines etcetera, rather than that they will not give me any more details.

So, I cannot change it for most of the cases I cannot put additional DFT and, but still with the existing test vectors which is even given by to me by that vendor I have to test it entirety in entirety like I have 4 modules. So, let me assume that this is my entire die. So, these are the 2 IP cores which I purchase from the market. Core means they are also simple hardware designs they can be at the gate level, register transfer level or it can be at the layout level and 2 I design these are my designs. So, I have design these 4 blocks, in one die and I send it for manufacturing.

Now, for this I have full control for this I have full control I can put my DFT circuit etcetera, but for these blocks I do not have much information, only because they are IP cores which have been sold to me by the vendor. Why I am purchasing it because I do not have much expertise to design them, better I purchase it. And I concentrate on my design, but I have to design the entire embedded system hardware and share it to the markets and is a very standard practicing current industry.

This is just like software module that some modules you develop and others you use library modules, but in case of software basically there is more flexibility, but in

hardware the flexibility is less. Because, once you fabricate it the whole thing gets fabricated and you have to depend on the performance of not only on your own design, but also for the other design, the rigidity is more in hardware as you all know.

So, now, secondly, nobody will tell you the internal details, but of course, you have to test them. So, what the this people will do these IP vendors will do, they will along with this IP cores they will also give the test patterns which is required to be tested. Again and one more thing basically they will also give sometimes is call something called a wrapper they give a wrapper; that means, the way to access this IP blocks in test mode and normal mode.

Because there is a entire circuit given to you because what I you can read about some other books also on test based hacking. So, if there is lot of access given to this internal IP core because for the cores you have design I have full knowledge, but for the IP cores I have sold it to you to be using I do not want you to back engineer it or reverse engineer it.

So, now what happens if I have, if I give more access to the pins of the IP cores? I can do a reverse engineering and again try to find out your design. So, what they do they give also a wrapper kind of an architecture over the IP cores which tells you that these are the patterns to be applied and wrap you can you have to apply through the wrapper they will make proper interconnection between the IP core and the external world.

And there can also be a operating mode normal operating mode which is the normal function mode. So, also then this they have a wrapper so, that it becomes a very well means encapsulated IP core. So, that it functions in test mode as well as you can test them with the vectors already provided by the vendor, but you do not get much inside into the design. So, this is actually called core base embedded system design.

Now, the challenges remain that how do you test in entirety? Test patterns generation is very simple in this case for these designs I generate by my own algorithm for these IP cores the text pattern are already given to me by the vendors. Now, the problem is that I have to apply them why, some picture I will show you then again; I will come back to the normal discussion like this.

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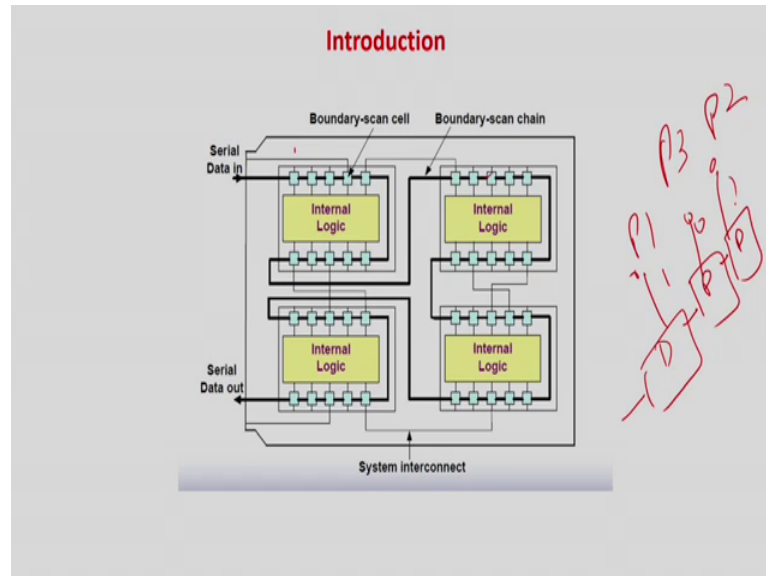

So, there are may be 4 internal logic blocks may be this I have designed. And this I have designed and this one is actually IP and this one is IP.

Now, how do I apply test patterns because the number of input outputs may be very less maybe I can say that these are the in IOs, these are the IOs, these are the IOs, but these are some of the internal piece which are not directly accessible, because they have 4 IP cores and they are the internal lines. So, there should be some mechanism so, that I can apply the required test vectors in this pins also.

So, in case of embedded system based IP core testing the main challenge is accessing this internal pins or internal IOs of the cores which are not accessible to the output world. Generally in a single if is generalize 2 form not only IP core for any core based embedded system design.

Because, there will be multiple cores whether you manufacture or you get it from the IP vendor, in case of IP vendor the problem is more higher because you do not have any control in the internal logic. Like for example, if you have all the 4 cores designed by you then if required that I want to apply some test pattern over here, some test pattern over here, I can make some more adjustment maybe, I can if something sometimes it happens that lot of test patterns are required to be applied to this pin, then I may try to make this as a input output pin I can put this block here. So, that there is a direct input output connection maybe I can replace this block sorry.

So, this IO pin here I can do sometimes of reorientation. So, that it becomes the input output portion more available to the IO lines there is external world IO, but it is not possible in the case of IP cores, because in case of IP cores everything is fixed you cannot do more changes. So, the problem will really happen if the I have to apply lot of test patterns at this pin to test it.

So, testing of IP cores the main issues or IP cores or any core in that fashion in case of embedded system the main problem arises how to access this internal pins and how do apply test patterns, that is the main challenge. And in today's lecture we are going to look at it that how can I access these internal points and how can I apply test patterns to that.

Again repeating this is the story with any embedded system core based design because the cores are somewhat chips in itself, but they are not at the level of external devices which can be put in a breadboard sorry in a PCB whether this is a single silicon die and basically you are putting all these at the fabrication level. So, that this the delays between this interconnects are much lower and you can have a highest frequency operation for the entire embedded systems hardware.

So, they, but problem happens is that of lack of observability and controllability, because these are the pins which lack observability and controllability. How to access those pins and apply test patterns is the main challenge for embedded system core base design which we are going to look at in this lecture. So, with this picture I have given you the motivation.

Now, basically technology advances allow embedded system hardware that earlier occupied one or more boards onto a single IC so; that means, if you think of entire system in previous disk there used to be multiple chips or even multiple boards connected to make a system ok. But now basically problem is that of a multiple board size may be larger and all it is may be slow or low power will high power will be high power will be consumed etcetera. So now, what happens basically we are putting multiple cores in a single silicon. So, it leads to higher performance, low energy consumption and smaller weight and volume.

So, instead of multiple boards or single board with multiple chips now single die with multiple cores so, but actually this also this cores are mainly heterogeneous, they can be digital, they can be memory, they can be of some other embedded kind of hardwares,

they can be analog circuits and so forth, and there can be also IP cores. So, basically different natures of cores will be placed in a single die and you have to test it.

So, that is what is actually nowadays embedded system hardware cores are of heterogeneous nature, but again we are only looking in this cores mainly a digital. And memory chips (Refer Time: 10:39) same called as IP cores ok. So, IP cores of something like it can be digital analog and have been memories, but people will not tell you about the internal details it is IP protected ok. So, different type of mixers or different types of cores are possible.

In this lecture mainly will be are focusing on or in this cores mainly your digital. And basically your memories, but again I want point one type trying to try here that, testing an IP core or a testing that IC in separation have no problems or they are very similar for the test pattern generation. Test pattern will tell you what to be applied and what we will get out of the golden response, only when they are in multiple what do I say in a single core multiple ICs are multiple cores are put in a single die the main problem is in accessing the test points. So, that is the main challenge of core base testing which we are going to look at ok.

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Introduction

In traditional system-on-board systems components were ICs, designed, manufactured, and tested by the same vendor

In modern ES (SOC and NOC), components are cores (soft, firm, or hard) that are not yet manufactured or tested for defects.

- Large, reusable building blocks
- Reuse speeds up design, brings in external expertise.
- Examples of core functions:
  - CPUs and DSPs
  - Modules for graphics computation, e.g. MPEG and JPEG
  - Memories
- Core Types
  - Soft (RTL code)
  - Firm (netlist)
  - Hard (layout, GDS2)

So, in traditional system on board components were ICs design manufacture and tested by the same vendor that was generally the case in a very slightly 30 - 40 years down the line. Generally what happen there used to be a board and used to manufacture some

chips and you have to put on them and sometime if some of the chips were also from the other vendors people use as there is available as discrete elements, they could test it and they mean and they could also guarantee to be it is correctness by the vendor we selling it. And then when you have putting in a board if you required to test other chips also you could put another discrete components. What I am trying to say here is that, maybe this is the board not this is the PCB right and maybe we are having these 4 chips because in a in a previous it was chips right.

So, we have basically this is chip 1, chip 2, and 3, and 4 maybe we are purchasing from the other vendor. So, they are discrete component tested and put it. Maybe after that this interface may be difficult to test because the chip point basically the boards IOs are discrete right. But still you can make a probe here it is more simpler to probe these lines and look at the values that is possible, but certainly difficult not as simple as the standard IOs.

But still you can do it as the board, but in a die if you the silicon you cannot probe this you require a external prober (Refer Time: 12:42) very difficult to break it break the chip and actually probe this line in a PCB it is much simpler. Not only that also you know that if I want to test this line I have to actually make a multiplexing arrangement because where I am applying something to this chip data should not come from here, I have to give some external test data.

So, that is possible I have to put some multiplexing arrangement like this is chip 3 I put some multiplexer and this is your chip maybe this is your multi twist one multiplexer, this is your normal input sorry, this is your test input, this is your normal input and this is chip 1. So, I put a multiplexer and normally this one will go and the test mode external input can be go given. So, I can easily put somewhere a multiplexers are I can do it because in the previous day I was to procure all these chips and put it in a board.

So, wherever such type of difficult to observe by control lines whether I can make a multiplexing arrangement, but see in the die sometimes this is very difficult to do because there are lot of other issues like loading, loading means loading of the pins etcetera. There is unnecessarily you want to this is a big die like something where you are putting some of the IP cores because some of the IP cores you are putting, here if I put some kind of multiplexing arrangements so I mean; and I do not know much details

about this IP cores. And also in a chip inside a chip fabricating some extra basically multiplexes etcetera may not be that easy as it was done in a board and also not very adobe.

So, I should not say it is more difficult because putting an extra multiplexer in a board as well as die is now there is silicon chip also is not is almost equivalent in difficulty level, but in the traditional level when we are doing board base design it was up to us, that these pin is very important I can put a external marks to go for test mode. These pins are not very important I can take a adopt decision because I most of the chips are built by me or few I have taken and I am soldering when we have PCB. But in case of a silicon or a die it has to be manufactured it has to be fabricated. So, I have to very careful on what I am doing with the pins.

So, there should be proper protocol that manufacturing this devises or when in the case of a chip, to CUT the short story, long story short in case of board base design, PCB base design I can do take much ad hoc decisions because I was actually purchasing chips and manufacturing and doing a soldering which is much more simpler then doing a fabrication. In fabrication everything should be very much in a protocol or should be following a standard. So, core base embedded systems testing to access those internal pins there should be some kind of a standard, which allows a particular way of accessing these points or controlling this point. So, that is one more important aspect we have going to look at in this lecture, that in core based embedded system testing there what are the ways we put some points in the internal of the interconnection of the your cores and how we can access them.

So, in modern embedded system like NOC SOC components are basically cores. So, cores can be soft core, firm core and hard core, rather I was saying. So, basically what is the soft core, soft core means you purchase the RTL design. So, in this case is RTL (Refer Time: 15:38) core given to you in the register transfer level. So, slide modifications you can do based on your agreement with the vendor.

There is something called firm core with a net list they will give you the gate level design, there was you can slide changes can be done, but of course, you are not going something like in EXE file is given to you, you do not know much about what exactly is the logic behind it. Means synthesize net list OR gate level design is given to you, many

times you also purchase a hard layout, hard core; that means, only the full layout has been given to you, very very difficult to make any changes because it is full (Refer time: 16:09) level of transistor design is given to you.

So, generally full secrecy is one they generally sell us hard core, firm cores and soft cores basically are more flexible and you can very easily know; what is the functionality of this cores. So, they may be more cost costly to purchase and because we are also you can also do some kind of little bit changes and there is no secrecy in those designs. So, generally for most of the cases I will prefer to purchase a hard core, because I do not want to invest much time on the other vendors expertise; I will just take the hard cores put it them together I will put those cores which I know how to design and build a complete system and sell it to the market. Also sometimes it happens that some of the vendors they do not design anything, they basically take all the hard cores in the layout level put them in a single die made the interfaces and sell it as a product.

So, in that case that company does not know the internal details about any of the cores, but they are for every with every core the test patterns would be given by the vendor this is that if we apply then the circuit will be tested. And then, they do some kind of a testing of the internal cores and then you have to also test interconnects and as we will see more in this lecture. So, the idea is that the cores with the test patterns are purchased they are put on to the chips individual core testing functionality will be done by the test patterns given by the vendors.

You have to now on, but only check the interface you have to test it because I have put the cores taken from the vendors, but I have to now check the validity of the interconnects and totally integrity I have to validate and there I can sell it to the market. So, that is also in picture that I may not be manufacturing any of the cores myself only I am doing the integration, testing, integral testing and selling into the market, may be some I o I will design and do. So, that we is the modern embedded system industry going on.

So, basically why it is large, reuse speeds up designs and bring external expertise. So, basically what you can speeds up the design process, if I have doing all the designs myself then it will take a long time to do it and I will be showing in selling my product to the market. So therefore, what it does, you take different products from different

company and put it together and sell it. So, the actually is an external expertise. So, the expertise for my company is not to build it, but rather integrate it. So, therefore, testing in embedded system core base design is the different challenge then what you have been looking at in the first few lectures the test pattern generation, how to optimize that and so forth, here the idea is integration and how to access those internal pins.

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Introduction

- ES Core user responsible for manufacturing and testing
- However, this is not possible without the assistance of core designer because core design is IP (hard cores).
- Typically, core designer assists by delivering pre-defined tests with the core.
- The problem that faced the core designer was how to apply these tests at the core boundaries.

So, basically embedded system core user responsible for manufacturing and testing that is I am the core user. So, basically I am going to fabricate it you have only given by the design and a soft level; that is basically the net list level or the RTL level or basically at the gate level or even at the layout level, but I am going to put everything in a die and I am going to manufacture it.

So, see basically I have purchased from you the GDS to level that is the layout level of the chip or the core and also maybe at the RTL level, I am purchasing from several vendors putting it to a single die in a design sending it for manufacturing. And finally, I have to get it from the vendor and I have to sell it on everybody's behalf. Then what I have to do, I have take those core manufacture it, test it, test pattern somebody else well give it to me means whoever has sold the cores will give it to me, but it is my job to test those individual cores as well as the integration which I have done.

So, the core user that is basically see there are I am user I am using your all of your cores which have given me this is my responsibility. However, this is not possible without the

assistance of the core designer because the core design is IP. So therefore, you just sold me a black box I have put as the internals, but you will not to tell me the internals. So, what I can do, I have to take your help and; obviously, as you are you have designed you will not tell me the internal details, but you will at least tell me apply this pattern box and everything will be tested.

So, those things we will give it to me at the test patterns. So, the core design assists by delivering predefined tests with the core you will tell me that these are the patterns we apply I assure that if you can apply these test patterns you will getting 99.9 percent coverage etcetera for this fault models. But now the problem is he is designing a core and he is saying that these are the pins you have to access and do it, but the problem is that now this will be in a bigger design. So, maybe I will this will be coming into another chip like this another block and these may be your input outputs, may be these internal pins and these internal pins of these 2 cores cannot be available as output.

So, the test pattern or the core builder or the core where designing of the core will tell you have to apply these patterns over here. And you have to probe this patterns over here this is a response from this pins. And you are going to get the response analyses, but these are now becoming internal part of your main chip. So, I have no access. So, in case of embedded system design as a core mean of the as the manufacture of the entire system purchase in the core some external people it is my duty that how I can access these internal pin so, that the entire system can be tested after manufacturing.

So, now the person who is actually designing or manufacturing these cores or embedded system entire design from the cores it is his duty then how we can access those internal points. Again repeating because embedded system core base testing means that is what is to be emphasized, the test pattern generation not problem people are give in me the test patterns I am putting them in a single die my point is only how to access these lines and do it. As I told you is a not of PCB base design it is an the chip is manufactured after putting all these all these cores. So, they has to be some kind of protocol a nice standard of how to access this internal pins and how to apply the test patterns and how to observe this responses right.

So, the problem faced by the core design was how to apply these tests at the core boundaries that is what is the problem, that some pins will become internal pins these are

the core vendor has send you an entire core with input outputs, but some of the internal pins will be now internal pins of the core how to access them that is what is the challenge of core base testing. So, again this is what was my over I am this was what our motivational example. Like whoever has sold this core to me he will tell you see these are the internal pins we apply something, these are the external pins somewhere you have to observe the response analyze fine, but after it is becoming I have put it in a single die and manufactured it. So, these are the pins which are no longer access to no longer access from the external word, maybe I can tell you that these are your external pins, these are your external pins, these are the external pins, these are the external problems are with this internal logic how to how to access it.

So, again very famous old story scan chain is going to help you. So, what is the scan chain as you already know scan chain means some of the flip flops are made in a single shift register fashion and whatever pattern you want to apply you apply it and set it accordingly by the scan shift. And once the flip flops are you have got those values you can again go to the normal operating mode and test it and again capture the response in this scan chain again bring them it out. Simple idea is that may be multiple points in the circuit has to get these dilutes which are fed by we will flip flop. So, now, what you have to do, say for example, Point 1, then Point 2, like that lot of points are over here Point 3 there points are there and these are all connected the D flip flops, these are the D flip flops and these are the D flip flops right.

So, in a scan chain what you do we put all the flip flops in a chain in the test what and whatever value 1 0 1 whatever are required to this point. So, you shift them by using a scan using the scan mode those are these are apply when you get the they get, and you can do the test and again take back the response from the scan chain. Same philosophy has to be apply or rather that is the natural way of doing it when I am going to access these pins, but in that case the pin scan chain is not the internal of the core they are basically at the boundary points of all the core pins as we called it is the boundary scan we can actually call the what is the boundary scan. That means, all these IOs so, may be this is your one core. And this is one, this is one some of the cores right. So, what we do is that a I mean along with the normal pin we actually put a scan register that is called boundary scan register these are the all the boundary scan registers.

So, basically let me zoom it for you let me zoom it for you so, you can look at it. So, it says if you look at the chain is thing. So, basically these are the external IO lines, but here we are actually put some extra logic which is called the boundary scan registers they are nothing, but flip flops. So, for example, if I want to access these point what I can do is that, I can shift the values in a scan mode and I can bring the value over here may be I require a one over here so, you can start shifting the values to this part I can easily accesses this.

These points are not of a problem to give any values because they are directly connected to the input output lines, but for the internal one I can actually apply a scan mode and I can bring in and here simple (Refer Time: 24:19) multiplexing arrangement like a scan register will be there. So, we will decouple it and the value will be available over here, same philosophy is applied, but actually you have to apply it in a scan mode like a simple scan architecture.

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IEEE 1500 Standard for Embedded Core Test

- Proposed DFT based SoC/NoC test standard that facilitates embedded core and interconnect testing and test reuse
- The Scalable Core Test Architecture comprises:
  - Source and Sink for test stimuli and responses.
  - Test Access Mechanism (TAM)
  - Wrapper
- The source and sink for test stimuli are provided by the ATE
- TAMs are mechanisms used to transfer test vectors and responses to and from the core, respectively.
- Wrappers exists around each core to connect TAMs to the cores.

So, this standard as I told you, this is the core idea of doing a core base testing and the I mean a they were different levels of standards that came up into picture we started with 1149 dot 1 then dot line which is for analog and for embedded core test they call it the IP I triple E 1500 standard. It is proposed DFT based NOC test standard that facilities embedded core and interconnect testing and test reuse. That is the core idea that it will test the internal logic as well as the interconnect chain because as I told you the vendors

will have sold it to you with the internal logic to be tested they will give you the test patterns, but it is my duty how I can test this internal lines that internal connections, because I have taken them I have integrated them. My job is to use the patterns given by you to test the internal logic, but this internal interconnects I have to do the test.

So, like the way I scan chain there is a protocol of designing scan chains similarly if I am doing at the boundary level or basically I have the core level so, it is call the I triple E 1500 standard. So, basically this scalable it contents source and sink for test stimuli and responses, which is called the source generator and analyzer. This something called test access mechanism because there multiple cores inside it. And you have to target one core at a time when you are doing the internal test and where are they when you are doing interface test multiple 2 cores may have to be taken into account.

So, somehow you have to access the internal of the chip where lots of cores are there. So, it is called the test access mechanism and very something called the wrapper, because the way you can directly access the IP core may not be all pins are directly given to you as the output in a flat nature for testing. If you look a if you want to read more you can find out that how you can know the internals of the chip by taking this scan out values. So, there are lot of attacks which tends to know what is your IP design by scanning in the values of the scan chains.

So, therefore, what people do is the, they will put a wrapper. So, that if the test patterns can be applied and response can be obtained through a buffering. So, it allows the integrity of the IP core. So, the source and sink are generally ATE if is your base it will be a internal hardware if it is from the basically your external equipment it can be through the source and sink at the ATE that so forth. So, source and sink means some pattern generator which can be external or which can also be internal.

The test access mechanisms tams are basically used to transfer the test vectors and responses to and from the core respectively. That is some internal collectivity has to be there, because if you look at it in this case the idea is something like if I have to access give some values over here may be this point is not directly available to me. Therefore, there should be test access mechanism; like in this case I can say this whole scan thing is basically a test access mechanism.

So, for some of the important course I can give some dedicated lines because maybe if these 2 pins are always accessed. So, to reduce the test latency I can make this is a direct input output perhaps some kind of logic. So; that means, are the way I am giving access to the internal pins of your core is called the text access mechanisms. Wrappers exist around each core to connect the tams to the core as I told you that there should be some kind of a buffering to do it.

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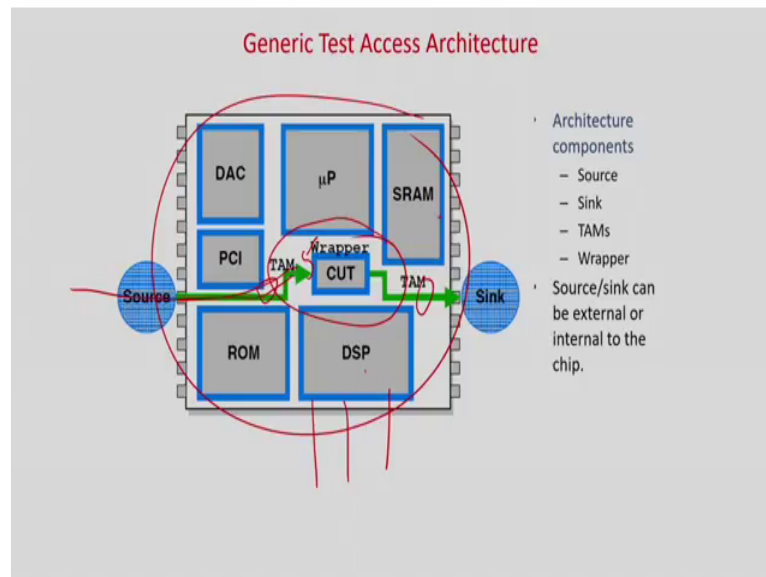

A simple architecture is shows that maybe I am going to test this undercut. So, this is the source and sink source and sink means is may be ATE, this is also the ATE this one, but this is the wrapper, wrapper will actually tell the protocol how this test access mechanism or how the pins will be connected to the wrapper to test the core. And what is TAM?.

TAM is basically how you connect the source and sink to the CUT. So, as I shown you this boundary scan method can also be one way of having a TAM is one way of accessing the test lines right. It can also be something like is a very highly critical means part of the core which as to be tested, many test pattern has to be given and recorded. So, I can put some kind of dedicated lines input output lines for that, for all other these are the others I can put basically may be a scan register because testing by scan method will take long time.

So, if more test time will be required. So, if less patterns can do the testing so, I can use correct to a scan register and for the CUT for this IP block maybe it is very lot of test

patterns are to be there is a very critical block. So, I have to put I have to test exhaustively. So, I can put a direct connection by wrapper to this through the input and output. So, therefore, it is actually called the TAM, TAM means how you access the points.

Source and sink means we are generating the pattern and (Refer Time:28:41) is it can be ATE for a offline test, for a bist it can be the internal sources like test pattern generator response analyzer can be put on the chip itself which I think we will have lot of full lectures are also available on built in self test down the line, but for the time being you can just take the fact that for bist means basically the test pattern generation and analyzer are put in the same on the same chip rather than basically using a ATE to do that right and the wrapper.

So, now, we will basically try to look at mainly we will try to look at these 2 parts in details, because the source sink and source are nothing, but some ways of generating the patterns means generating the patterns means applying the patterns and analyzing the response.

So, now important is Test Access Mechanism, there how you do access the chips

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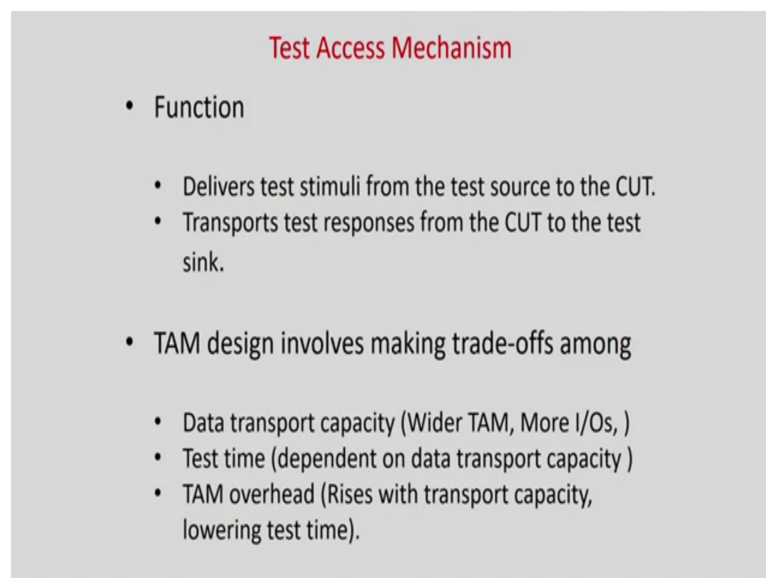

So, it delivers test stimuli from the test source to the CUT transports test responses from the CUT to the test and sink that is the job. TAM design involves making lot of trade offs

as I told you if ever full scan base design it will be the very simple low cost TAM, but the problem is a test time will be large because you have to scan the values and bring it to the point to the testing.

So, test so, it depends like and also may be I can have a serial TAM single line. So, one by if 5 values has to be applied over a is a single bit. So, you have to do it serially if I have a parallel TAM I can put lot of values directly. So, is you have faster way of handing. So, we can easily understand is a trade off speed and resource speed of testing and the amount of resources used.

Test time depending on the test transport capacity. So, test data transport like test data capacity there is wider TAM, more number of IOs, as I told you will have a higher access to the chip and, but resources will be more. TAM overhead means rises with transport capacity, lowering test time. So, if you put lot of TAM resources then basically lot of test patterns can be applied in parallel faster, but it will actually it will lesser lower the test time, but the TAM GFT cost will basically be rise in.

So, some people also thing that if I have to go for as speed test is very fast I have to test it then actually you can also reduce this physical distance like for example, if it is a long line why it is very important over here, because single core and single chip and chip with multiple cores means this area will be quite large. If this is a chip these are all individual chips then I can ever direct access and the test and the wire lengths are less, but in this case as these I have to if I have to directly access these TAM then may be the wire length will be higher.

So, leading to higher stray capacitance and resistance and we cannot apply test patterns at a very higher speed. So, if I can some of put this on chip. So, basically I can go for add speed testing, because the even just take because they have full device physics, but the idea is very simple if you have a very log wire length. So, the capacitance and resistance will be higher. So, you cannot puts put very high speed clock pulses there, but if I can put everything on chip there is test this length of this will be lower and basically you can put you can do high speed testing.

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Test Access Mechanism

Physical distance

Ways to reduce TAM length

- On-chip test sources and/or sinks.
- Sharing TAM among cores can shorten the total TAM length.
    - Reduced wiring area.
    - Possibly reduced test concurrency.

Reusing functional hardware as TAM.

- May not meet the desired test time constraint.

So, we can put on chip sources and sinks and also that will make high speed testing also TAM can be shared among multiple cores right. So, basically what that is an shared bus ok, but actually it will reduced the wiring area of course, but it will lead to reduced test concurrency; that means, what is the shared bus.

So, single TAM the bus multiple chips are accessing it multiple cores are accessing it. So, you can access one core at a time such are the concept a very similar like a single bus and a multiple bus architecture. So, the idea is very simple, but you can if you are having more resources for the TAM, TAM is nothing, but ways to connect to the different pins of the wrapper for testing the cores. So, more resources like more parallelism, more number of bit width you to make for the tams if you give more parallelism to that your TAM overhead will have a test time will be reduce. If you are using shared TAM like shared bus, if you are using a serial TAM actual the problem is that test time will be higher, but your overhead for the TAM is going to be lower.

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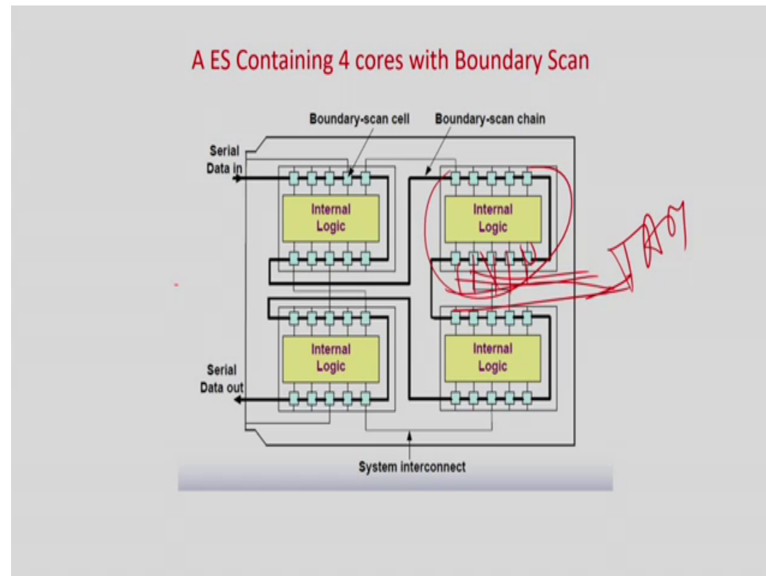

So, again the same thing I am showing you with embedded system containing 4 boundaries with boundary scan. So, in this case you can tell that it is a very simple one I am giving the whole access by a scan. So, in that case that is my TAM, that I access each these lines through a single scan chain, as I told you can also if these are very of very important lines. So, I can have 5 multiple input outputs where I can connect this line. So, this will be another TAM for maybe it is not maybe these 2 chips are not very important; sorry may be these 2 chips are very not very important I am anything about this chips 1 2 3 4 5 I can connect these lines and this will be set TAM for this logic.

So, I can have a direct parallel access to this it will be more faster to apply the test pattern simple logic. So, TAM means how basically you can access it and higher will be the more weightage you put on the overhead. So, basically have means more we put on the TAM sources test time will be lower. So, that is actually the idea of a TAM I will elaborate how it looks like basically is nothing, but simple scan registrant I have slide modification of course.

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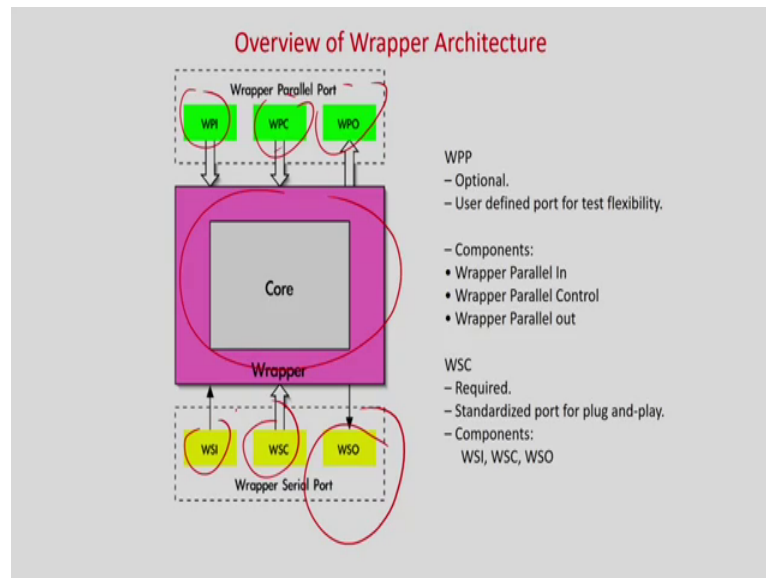

So, basically these are wrapper. So, this is the core, as I told you as basically we are basically not having a not a PCB kind of our design. So, is a chip which will be finally, fabricated show we should basically always tried to follow a particular protocol of design and it is basically I triple E 1500 standard. So, the core, and of course as I am manufacturing a chip I have make it IP protected I have to sell it. And everybody will be connected through a single TAM mechanism for a very nice single stranded architecture. So, I have to maintain a protocol.

So, if I have a difference wrapper, you have a different wrapper, he is a different wrapper. And I have to put in the single core and try to test to whether can be a problem. So, therefore, while designing the chip with the wrapper I have to know that there should be particular standard of accessing all the cores 4 pins. So, have to follow this standard. So, people also design a manufacture in the standard format. So, there is very easy to put the chips put it in a single die and you can use the 1500 standard to access them and you can easily there should be no problem in handling the testing of different chip from different angles. So, you always maintain a standard.

So, basically we have they said WPP which is actually call the wrapper port. So, this is the some ports which I have parallel access. So, WPI basically it is Wrapper Parallel In, parallel out and parallel control, control means basically means which of the pins you will want to, which of the lines you want to have a in test mode which mean you have to

want to in functional mode and so forth. This SI just the just the controlling just like controlling that which pin like control means what, just like your scan chain you have seen test mode working mode that is actually control.

So, this is parallel wrapper parallel port is optional is to speed up your testing requirements. So, PI WPI; WPI this is parallel the wrapper parallel input parallel output multiple pins you can apply to give the test patterns, here the TAM will be a higher overhead because multiple parallels can be given and these are control. Control as I told you is when to go for test mode when to go apply it for functional mode etcetera, but this is must, wrapper serial port is a must.

That is wrapper serial input, wrapper serial output and wrapper serial control that is that is what is basically nothing this one this is a single line. So, at least TAM should be a one bit others you cannot do anything. So, therefore, this serial port is mandatory that one each of the scan each of the pins each of the pins in this core has to be access at the serially otherwise if the testing cannot be done. So, this port is mandatory this serial access each port will be access serially and they should be a control, but which going to speed up you can also give parallel access.

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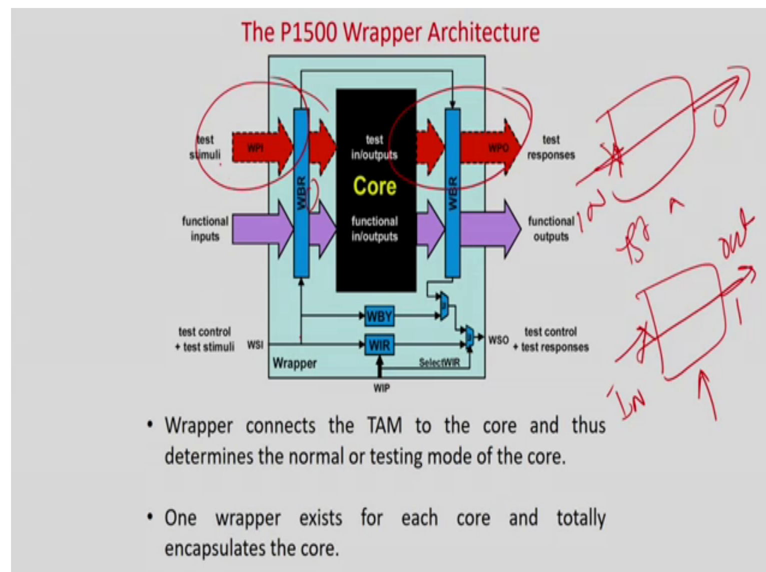

We will take more elaborate expansions which will be taking it clear. So, this is basically more elaboration on your this one on your core wrapper design. So, this is your core. So, there can be test inputs and test outputs these are the parallel that is again optional, but

this is the functional inputs and functional outputs will be there. So, sometimes what we do is that, we generally it is a single may this is the inside the core generally this is a single line they have show in blocks this is multiplex other we will give this or we will basically give this. So, basically why I am saying this is a optional because then your TAM or test time mechanism should be also have parallel it should be able to give multiple test vector simultaneously, but anyway let us assume that we have parallel access is provided. So, basically these are 2; and this is a WBR is this is your boundary wrapper boundary register this is like your scan this is the multiplexing arrangement with a scan I will show this figure of this is something like something like this.

So, either the mode the test data can go from in this direction is the test data and this is your input normal input and this is basically your output. So, the output is going to the core. So, this is testing. So, just if your single way of single mode application if it is in that manner then what is going to happen is that, I put another register another input to the core and this is your input another input line.

So, this is your scanning. So, maybe I have to give a value of 1 0 as the inputs to the core for testing. So, I will as your scan mode so, this one will be disabled. So, this one will be disabled and this one will be disabled test mode. So, I apply a 1, apply a 0 as a boundary mode it will come and apply to the core. But so, this is a normal serial mode of doing just like a scan. So, use apply the scan fill the scan chain and apply the scan chain has been applied. So, you applied and do the testing, but again while normal mode of operation basically. So, what is going to happen in normal mode of operation? This scan chain will not be unable; so, this one will not be unable basically and direct input will be going over here.

So, there about there is a multiplexing arrangement in the boundary register. So, either normal or parallel or normal mode so, test data can be going in this mode right and test data can be given out this mode right. So, this one I show shown is, so this, this is the test data can be given this is the serial mode of bring it by that is what is the idea. So, I can either configure this registers to go the this is the functional mode and an in case of test mode what I am going to do is it is a serial mode, the values will be travelling in this one and maybe I require a 1 over here, 0 over here.

So, the serial I will be apply and this functional input will be CUT in this manner basically something like this right and then basically the output will also be appearing in this functional output and it will be scanned out right. That is actually serial way of doing and parallel allow with this you can access if the TAM has multiple parallel ports. So, you can directly bypass this scan registers and you can directly apply the test patterns maybe something like this if I take this figure it will be clear.

So, maybe as I told you. So, here I am putting all the values or probing all the values sequentially, but if I have some 5 parallel lines over here. So, I can directly apply this 5 as a internal lines direct values I can put and I can do the test apply the test patterns in a much faster manner. So, that is actually these things are corresponding to the parallel access right, but serial, serial is the simple one. So, wrapper connects the TAM to the core and thus determines normal or test mode, one wrapper exists for each core and totally encapsulates the core that is what is the idea ok.

Before I tell you there is a 2 very important registers one register is called the WIR which is the instruction register that is what I am told you; that means, here the instruction this is very simple just how it is a decoder. So, what it does it tells when this has to be applied. So, accordingly the multiplexing arrangement in the buffer boundaries has to be changed, whether you want to shift it or whether you want to access by this mechanism, whether I have to give this as a output, whether I have to give this as a output. So, all these multiplexing arrangement for the W buff means boundary registers has to be modified and further they something called the instruction register.

So, you give the values to the instruction register and accordingly it will select in what more the basically this buffer register has to be in. There is something called a WBY is a bypass register, why is a bypass register important, because maybe I do not want to test this chip we can I will take this example to be cleared. Why this is a bypass register, why it is required maybe I want to just access may be this point and maybe I want to access this point.

So, should I transfer these values in this manner and then come over here and apply long time. So, basically something called a bypass mode in bypass mode what happens basically. So, it is not shown over here. So, bypass means data will not flow over here as it will directly come over here from near it will be coming over here. So, basically from

the bypass it will come over here, bypass means it will not go around it is a bypass way. So, you do not because I know that I do not have put test the chip (Refer Time: 40:51) bypassed it will be coming over here it will being coming over here. Then again is bypass because I am not going to testing it will again direct come over here and then it will going to test this part.

So, bypass means I do not have to scan throughout this. So, that is something called I can go around instead of going around directly for the test pattern I can directly send it out here. So, this is called the bypass register.

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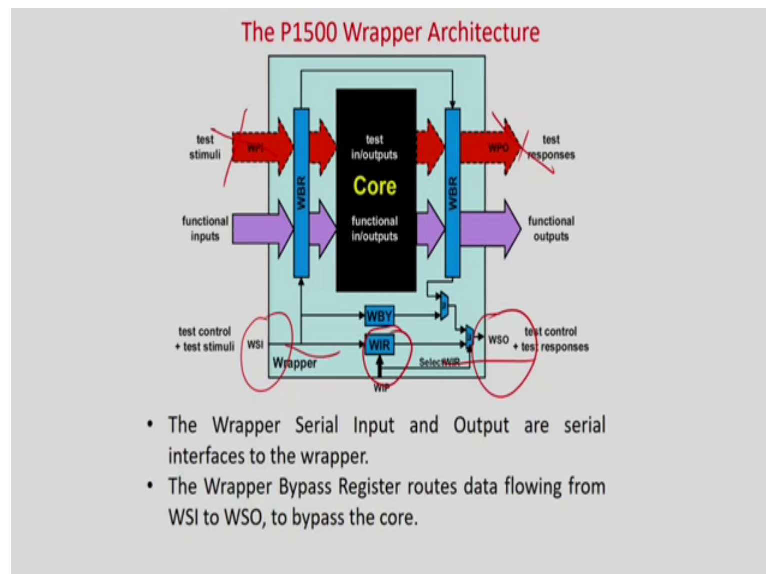

So; that means, if you have to scan through all the chips all the cores in the die it may take a long time to that or not required also at every point of time because maybe already 2 cores I am interested. So, some of the cores I will directly bypass. So, instead of going in the round about direction basically I will directly pass the chip as I told you not by this direction I can go about by this ok. And then, one more important thing I should say and how to give the instructions etcetera or actually in a serial mode, because already it stored that at least the serial mode of access to all the chip force will be through the wrapper must be available parallel is the option, but sequential is must.

So therefore, all the instructions are given as the serial mode, the wrapper serial input outputs are serial interfaces to the wrapper. So, this wrapper basically this instruction whatever you are going to give, even if I want to give the values individually this may

not be available. So, in this case the single bit transfer so, sometimes will be giving the instructions, but is a in a all serial mode this also of course, there can also be a give the what I say you can also I have been some of the cases you can also have directly you can access this instruction register in a parallel mode, but as I told you in most of the design by standard 1500 they keep try to keep this the instruction providing in a serial mode, because the instructions are not very large in length because instructions there are very simple control instructions instruction register in this case is just a decoder.

So, for one mode it will actually make the chip or registers go in this mode in one mode it will be allow it to go in this manner in some of the instruction it will may be allowing to directly go by this bypass register. So, it is just a decoder changing the multiplexing arrangements. So, that is very simple digital design. So, in this case the instruction register is nothing, but a simple decoder and the instruction lines are also very very less because the instructions are very few. One more thing I am not go into the very details of the protocol because exact the what are the instructions, what are the names of the instructions, what is the input code for that that will actually make the lecture very very monotonous.

So, after looking at this lay means basic architecture on the basic explanation I am going to give you, just go to the a triple E standard I will give you the reference you can read it. So, it will tell you the exact code what is the value of this instruction for this, what is the I means what is the instruction binary value for this instruction type, how the multiplexing arrangement changes, you can find out in this standard, by repeating it I will take a long lecture and it will it will make it very very monotonous.

Because telling a standard is just like reading the newspaper without any means I am without any kind of a mean whether it is just a news means I am what I am trying to say is that standard means go to A, then go to B, then go to C is just like telling you what to do in a very clerical manner, but if we want to really right a 1500 standard wrapper then of course, you have to look at the standard and design. But, in this one our lecture what I am trying to do is that basically I am trying to tell you, what is the basic philosophy.

So, that after that you can easily go and read the standard you can better have a better appreciation of 5 standard was design like this what are the fax etcetera why. So, this is a wrapper. So, in this case as I told you this is bypass register so, if I sequential input and

sequential output there is mandatory that if parallel interface is not there still serial interface must be there. So, you can apply the test pattern and you can observe these test pattern along with that some instruction which I am going to give it to is also in a serial manner. As I told you parallel access may not be given to you. So, there therefore, by standard they have called WIR or the instruction are give in the serial mode right.

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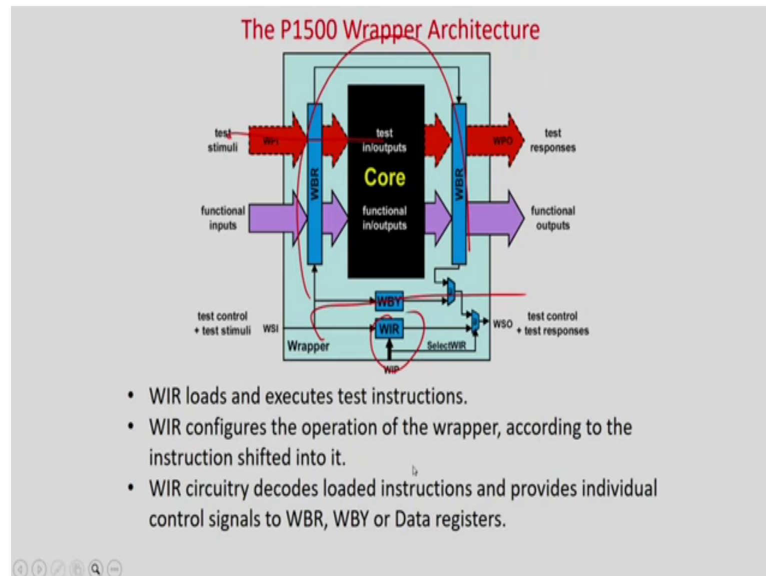

So, what happens, WIR loads the loads and executes the test instructions. So, it will load it and it will execute. So, instructions I told you with the functionalities very simple whether it may go around by this manner, whether you will allow this or, whether it will bypass this particular core is taken is taken care of by this instruction register.

WIR configures the operation of the wrapper according to the instruction shifted to it; that means, the in instruction is given in the serial form and after the whole instruction is shifted it takes the action. The WIR circuitry decodes the loaded instruction provide the individual signals to buffer register, analyzer and data registers it is very simple idea.

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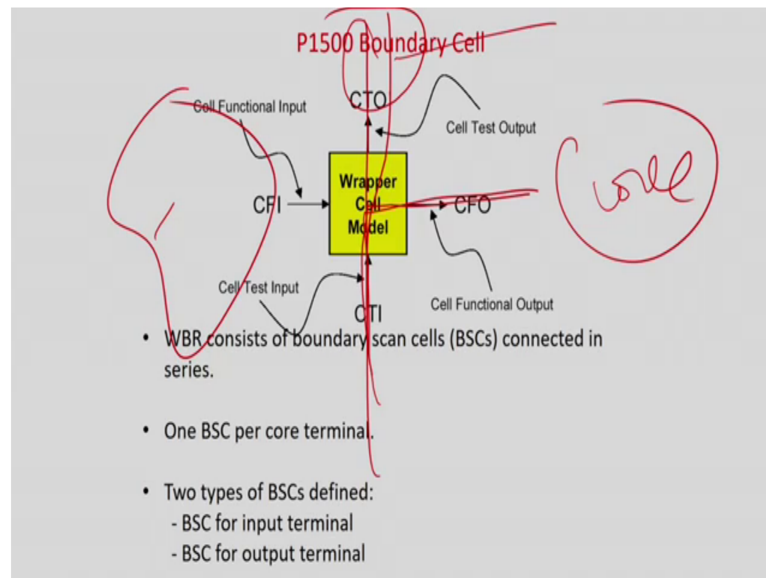

And, as I told you if you ask me how this cell looks like so, this is the scan input scan output to the wrapper cell boundary cell or you can leave it as a test input, this a normal cell functional input, cell functional output; that means, it is something like this is going in and going out.

And basically this is what is being scanned and going to scan output. So, if you want to give a test pattern it will be in this manner, if you want to give it to this is the core, if you want to shift some test pattern this will be in this manner, if we want to keep the test pattern basically. If it is an IO pin directly like this pin like this point if you want to access something you need not scan in the value here you can (Refer Time: 45:41) as the output, but if you want to give some test value as the this pin if have to scan in over here. Accordingly you an easily appreciate that I can actually change this module.

So, if I this is the input or output pin you can directly give the test output pattern here or you can also give directly the normal input output pattern over here, but if we just to be a if it not a input output pin may be discovered by some other core then we have to scan in the value and you have to apply this one. So, simple standard multiples arrangement as you can easily appreciate there is some multiplexing arrangements to do it. And again this if want to go to the next boundary scan value boundary scan register or the called the wrapper boundary register so, it will be again scan will be passed over here.

Same thing like a scan chain only thing is that it is the applied to the core boundaries rather than the internal points of the chip, but as I told you why they called it is a standard, because as I told you multiple course will be purchase from different vendors they will have the wrappers and I will put it; and I have to go for test. So, if everyone does not follow a standard and make there own wrapper, it is very difficult to the boundary it the integrated test that is why we maintain a standard. Otherwise it is very very logical and we have to do it in this manner, but standard makes it very much fixed and I know that if they are following 1500 standard then this is the instruction, this is the bypass, etcetera, etcetera, etcetera. So, very easily I can design my tester integrity.

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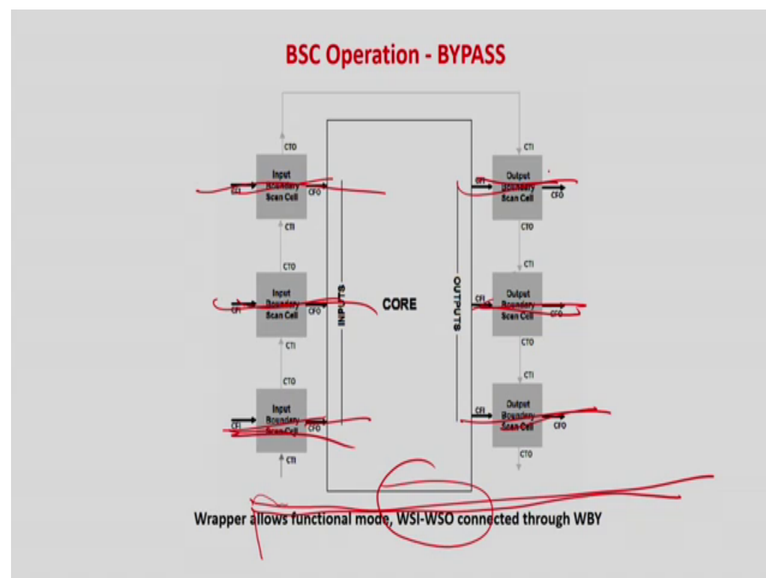

So, one of the very basic type of lot of tests are possible one is called the Bypass, means what are different modes in which the boundary is just operate first is call basically bypass. Bypass basically means wrapper allows functional modes basically the chip is working if we can see bypass.

So, in this case what happens I am this patterns are traveling in the this way you can see the internal the chip is working in the normal mode. So, inputs are coming from the input output. And this is going to the output this is normal functional inputs and functional output. That is either the chip I am not inserted in testing this core or it can also be happing that basically this opening the normal.

So, I am this test patterns will came over here and through go through the bypass register it will came out, you will not be scanned the distance of the half count is reduced. So, it can be very and what basically happens in this case it will be multiples arrangement it will be disable all this scan and direct connection with the made. So that basically changing of the multiplexer control will be taken care by for the instruction register decoder.

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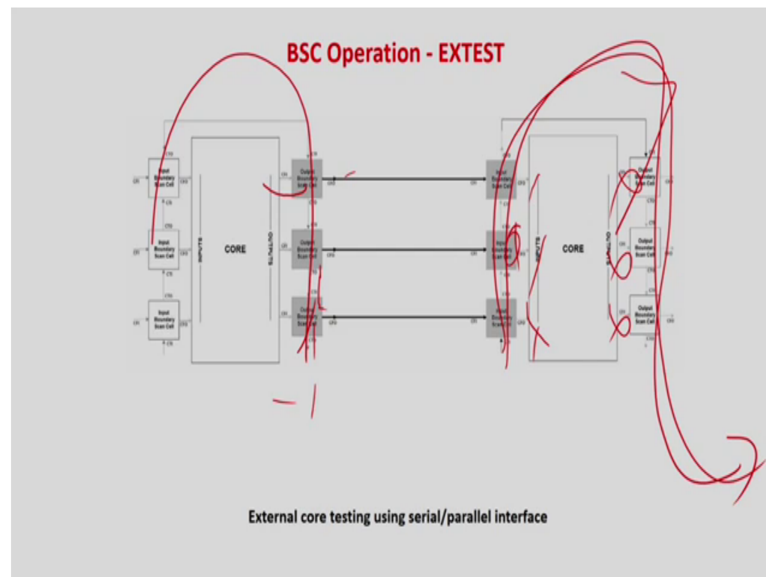

Another very important EXTEST so, this is the functional mode this is not actually at test sorry this is a functional mode not a (Refer Time: 48:02) test (Refer Time: 48:04) in the EXTEST. Because this is what I have purchased this, one I have purchased now I have made these interconnections, how do I test it? Testing is very simple you apply a 1 get a 1, apply a 0 get a 0 that may some (Refer Time: 48:15) values can also give like 1 0 1 alternate, because there can be inter face into the lines, you can also give something like 0 1 0 1 alternate values.

So, that if they can have interference both this can also be pulled there can be bridging for between these 2 units. So, there are lot of we have testing the interconnect, but the basic idea is that you send a 0 receive a 0, send a 1 receive a 1, you send a 0 will get a 0, send a 1 get a 1 all of that has to be verified, but sometimes I told you sometimes you make different pattern combinations in the nearby neighboring lines.

So, that you can test for bridging falls or interference falls like one pattern can be something like I put a 1 1 1 here then a 0 over here assuming the fourth line to be there. So, in this case all these ones can try to pull this 0 to that can also happen, but again test patterns are simple you apply different combinations and, but the analysis is very simple you send 1 expect it this one apply a 0 one this one whatever you said you are going to just expected at the output and it is very well known it is very well know by the test method or the model that for testing it what I should apply. May be just I can give you a example may be I will first step by all 1 1 and it expects all 1, then I will expect all zeros like it a 0 0 that is it. That is a (Refer Time: 49: 28) test, maybe I want to see some kind of a bridging effect then I will put 1 0 1 0 alternate and 0 1 0 this alternate.

So, both of these parties know that first it will give all zeros, then all ones, then basically alternate zeros alternate 1 and I have to expected in the output. So, that is what is basically predetermined my determine test cases for the external lines. So, in this case what you are going to do, this is actually called EXTEST. So, in the case you have to put scanning the values of 1 1 1 1 and then actually this in this case it will actually block 0 or block these lines initially it will actually get this lines over here and just do the (Refer Time: 50: 04) matching. So, in this case this is call a EXTEST.

So, EXTEST is one of the very important instruction which is given to takes the internal connections. So, this means you can scanning the values or if have a parallax given to be, it is parallel wrapper is given to be. So, directly they can be fade over that is the parallel access is given to be, then it will be faster, but as I told you is a not a mandatory requirement to give parallel axis. So, sometimes it can happen that you have to do it in a normal serial mode you can scan it over here do it in again scan the values are the output and you can analysis the response.

But if you have a direct scan out direct parallel output you can directly probe the value of the output and test it, it depends on the what speed and what overhead you give for the TAM So, here the TAM overhead will be very high because you have to give the parallel axis, but if your do not want a parallel axis that also fine you can take the values at this scan output and the testing. So, excess is very very important testing the external pins.

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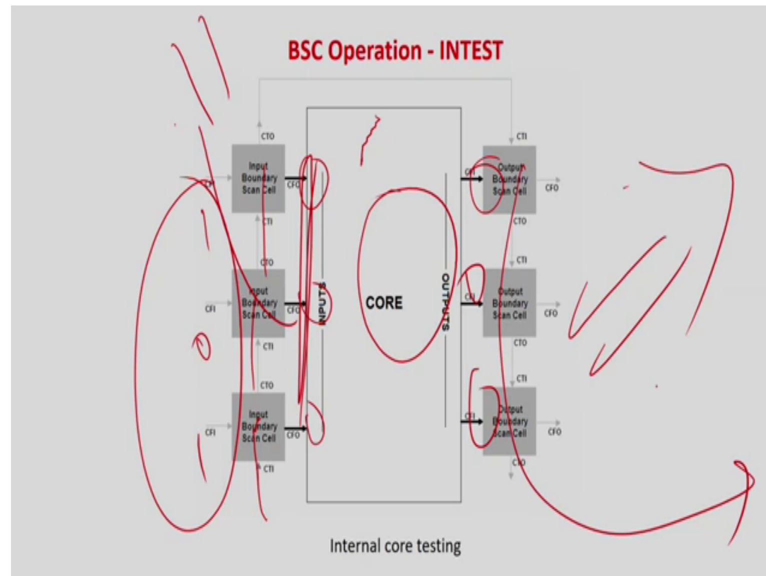

There is something called INTEST

Intest means you have to test the core functionality. So, in this case you can scan the values required one you give scan the values required one give scan the value required one you give means 1 0 1 to be applied for testing of. Now who is giving you the test pattern, very important point note that I have purchased this core I have no idea what is inside. The test vendor or who has manufactured the core will tell me that these are the patterns to be applied then your INTEST is done.

EXTEST he will not tell anything, EXTEST is my responsibilities because I am something EXTEST is simple have to just test the interconnects, because if I know that cores are operating fine by the patterns the core vendor will give me then it is only remains that I have to test the whether the internal lines are operating properly or not. Maybe I can do some kind of overall system functional details that is also possible, but that does not generally come under the P1500 standard. P 1500 is very simple you test your internal cores you test the inter connects more or less you are going to be done.

So, INTEST basically what happens the vendor will tell me the points. So, I will scan in the value there again get the values that the output pins in again I will scan out the values so, scan chain analyse them right. So, it is very simple again if you are here it will be a serial access, if you have a parallel port, then you can again directly apply these patterns over here and you can get the output parallelly by the parallel tag and your job is done.

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References

- http://grouper.ieee.org/groups/1500/index.html.
- E. J. Marinissen et al., *Journal of Electronic Testing: Theory and Applications* (JETTA), 18, 365-383, 2002

Basically this is what is called and this is very important these are the references basically this is first one is the when you can read this whole standard document and it is also appeared in a in the journal of electronic testing about this P 1500 standard.

So, basically we with this we come to the end of this lecture what we have seen over here that is very important, we have I have not discussed P 1500 standard line by line or the standard in a very very protocol in a very very rigorous manner, rather what I have tried to give you I have tried to tell you that what is the problem of embedded core based testing.

Nowadays most of the embedded system are tested in the level of cores, you buy the cores put in a single die go and manufacture it now you have to access this internal cores and basically test them. The problem is the internal pins or because the core test vender will tell you the input or output test level of you core, they will not they do not understand that whether this core will be put in the one corner or in the middle or how much observability or controllability difficulty will be there that the core vendor does not know.

Therefore, he will put a wrapper and he will tell you that this is how my core can be accessed because the IP it is an IP core (Refer Time: 53: 08) people will not allow you to give all internal details about it. So, they make a make a wrapper and apart from that the wrapper is also manufactured based on the 1500 standard. So, that you can take multiple

vendor cores and put it and test and try to access the cores in a normal simplified design protocol because everybody is following the single standard. So, you take multiple vendor cores because you know that all are following 1500 standard you put it in the die and manufacture it.

Now, you can you have to access all the individual cores for the internal testing as for the interconnect testing. Inter connect testing is as I have told you 2 cores will be there you apply a some values binary values over there look at the other end of the connection and you see whether the values are reaching over there or not. So, that is also called an EXTEST which is definitely has to be supported by the P 1500, but where you have the access the pins where there you will pull up the values are all very clearly written in the EXTEST instructions, but also you can have to do the internal test of the cores in that case again in very important the vectors are already told to you when the vendor you have apply it only problem is that how you apply that because the core positions are not known a priori when you are designing the entire die. So, therefore, you have to go by a scan method and you can put in this one.

So, therefore, this P 1500 basically tells you how to access the chips and how to apply the test patterns and basically how to bring out the values and analyze it. So, that tells a test access architecture is nothing to do with test pattern generation how basically an optimize is not like that. If basically multiple cores are there you make in a big die and put it there, how internally you access and test the lines and the internal that is all about P 1500 or core based testing. So, core base testing is mainly how to get access to the internal point observability or controllability.

So, this is one of the very important aspects which is coming out because more of the embedded system designs are core based. So, therefore because this the module are mainly talking about some of the interesting aspects of testing which are mainly emphasized for embedded system design. So, in that respect we were dealing in details with P 1500 standard.

With this we come to the end of this lecture. And in next lecture were will be will be going seeing more issues on some type of important issues of hardware testing mainly emphasized on embedded system.

Thank you.