Design Verification and Test of Digital VLSI Designs

Dr. Santhosh Biswas
Dr. Jatindra Kumar Deka
Indian Institute of Technology, Guwahati

Model - 11
Lecture - 2
Built in Self Test

So, welcome to lecture 2 of module 11 in built in self test. So, in the last lecture we were looking out or this case that with the assumption in whatever test patterns or whatever testing, we discussing at length were offline testing. So, what do you mean the off line testing has been fabricated and it is put in applying this pattern through test. Then, we also show that now what due to its micro design what happens even if the circuit is fine when you have sold it off when there it is shift to the vender shift, to the vendor to the customer, even to the system. It may have failure because of the micro design for all this soft failure design what you call.

You had the idea what has to test that to found out to develop a technique in which case what we can do, we can put a subminian major version of this pattern generator. A major version or what do you call sub sent version, this is component on chip, so everyday now chip starts the operation, what do you do you activate the test patterns generator. This is a miniature version with this and use a random dispatch this component to final this everything has got wrong.

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So, if you can do every start up of your circuit actually, we call it has up building self test, so in the last lecture we have seen that what we basically require in beast architecture. We require test controller, we require generator and its size should be arranged should be very less, so it is an on chip circuit, so that area constant is very high, so we have seen that the linear feedback can resistance in a standard way.

Using a series of simple example, we can easily develop an exhaust type of just like excluding the case of all 0 s, we can generate patterns from 1 to 2 minus 1 kind of the subsequent of the module testing. The area requirement is nothing but a single in a example of the last lecture. So that is much less than the case required by the generator that will like 1, 3, 5, 7, 9, 11, 32, something like that in the pattern generator like this so on. The chip circuit is very high because you have to go for the final state mission design or get up device. Finally, you can see a more than few excoriate which is the case in the standard feedback LFSR or standard LFSR or any other type.

We think idea is there in sure and then generation using linear feedback registers and much more area means much more area less in area compared to standard determination to generator to the final machine of approach. If you do because the low area requirement of LFSR, we find then a very good candidate for in case of built and selfless, so in the last lecture if you remember we have seen something kind of LFSR of this nature.

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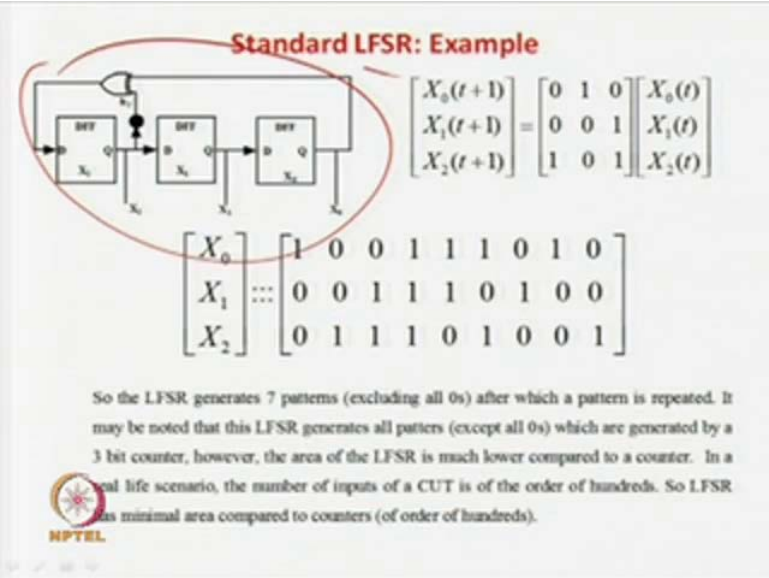

We call this standard LFSR, today we will see another type of LFSR about why do another type of LFSR whenever just we could get the motivation. So, what was the idea in that you can see that in case of standard LFSR there is a chain of excoriates if there is also another feedback from this excoriates. So, you require another excoriates over here this input will be there and this will be feeding.

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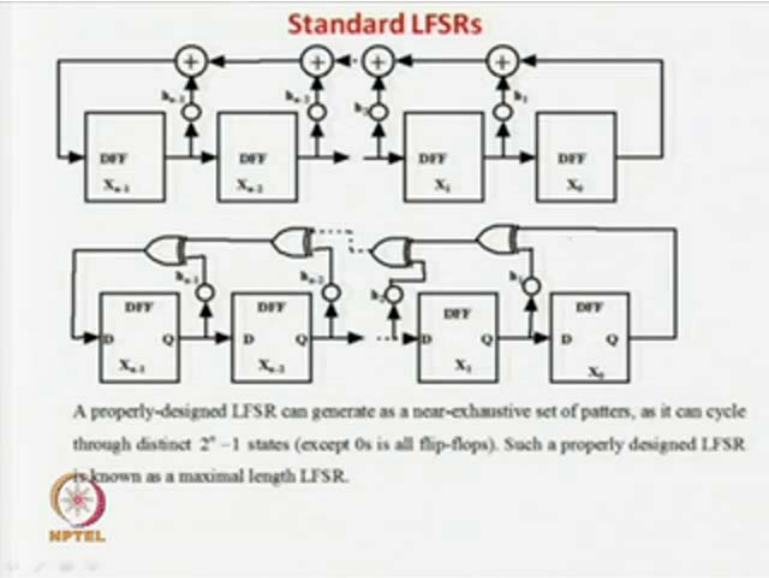

So, the delay may increase in case of LFSR because you have a very high number of excoriates, you can see if all the edges are one than 1, 2, 3, 4 dot n, h s or n minus 1, it is

of two input excoriates it would be this one. So, to avoid these delay to study a new type of LFSR which is actually called the modular LFSR.

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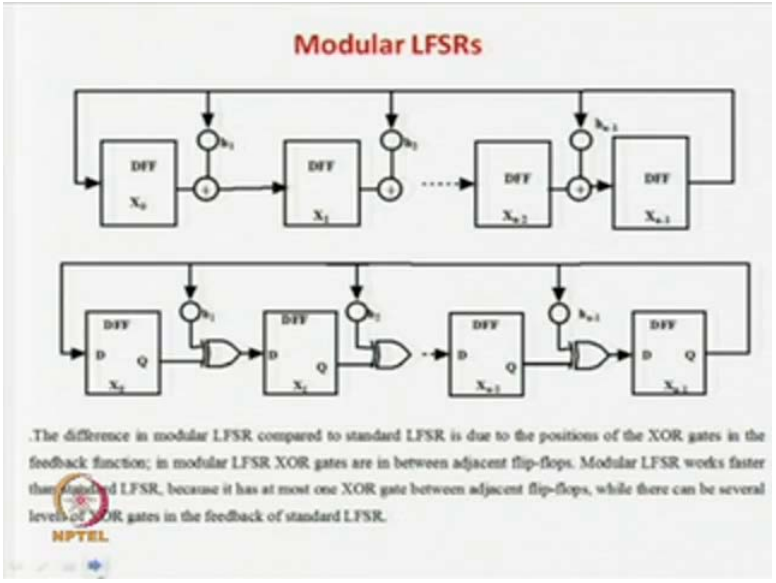

Then, we will see for the response compacted and all those things, to avoid those delays people have developed very kind of LFSR which is called modular LFSR. It is almost the same it wills also characteristics polynomial, it is also nearer generated random patterns and same thing the only advantage. You, will have here is, there will be delay will be less in this case the alternates in other way round no sequence are excoriates. So, in the case in the chain of excoriates are not there, so the delay will be minimized, so what is the idea here.

So, you put the excoriates as in the case of general LFSR, a chain of I mean if you remember the standard register we have direct connection between these two and this feedback to this. Here, actually involved a lot of excoriates that actually cause a deal, but here we are not doing the averages would be different. Here is the direct feedback here and each of the inputs of excoriates for deregister than either use of feedback from this.

This may use a feedback and if h minus 1 is equal to 0, then is to direct connection this feedback will be not in used if this f 2 is not one side, then this feedback will excoriates. This is how the basic architecture how modular LFSR, so in this case you have seen in modular LFSR this modular LFSR due to the position. So, the helix LFSR excoriates, so the helix LFSR excoriates in the delay between this one and this one. In the previous

case, the lot of excoriates are here, delay compact the output of the last from the first kind of start.

So, to avoid this we have to now move on this lecture, in this case we have actually only one you can this one excoriates in the input, so the delay are in less. So, in this modular LFSR, it will be one excoriates, so these LFSR works has a LFSR the adventives, LFSR of the other one it can be a lots of feedback in the standard LFSR. So, that is why we are moving to what do you call modular LFSR.

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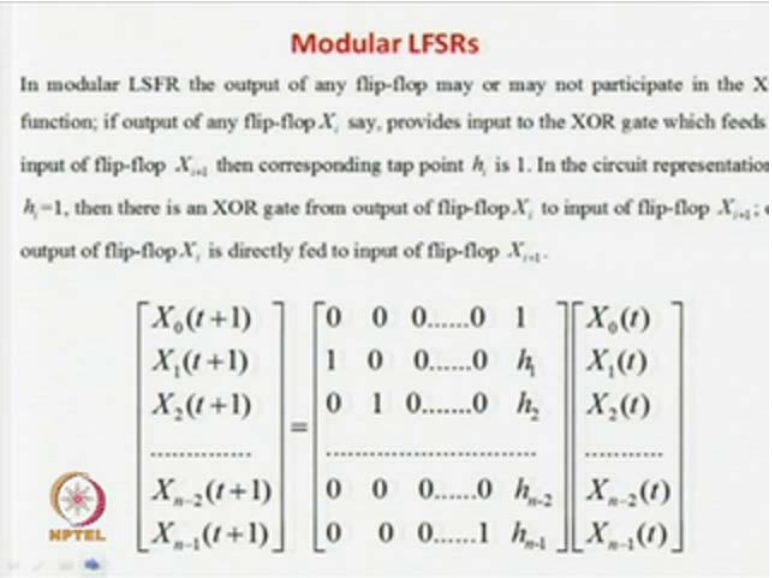

Now, we will see just like in the previous case the matrix are definition for this and we will also have what do you call this characteristic polynomials. So, what is the case, so in this case also you want the feedback, then here one thing is there you have to remember is X naught input of X naught is equal to output to X plus 1 that means if you say that X naught t plus 1 is nothing but equal to a X naught n minus 1 t. That has to be n minus 2 and whatever would be the value here at the time t here the value at this one value that means here t 1 s 1. So, in this case you can also see here that if you can see that this one is your deco our matrix, so this is X naught 2 X n t plus 1.

So, this X naught, so first you already know that if the value of X naught t plus 1 that is X naught t plus 1 only nothing but X t n minus 1 t naught because these are the direct connection from here to here. So, that is what the case is, so X naught t plus 1 that is equal to 2 all will be multiply with 0, 0, 0, 0, only this one will be there. This would be

like this one together X naught t plus 1 is equal to nothing but X naught X minus 1 t that is why this last column will have 1 here.

Now, next we can see is how can you develop the expression for X X 1 t plus 1, so if you see X 1 t plus 1, this one is what X 1 t plus 1 will depend on, what it will depend on this one means it will obviously depending on this one. So, you will be what it will be X naught t X r, there will be an X r, it will be 1 is 0, then it directly depends on the direct connection. Then, it will be nothing but X 1 t 1 X 1 t plus 1 is equal to X naught t, but in this case X 1 is equal to 1, then this feedback will also come, then we have to put what is that X n minus 1 into t naught.

So, into t previous t, so in this t naught, so it is t, so there than the feedback will also be coming to pictures that is X naught X 1 t plus 1 is 1. It is nothing but this guy will be there, so one product will be 1, so it will be anything X naught t X r. So, because this one will be gone this one will be gone, product will be 0, everything will be off because of all these 0 s accepting this each one will be there, it will be h 2 1 dot X n minus 1. So, way what do you say that so X n minus 1 is feedback will be considered, it will be each one is equal to 1, else it will be direct feedback from this one.

So, h 1 is equal to 0 is to be considered, it will also be gone, this one will be gone, so X naught t plus 1 will be nothing but only this first product X naught t plus 1, sorry s one plus t plus 1. This will be nothing but X naught t only this one X naught t will be there, you can develop for everything, so just like let us also look for another flip flop in between. So, in between we consider this is X naught n minus 3, you can consider this flip flop there, it will depend on X naught n minus 4 and also the feedback. So, we can look at it, so if you can consider X naught say X naught we can consider this one.

So, it will depend on X n minus 3, then the feedback is equal, so it will be dependent on here, those things for this thing one over here, so will be depending on X n minus X n minus 3 will be there. So, this will be if you consider this to roll 0, 0, 1, 0 h 2 will be that element, so it will have something X n minus 3 of t will be there. So, X n minus 2 of t plus 1 will nothing but this will be there, this product will gain these, and all other will be 0. So, it will going to X and minus 3 of t, then f to use X art, then this will go on of because this product with the 0 will go on page.

Here, X naught a X n minus to product of this one, so is will be X n minus 1 of t, so depending on weather 80, this one is 1 or 0, so this factor that means two factor that is each n minus to product that of X minus n t. They will depend on this value, then there is have to be X are this one is this factor and each n minus 2 is 0, these will not be there n minus 1, 2 will be accept n minus 3 into can be extract duty. So, that is what is the updating of day, so the each are 1, so that is dependent on the other extract with the extract with the feedback of X minus 1.

If this corresponding X is 1 else is 0, so the very simple, this thing very simple test, so this can be represented by a matrix format as labeled in c. So, this matrices format here is you have a diagonal matrices are over like this this row here all 0 and it is 1 and here corresponding with the similar route to this are the character standees of a.

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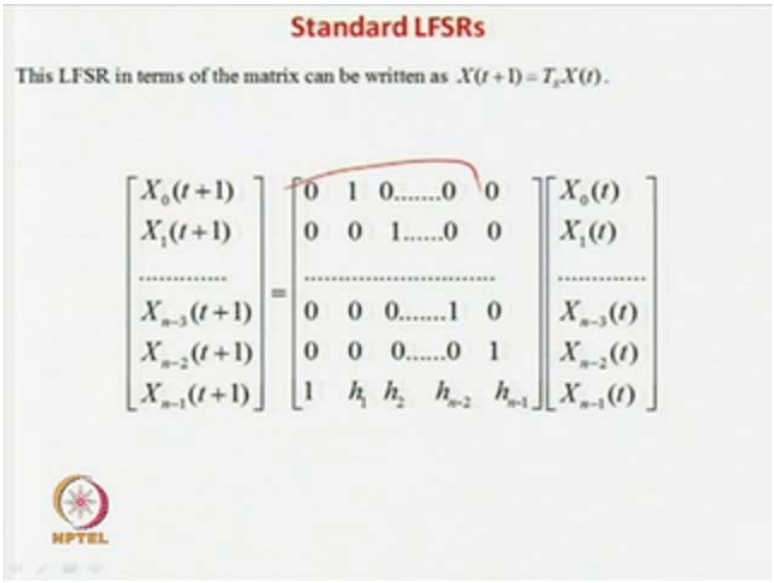

If you are look this is also having a similar step, but everything as rooted this is your standard diagram metrics and this one is all 0, sorry just a minute here, this are standard LFSR already giving discuss in the last class. So, this is your diagram matrix, this column with all 0 and you want be one and these are with this, so this you will consider for the module. This is a LFSR is nothing but it is big round up, something has been rooted kind of nothing but what was they doing actually equivalent nature, but by using this type rooted guide of an architecture.

Then, they deal between this this top this top because we have only one for getting between. So, that is why we are move to something module refines because of the dilate constraint which we are wading in case of module refines compute to standard (( )) whatever told you what are in the text. So, in modulating output, any other function if the output any prefer excides provide to the input X r forget with the feedback, then corresponding h is 1, else it is a 0.

So, whatever we discussed that the output of one will control through output of the output of one will control of another output, but if you depend on the feed because of X minus 1 corresponding, it should be 1.

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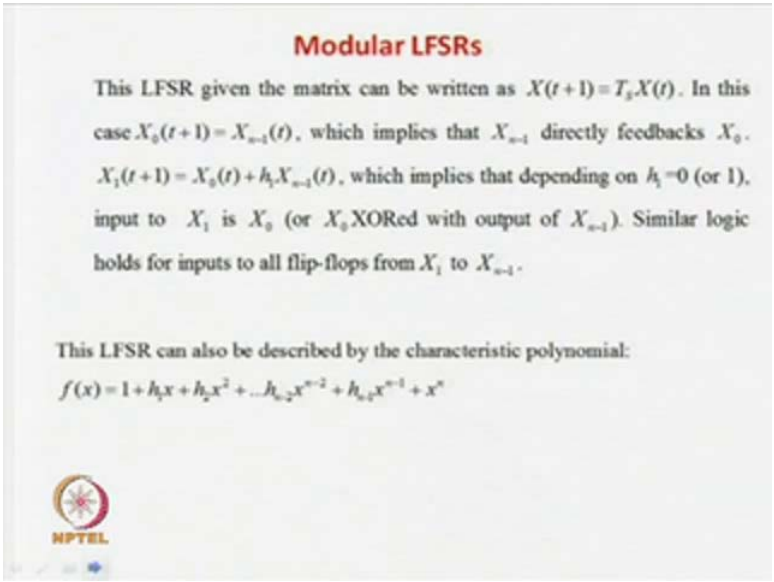

So, that is not actually as return label here, so I mean again this equation this X will be equation. So, X t s is this metrics is t of a it is the next with the and you will have a flip flop and this is the present value of flip flop. So, this is what in the case, so already we have discuss about how do you get this equation and again this is your characteristic binominal f X will have 1 and X n this is depending on the last term. You will have this values depending on the values of h 1 and h 2 naught n minus 1.

It will considered as a, so based on you can get the characteristic binomial as same in the case of standard. So, only difference is that, so again not of theory exist as we as we discuss in the next class a lot of theory exist find out this characteristic binominal generate a complete set of random patterns weather you can.

Actually, weather will not and also the case weathering it may not available generate to go those things a lot of curry exist that given a page characteristic polymer like that is lot of analysis which can predict or which can say that. This can determine that if any modulator has have this polymer characteristic and will be generate here exist random of patterns stooping all 0 sometime here.

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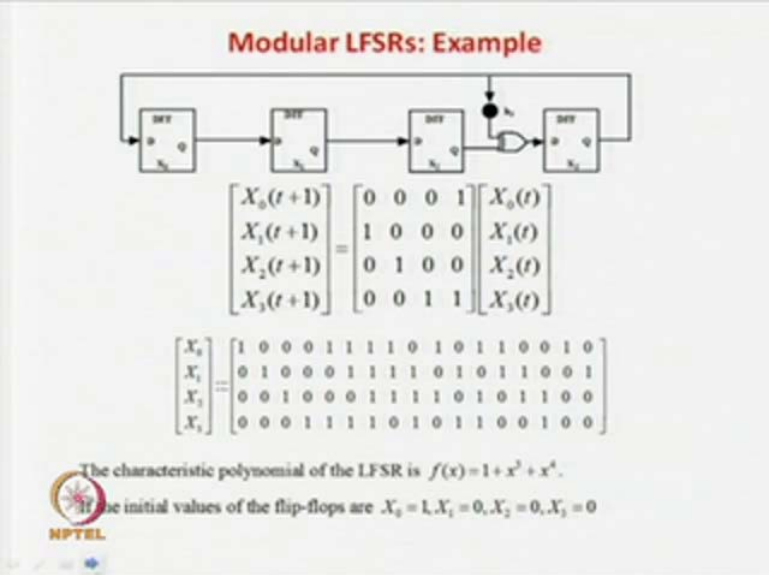

They are also existing some characteristic polymer which not generate, they also existing some pattern. So, depending on requirement you can see that characteristic polymer and how to select characteristic polymer is based on whether you feedback required and for extracting requirement use on possibility. In this example as in they are not to use this, so required to all this from exceeds of a flaw of curing part of this from the other sequence. Here, in the characteristic binomial it will be 1, 2, 3, 4 polymer will 1 plus X 4 plus only X 3 is 0. So, it will be h 3 X cube was this is one and you can eliminate this is one X cube plus X 4 this X 3 and 4 already there and X 3 equal to define factor X 3 comes here use as a X 3, 1.

There is no product like X 1 X square because in this case this gets the 0, the X are 0 they involved from this characteristics laminar, now they exist the literature. So, you can find out these characteristics, we are exacting certain pattern, so in this case you will get it find out the these characteristics per this phenomenal generated for exacting set up patterns. Now, what you find out than another thing which depends as in the case of

standard got them important is actually call the seed vector seed means what is the initiate reset values.

So, depending on the next series of I mean you can have the series of fees like also the in prevent you from that. So, you can have these are the seed vector than you start from this one and you can have any other set than you have start from the part that are vector and use an very important find out that how do you seeds were vectors. Then, actually for example, you can set these are there, therefore actually from test table case, so better I start from this one very quietly. I will from here up to get if you that protesting, then I will again say back here this will said seeded, but if you are very important if an important pattern are this one.

This one an obviously you start from this series get I forward from here and you will start from here. So, what is the idea seed I will tell you where to start from and what is the sequence of patterns. So, obviously we will try to such the seed vectors, so you can get the requirement patterns we keep for test and sequence what was the idea. So, what are saying that is already case some existence what are the stand, we are said to this it vectors such vectors. So, the very quickly requirement patterns in this case that may be important vector.

So, given these are the seed vector, let us see how it happened, how it gets this pattern same example in the previous case also, he has used X naught is 1 and other as 0, so this is servitor sorry this one is the seed later, this one is seed later. Now, what is next how do you about it know that this is our diagram active, so this is there and this one is all 0, so first one you keep it as a 1, that is already there and this case X 3 is 1 X 2 and 1, 0 and you get 0 and here put a 1 because X 3 is a 1.

These develop metrics, now you as we know that here X will not determine X 1 X 1 will determine X 2 X 3 will determine, sorry X 2 will determine X through naught, X will determine X 1 determine X 2 will determine X 3 and X 3, sorry this one.

So, in this case X 1 will determine X 0 determine X 0 and it is direct control, it is no feedback require if the feedback given into picture, so X 1, X will not control the X 1 with the feedback. So, in the case we can directly say that X naught is controlling X 1 with the no feed back here. So, we can say that X 1 is controlling X 2 and in this case

with the feedback, so X 2 is controlling X the feedback and then directly again you say that this X will directly controlling one case, this is no feedback.

So, X involves direct control here and actually from here to here and confirm here to this the control are the control involved and exhales than, but in this case there is no feedback. So, this is the aid control and this case is the feedback there is the depending control from X 2 to X 3. Now, you can see what happen in this case is very easy, so delete with the seed vector, so this is one there is a 0, 0 and 1, 0, so 1 and then 0. Then, 0 and 0, these the case after the next situation what will be the case we know that so this was control here is in X control and these the control is so obviously this value is come here, this value will come here the third value will come here obviously.

So, this one this value is coming here, this value is coming here and this value will come here, obviously we can X r condition. So, in this case what happen, so determine the values of X 3 to the X are 0 with this 0 X are 0 and we get the 0 over here. Also, we know the X directly control X 0, so this value will go here easily we get the vector of 0, 1, 0, 0. This is the case, these are very control direct this case no dispense are in the case, so there is this X 2 is controlling X 3, what we get X are this one.

So, in this case X are 0, get the 0 and this one directly feed back over here, so we get 0, 1, 0, 0, so what is the next vector here, so this vector will be, but this is 0 over here. Then, it is 1 over here, 0 over here and it is again 0 over here, so these how you now we can you find out the next determined. So, in this case, now this one is the direct control this one is the direct control, so directly third value X 1 value of the X was 0. So, we get this value of the over here and then this is the feedback here, so we get the factor 0, 0, 1. So, it is the 0, 0, now it is the 1 over here and it is the 0 over here.

Now, we can see the forth vector, so fourth vector we can now this this is the direct control here. Now, this control from here to here depend on X r this value is X r 0, X r 1, we get 1 over here and this one is actual here feedback over here. So, we now get the here 0, 0, 0 and this is now 0 and this one will be 1 now.

So, this is what is here next based over here, so we can say now this one so same way you can find out this whole sequence of pattern will find out that that means started from 1, 0, 0, 0. So, after so many pattern, we will find out the they will happen, so count the 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 13, 15, fifteen patterns, so 2, 3 n minus 1 was the

excluding all four 0 is the existed taste of generated by using this characteristic of the matrix.

So, in this cause if you are an application were you have to generate 4, we have to testing generate and we assume that the where we have these three. We can say these three more important this pattern and this one, so what we can do in this, this is the feed value and they will pattern of this and we can say this and again this value these are an input the important this pattern.

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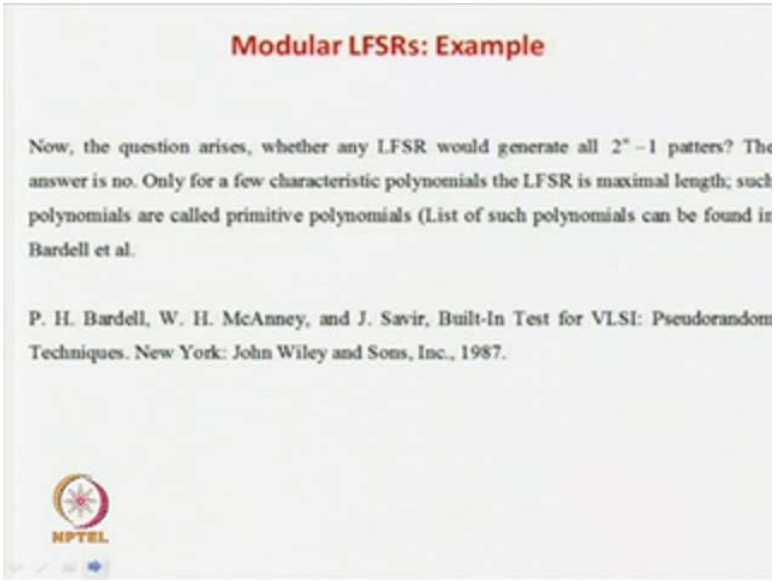

We can this about value, so see the very similar cause, so very similar cause modules LFSR as standard LFSR whatever you take the basic idea is that we can generate and state our patterns. The area over the very less in this cause of very only one X on this you get, but only in cause of standard they feedback in the last feedback in the first feedback (()). These are the feedback, the whole feedback in the first feedback to the last feedback somebody we can say last feedback last feedback to first feedback, so whatever in language feedback is standard LFSR sequence are LFSR. So, that was leading to some one r, so we lead for modular LFSR in modular LFSR which is also the same cause.

We can characterize for nominal, the characteristic is very nice way where ever the sequence of X r. You can similarly, generate for near is existed of pattern here, the delay is very less because in between one appear at max only on X r. So, modular LFSR has this all the feature that is sandal LFSR, but only with advantage are there is no extra

delay, extra huge delay. This was of the exchange of insoles, so again I was the discussing much time that all to the part of important actually answer is low. This only on few polynomials for which is then maximum length we are actually primly polynomial.

So, they are the least like this person why in this people we are in this least of such polynomial. So, you can have a reference that and to have that an design that which require existed that the new can about that characteristic nominal call the primary polynomial and we will be able to generate what you can call near elastic setup pattern. Some days may not be a huge set off the 2 minus 1 in huge of the set up pattern of, so in that because we can go facility other different kind of characteristic polynomial is may not be primary.

So, we did not generate the elastic set of patterns, you can generate very set of particular set of patterns and particular sequence and the depending on the charlatanic polynomial and whatever you can see the factor. You can get your design random aspects of generation according very low area cost, so that is the actually what you call and this is the senior feedback of the sit back in cause of best measure. One more measure he call to government in cause of distinct what will be it is a pattern generation. Again, the pattern generation cannot be a very huge area over head pattern generation because 8 is area over a pattern generation for automatic test equipments.

This is not at all concern huge equipment and can do that what whenever you going for testing all keeps will have on cheep a test past generation to this area of very restricted area. So, one of option you say one of the design mission of test pattern as we have done using just implementation and design of this, but the here the area of over will be very high. We have to optimize to number of gate by in this of standard of procedure, do you now the standard of the late of financial machine of the all the state and sequence.

Then, way of the find out the number of people in the standard of person of the follow, but you can generally find out the number of gain to the much larger than the an single XOR gate and sequence of single input. This is actually the number of the number of must larger if the deterministic financial machine to generate, but they milliner feedback to generate the modules sent. They are actually very much in this cause by using the single using of the by input if the by achieving of the number we can generate the design

characteristic polymer and the see that means give the see sequence of pattern the forgoing the testing.

The area of the extremely smaller pay to are what do you call with this, so that is why the all go for the LFSR with the design, we can design the LFSR the desire crinite polynomial, sorry I mean design whatever the characteristic has the polynomial. If you remain existed though you have the go for it for a polynomial minus the polynomial, say least can be fall in the people. If you do not require that, your design can have a kind of a characteristic polynomial, so that may not have.

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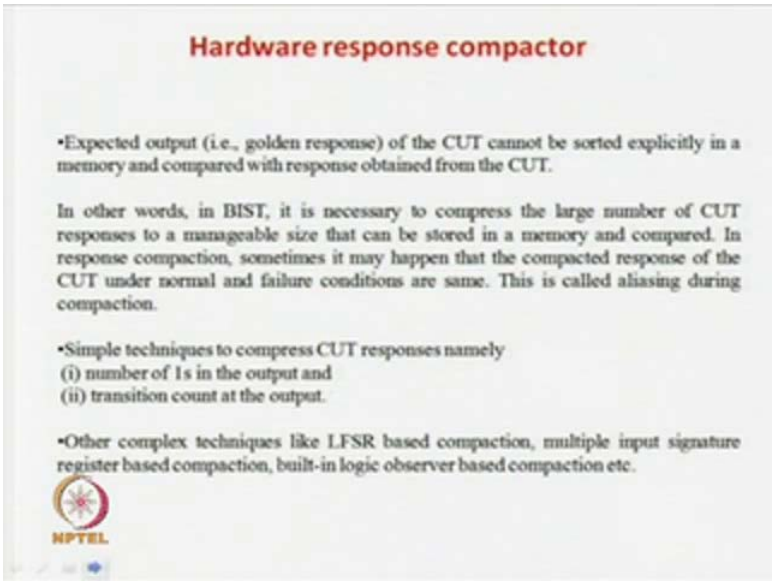

Again, if you want to say eclectic sequence of pattern this such a way so that you repeat of the discuss of that, so we can see select the see that accordingly a job this time. So, that is how design what you call the pattern generation is called the best using LFSR, now we second part of best design of the unique be set the components may be in components with the that is controller that controls this one. This is the standard digital of the fundamentals controls yourself of the design, next then was you the standard test for the generator which have already saw during the LFSR that is the modulate LFSR.

Now, they remain is the another part is an actually the response compactor and the response comparator that is the circular design generate some responses. So, already put that, so this input pattern that we now saw with this LFSR, what this pattern is and the generated by the circuit. Also, you can usually compute that what will the always

response for the circuit corresponding the to this pattern, these are the characteristic for a nominal and a design of what is the design. So, we are already the fabricated in the circuit, so we now that this is seated, we know the this is the cite, this is the sequence of pattern that is generated.

Also, this involved that the circuit of operating is the normal and the output response of that. We already saw the pattern of the related and that can store in the raw and coping, but now a seen because is ram is also a see the expensive components of nothing of on chief design. Then, we cannot the go for a flat design like you select the pattern from the test pattern of the generated that is the LFSR main for all these patterns. We expensively store the output of full response of circuit wrong, then you can the raw these are call flat design.

This is the pattern this is the output of the how does the story, you are pairing the wrong and compare the response is a compare flat design, but the RAM is very expensive here, also what you have to do we have to go for the compaction or compilation. So, that your RAM area is very small and you say, but obviously where as the compressing of the elastic of the pressure. So, we can find out the well some losses all coverage, but still the major requirements for the all cause was a in this cause was that will have to go for low area, but you can achieve that the other sends that that is it. I mean studying in the was lecture, so that is was the told you expected that whole time response.

So, I have already told you that the respected output response that the also cannot be sold that the because of the rise in the wrong. In other words, what he can say the in base it is necessity comprise the last number of the cards, I mean the cards responses to manager will the success of that. So, we can be told that in the memory and also who can the target should be there should not be any idea. So, it is kind of nothing, so that is if you do not compound, so we fall can be detect and if you compress it for may not be detected we will see expending is there an example. So, we will happen the compression of this called this.

So, your target we should the do the such a components, the alias in minimize, so that will be expending the for example, so that will be actually called that will be more clear. So, the simple techniques of components a lot of techniques of the find out the compression of the nous the compression of their huge, I mean the area in cause of the

communication and lot of thing. So, the lot of cure existence the compression and again recovery although things. So, that will not although be very simple and what will be the components techniques what is the numbers of one and the transmission count of this.

So, there are many other more other lot of the composing techniques like LFSR more composites multiple input signage. So, there are they may have the they are all part of the advance of the testing kind of staff so as in already discussion in the this course covered over view of testing verification in a 1 in a 1 who they are not going on this. They are the two basic very components of the compassion techniques and will be dealing in details.

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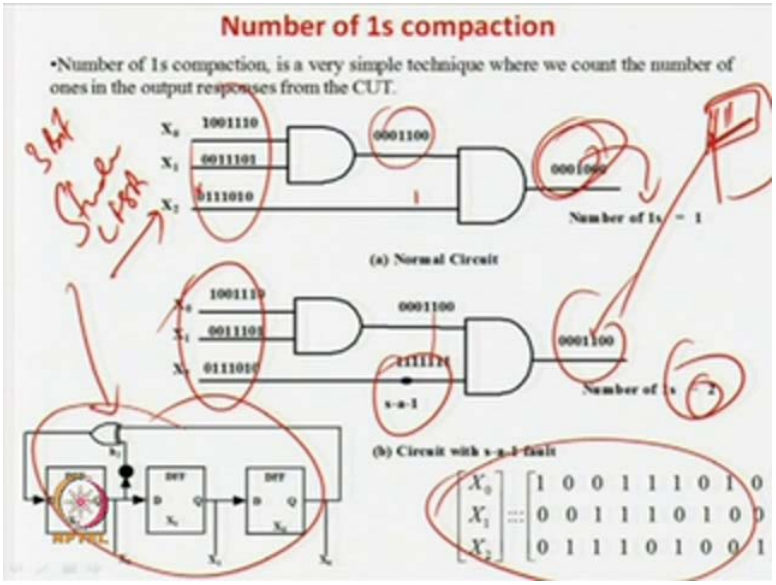

So, we will first see that the about the number, so number of own compressor, so what is the idea? The idea is the very simple it comes in the number of ideal output for example, the start with an area this as on the name of the technique will be count if the numbers of ones in the output of the circuit. So, now let us see compression, so the idea is there old we first LFSR, we are studying in the in the circuit. Also, we are consuming the first there is the standard LFSR, so this is the pattern of the generation. So, if we look at this consider pattern which will be the you are you this kind of the of LFSR, you just make the assumption so that assumption that the those pattern.

So, we can see these are the patterns of that will be generated that standard LFSR, so now we can these are input that the all LFSR, very important of testing in our the input.

Now, if you can assume the normal compression will be 1, 0, 0, so that will cause all the input of well like this 1, 2, 3, 4. So, 1, 2, 3, 4, what is 1, 1, 1, so only one cause will of the inputs are one all other is the answer is the 0, so if you apply the standard LFSR discussing the last class on the inputs this circuit your applied that will be this one all 0 s on a 1 and again three 0 s.

So, numbers of one in this cause is one what you are wrong will say that if you are standard LFSR give me the input from that one and the 3 bit of the deserve the if the standard LFSR last example of give in that the input is wrong. We can the normal cause have the only a single one, so they wrong will say now that the only one on this whole set of input, but if you are story what you can say using the flash stories and what will be the cause told this whole 1, 0, 0, 1, but assume that there are lot of the output. When you can assume that responding of the store in the wrong of this output, this output for which would large number, but in to the size of the wrong.

So, even if in cause of single be the output you wrong should store this whole value for this series of inputs. So, again this would take a wrong take as a, so we have done a compression a can, so what is the compression of like which is the number of once in the circuit. So, in the output in the case, so there is only one, so only one be there, it is requiring, now let us consider the socket for the one for the will again the all this cause of all one this is one vector, this is one vector be applied because all 0s can be applied.

This is our standard LFSR where using the characteristic polynomial in that, now this is socket, now that the for all causes so if you apply here the 1, 0, 0, the normal cause the answer sheet the 0 is applied in the normal case which would be the 0. Here, 0, but now at one more it the every time with the we will have the 7, now the because in the series of c 7 of the patterns of the 1, 2, 3, 4, 5, 6, 7, seven pattern is an applied for this.

So, in this cause every one of them should be a 1 about the one for now, this generator for the normal. So, we get the this value say that the game over here, but now in this case the previous case, I mean we got only a only a 1 1 over here. In this case also the see the one over here because in this cause we will get a because of these cause a of the intense of the are once get a will be number of once again the plus 2 in this case.

So, just apply all this cause the started with the second of the over here, so will the there is one more instance of this one more of the one I will get the answer here. So, here

number of the once result here, now what happens, apply of the theme of the pattern the wrong to the steps told one, but output response on the two 1 s. So, in this case for so in this case we can what are the requirements, the requirement is the wrong with this and single beta and the beta. So, it is one case, similarly this setup, and then we see, then other faults over here that we can the find out, but the so emphasizing.

So, you have done account the of 7 bitone, one bitone there is the number of once there was no ideas for his fault means why that is will with computation if the fault is there. It can be ejected their fault is not there, now press than more are with the settle will the example of the problem.

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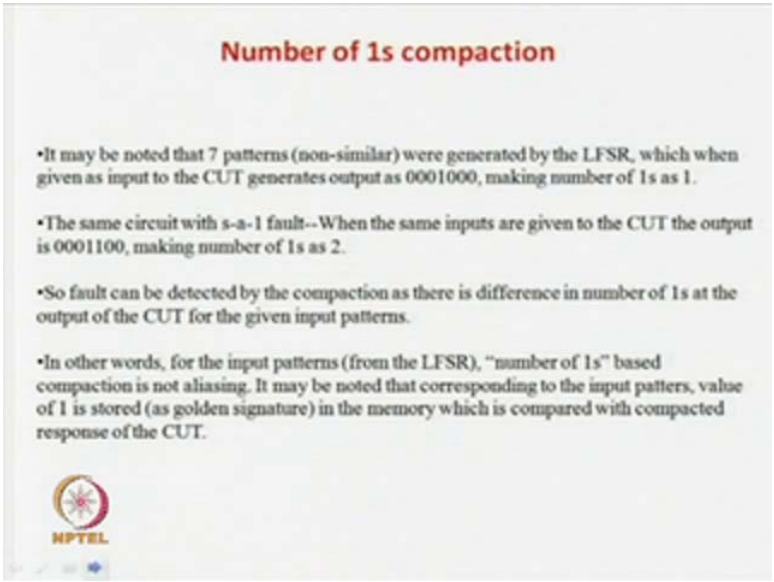

So, now just repeat the by Singh about him the compaction, so in the last seven that the non similar pattern, there is no temptation pattern employ to the LFSR me circuit generated this also to the number once. So, it the computation the same circuit to the for to the tool, so numbers of once, so as the difference of the numbers once of the flat is different.

So, we can say that numbers of one bit computation is non aliasing because in this in case the flat would be detected is non aliasing of the flat. So, it may be noted that the corresponding to the value to the fold of the signature in the memory which is compared with the response of the device. It is a single beat response compaction and the more important staff here.

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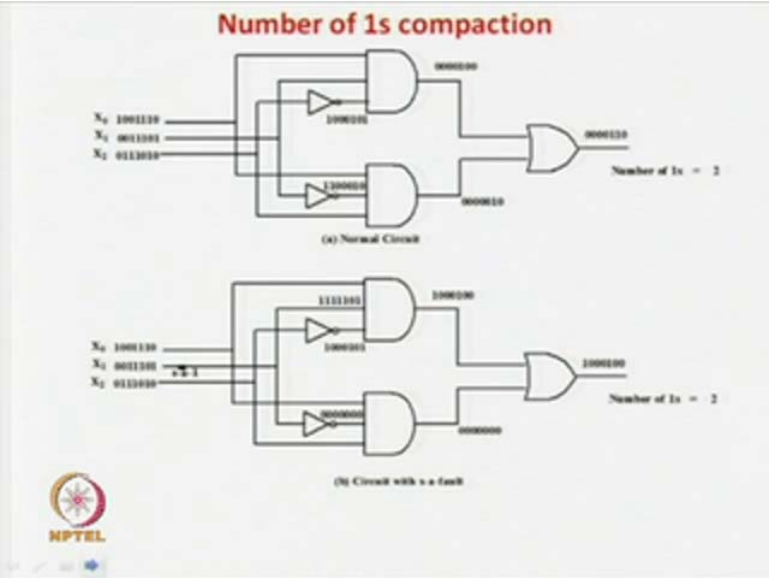

So, there was a no compaction in this file, so again, but now will see that not life is always as green always. In this case, we will see another example circuit in this case and the same sequence inputs are given like this one.

A circuit generating an existing set of patterns have 0 s, so apply this you can easily find out what could be the value is over here and find out the value. So, it will be 2, there will be 2, once in the case because to find out these, so this is one instance and the other instance the two instance will be output would be 1. So, number of once in this case is going into 2, now let us take a case where there is a unfelt over here to state one for here is all this case time. It will be all once be the case, so if you have 1 over here, 1 over here. So, in this case we will have always 1 over here and in this case here 0 over here.

So, in this case if you do so, now if you can do it over here, so just you can try it over here, let us make things more safe for example, what we can do here is that it is this. The pattern here is you can just say, I am just sorry, over here you can just say that pattern all over once because this one is connected to this over here. Again, we see there that those over and just it may compare of the values, so we will find out these are here, you can just compare out the values just computed. You can easily find out the 1, so because this is stuck advance, if it will be avoided, we can easily find out.

So, there will be two instants here, you can be able to find out, so again this case what happened, they will be number of 1 is equal to 2, there is actually what you mean by that

is then what happened is no of 1 s will be 2, 3 number of 1 will be position are different. We can very easily identify that number of 1 is also true if you are using a number of counting the compression. So, it will say that for this pattern the circuit is there, no false that is an area because fault over that is what called a compression that is it will say that for that pattern this circuit an area fault that is called as the compression that will be the counting the number of use.

You can see if I was told that flat represent of this one, so what do you mean by flat representation, flat representation means the hole which is told would an immediately called an because of the mismatch of the point. Then, also a mismatch this 4, 5, 1, 2, 3, 4, 5, 6 position, this is the mismatch, this portion one and this is the 0. So, you can mismatch in the first position and the mismatch, see this position, first position is the next six position is the mismatch 0 and one you have got it. Then, easily we cannot solve this part, but now because of compaction what has happened, it has gone about could not expert this part compaction, both the compact of this is the 2.

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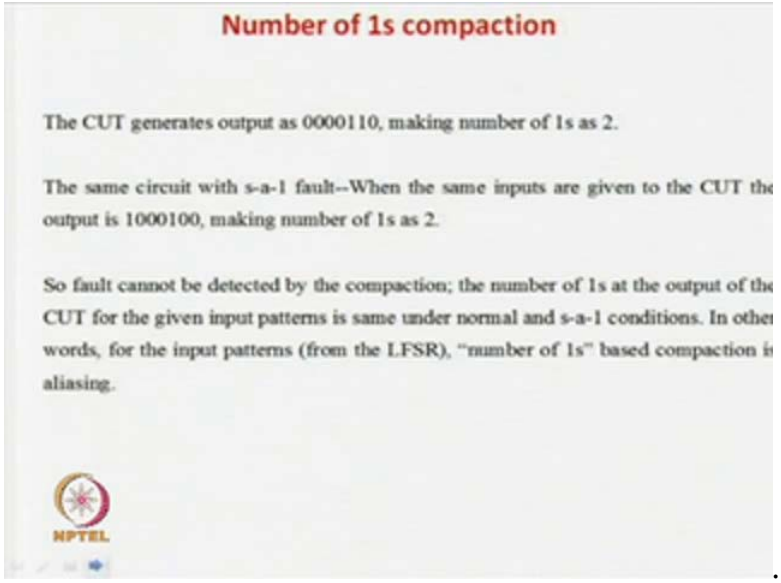

That is actually come back because loss the compression number of inputs number of equal to the number of basically 2 here. You cannot regent this vector as we cannot compute the loss compression and these are loss compression. For this, there was this, so that is what are you told is that now RAM which store only 1 bit information is in one

interior say information. So, in the case 1, 1, sorry 0 will comes store RAM corresponding to the value of 2 and it 1 store this belong flat.

So, that is the ideas belong value not require to store because you save several not only RAM, so RAM size is less what have to be would some of the part case that goes in the last case. So, what is told over here, so this is the output when the number to calcite to this is the generate will case, you can see the different in these two type both the case of to this kind of compaction cannot be detected in the calcite fall. So, that is actually called a that is for the calcite 1, 5, but any satisfied polynomial, what happened just become on the coverage, what do you mean call you fall coverage decrease.

So, we have find out reasonable because this reason what we try the very high amount fall coverage become, it has given in the most important falls are the falls, some part of give these not of condition, lot of congestion in layout lot of hot scorch. Further, the circuit is more hot kind of a thing, so you can enumerate which are the more dangerous area the areas were false, more time to the developed false are more time to be develop that we found out in history. You can find out from layout is also there see, we can find out which of these are more important pattern that require to be tested or more important false to be tested.

Based on that, you can find out which compaction scheme you have to use because if you are use a compaction scheme, it will reduce the area of your RAM, but at same time you should be you should understand the fact that they would be true. False coverage will decrease which type, there we will see another technique, we will understand that technique for one technique of false happening aliases affect and other for others.

There will be another set of false in that effect again, case of this counting one this false was this effect and what happened in the effect, I will take another example. So, you can say that what is that, sorry the compacts and technique accordingly and find out that what is the required coverage and which are the most important false on even to target.

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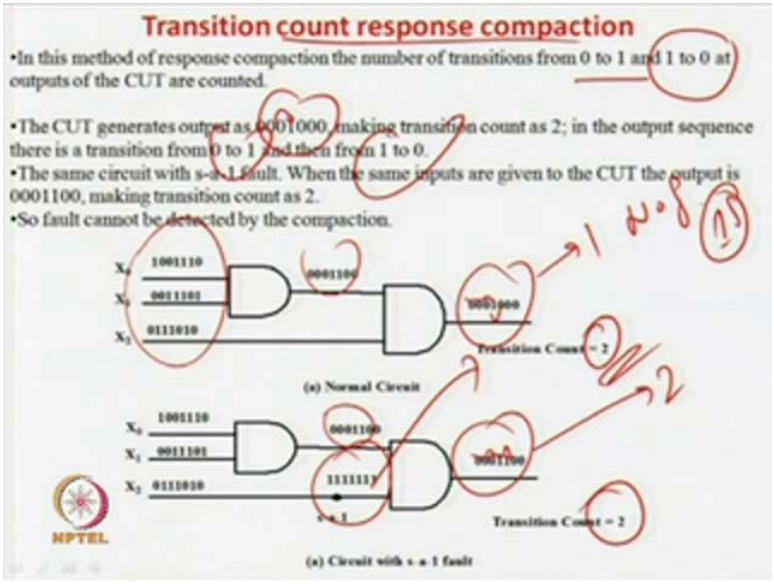

So, in that way I mean you can say you can get smaller ram size as well as you can able to get the good coverage for the important parts of the parts which are more developed in the circuit in operation. So, the important production technique which is called the transition count, so that means that again say same circuit you considered. So, these are the input usage and these are the output usage, so what is that transition count, transition count as a name say you have to count when it is going from 0 to 1an angle you have to say. Here, it is going from 1 to 0 that is in this case 0, no change 0 to 0, change 0 to 0, this 1 change and again 1 to 0, count is 2.

So, what is the transition count, transition count means there is a change from 0 to 1 or 1 to 0. So, in this case there are two changes of the transition count this are two changes, now if you take a one fault are here that already it was discussed in the case. So, this is your all 1, so were hear and then we already know that this was your output in that case. So, what is the transition count here, so still here no problem this is one transaction here, there is no problem one transition again the transition count is a true.

I already told you, so if you select our compact since scheme of transition count then these false which was having effect when you are using we another taking that is taking numbers of 1. So, the number of 1 s is 1, the number of 1 s is 2, this is using the number of 1 count to the number of 1 s. If you count that technique, if you apply, so if you are

using the number of one count as I was discussing if you are using number of one counts over here.

So, in this case you are good you are lucky because effect selecting number of scheme of transition. Then, what you are going to do, the number of one transition which we are using for the number of transaction are used. So, in the both the cases with and without the fall you are going to have a same as the transition count, there would be an antioxidant.

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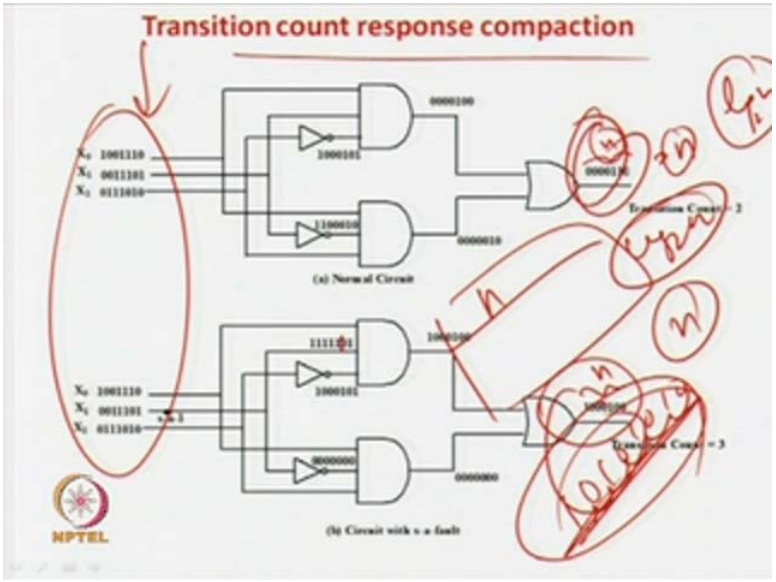

Now, just at the second if we considered this was the circuit one fault this on, sorry circuit on e false circuit, we are considered and this put here with here. This one is the output also considered here that number of transistors, then it upside, this is no transition this is transition from look at this output is the fault. So, the number of transition count is one transition in counts in then one transition count and other transition count, these three, so in this false deducting what is the number of 1 s in this 2.

So, for this circuit on this part counting once is having a antioxidant where as the number of transition of the transition count response completion that is not I told you is that depending on that circuit depending on false depending on the compaction. There can be different antioxidant effect and therefore what we are to do that pattern would be related. You can decided that by your random pattern generator by the LFSR design, now you have to find out the compaction scheme. Then, you are to find out which of the most

important part and which are getting detected which are not getting detected because of the antioxidant effect.

You find out the coverage and you do it, basically it is a multi optimization problem as you can see, so all are interdependent variables like say you there are ten very important parts which you need to detect. These RAM area you have to find out which is the best compaction technique, so depending on the base compaction technique or depending upon the compaction technique, some false will detected or some false are not detected. Again, these falls will be detected depend upon which input patterns, so if it existed pattern generated like that factors primed that is fine, but sometimes may not be using a primed polynomial prism wonders much more smaller area of the LFSR.

You may not be have full generation you have led to much more area in the case you can use a another LFSR without the premature polynomial. So, you do not go for the exhausted pattern generation, you can have what about you requires that number of pattern, the subside are using for this pattern generation may have the various effected that means what that is they cannot compactions scheme. Now, compaction the mining which are those patterns we have to apply so for example, number of compaction matter between area is less and get a very less effect, but the test is used, therefore then all these fore factor if you are using, you can use a compaction technique in the coverage is very high.

Then, you are had a grate design, then your life is good because all you can use this four consecutive patterns and then apply very quickly from your LFSR and all the factors are constricted by the compaction technique. So, that is why it becomes a very important role in design challenge that given a compaction technique or some time you may have to require to change the compaction technique. If I apply this alternative patterns, it takes a long time to generate, so what I can say that can I have this patterns, can I have approve attest this number of pattern some one of them.

So, I can generate this pattern very quickly from this LFSR, but still the compaction technique will give me a less amount, so all these have to be studied and there are lot of characters which will tell you the result. In a given circuit, we are saying that If I do this is the patterns compaction technique in to the false coverage. Then, it may if you are getting very low completion, then either change your completion technique or change in

the patterns from here the all these things. We have to do is besides which tells us to apply to compaction technique we will use and depending on which test pattern will happen.

You can decide characteristic polynomial, you can decide on your seat, so that why it is the design of bits is a challenging problem, so that you can appropriate correctly of our most of the files are at the same time. You can say that very quickly using the initial set up patterns, these are from the seat from a standard modular direction. So, that is a very important point, so I mean one most important thing is before we start for the discussion is what do you there is two particular compaction technique. So, what is the game, so if say it is a input output input output, then what is the gain in the storage.

So, if the n bits output can be there, so if there are all 1, so if there will be all 1 what will be case there, you require how many bits to storage, so there will be in number of 1, so what is the number of bits required to do that. It will belong to n, similarly count can be what, so 1, 0, 1, 0, 1, 0, 1, 0, 1, 0, so 1, 2, 3, 4, 5, 6, so it can be played game in the order of n. So, if you are storage means flap, so you require to store the fact, you can require a n bits to store if I count the number of 1 s.

Thus the value will be n how many bits are required to store n in a RAM, it will belong to this in the case of transition. So, transition counts then in vast case, there will be always the flip and the value will be at most in the order of n.

We are going to store n in a RAM or binary again log of 2 n, so if the ram size you stroke this outside output flatly requires n be to storage the output is in between if you are using one conventional count or transition count see you require. So, that is the amount of factor we are same in this case of this one in this case of this two compaction scheme we have seen, but again we have seen factors in those things. Now, understand the fact that for one such an output n to login we have seen and if there is a large number of inputs. So, you would be saving every hour every output you will be saving value from n to log of n.

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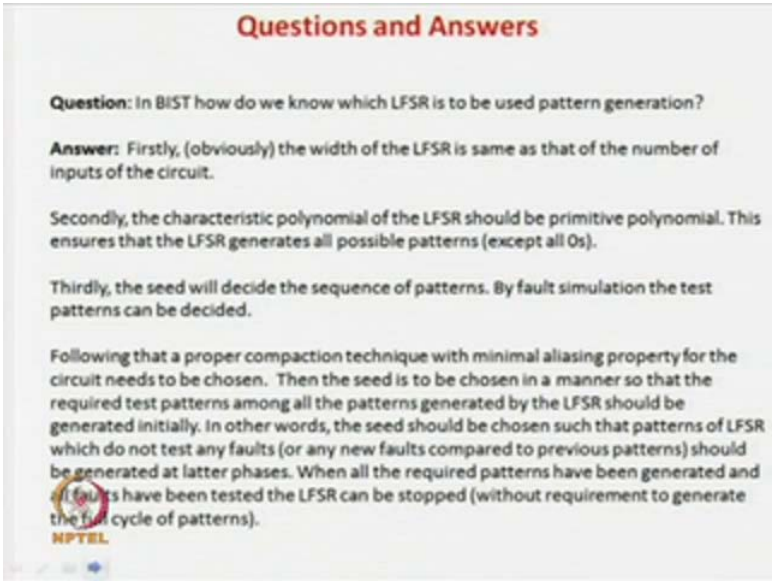

So, that was about discussion on what do call the best architectures, so we have discussed two very important components of bits, one is the random pattern generator which is using LFSR. Then, also have seen the other most important components of bits that this is response compaction and comparative. So, the component is very simple, so compression with two comparative in 1 s, so it is just bit wise compression you can use, but the very important part is how can compact your output response.

So, compaction should be minimized, so in this case we have given a few examples that given the circuit given the pol given the input peddle and the compaction method the values will change. So, it is design problem and we have to find out which one is the best for you, now we will go to the question and answer session, so in a bits how do you know which LFSR is been used for that is a very important part that is what we are discussing. Now, that is given of circuit how to design how to design which is, how to design which is fashion relater, how to design which is your companionate, how to design which you see.

So, all we depend how quickly you can do your testing and that is with the minimum number what are the factors and how could coverage the minimum when you think it actually. So, first as the number of this side of that is obviously any inputs are that. So, it is the n circuit, there will be, so the obvious to the generally secondly characteristic polymer should be with the polynomial with generate all personal activators. The general

statement if you general gave most of the cases you may be require all patterns do the testing.

You can go for periodic polynomial, but also the other cases in the all 0 cannot be generated see were the soon, so other way you can find out the which is the most important pattern require to be generated. So, according to you can say that you can use the there are main characteristic were phenomenal may be if you usual targeting are few are be vectors and you do and also the existing pattern. It will pre multiply with the polynomials if may as the paramedic if you can solved the testing tough with the good coverage. Normally, I am saying with the few initial pattern kind of first and you can go for may be periodic polymer.

Thirdly, the scene is very important as a that you told the generate being a such fashion that the initial pattern testing for the coverage, so like this one following that the compression take that taking has over good compression. So, what is the good compression taking which is going give minimum amount as seen for the said of pattern which you have decided seeing this LFSR. Now, again these are already told you these are not sequential problem will be decided sometime you have to go that at a integration. So, what you have find out basic problem take, already these have a scheme whatever complex and comp active to complication.

They can use these is the lot have seeing because one of the taken for the (()) go the different type of patterns. Now, you can find out for using difference of the pattern which has give no here over of what you can do, we say the compaction techniques. So, these are three postage required to design a LFSR, you can say the design of this architecture this circuit, but again these are all inter depended problems, you may have go for iteration.

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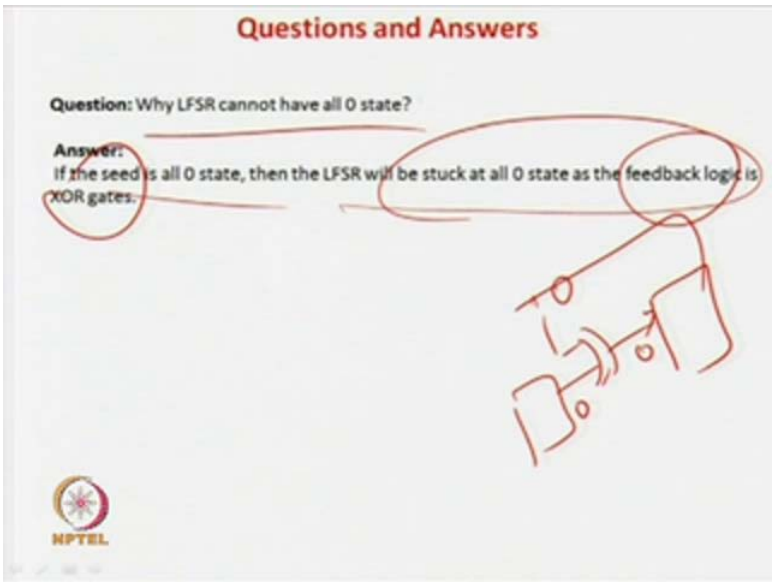

So, that is the answer the first question in the case why the LFSR cannot have for 0, the answer is if the series are 0 LFSR this all circuit state 0 as a feed back all 0 s are LFSR as the feedback have the targets. If you have a LFSR as already seen this case, so modernize LFSR, you considered something this. Now, see this one is also zero these are a feedback from a thing, so 0 X are 0, so I am getting always the craft, so on the feedback in the X targets are on the feedback LFSR. So, it gets everything is 0, so X are of a 0 and 0 is a 0, so whole thing is started at 0, so if you have very adamant it is very much equal to 0, 0 as the pattern.

So, you have applied exactly that have to applied if you cannot do that if you have certain smaller circuit which is apply on all 0 to the circuitry because LFSR can be all the other patterns. So, with the discuss of compilation of 0, so in the last class what are in next part of the course will have a interesting part that is actually remembering till now we seen circuit how to do circuit in the offline mode.

Also, circuit have the testing incentive molds that is the based that is the thought part of circuit not have base. The course is not a ordinary combination, see the circuit is the specially design circuit which scores more a lot of binary circuit which are taking, but a mode of area simple test. We have seen in like growth in a 80 percent sense, generally whole for or binary architecture quite from in normal discuss, how to quite from in next class, we can do testing from memory design. Thank you.