Design Verification and Test of Digital VLSI Designs

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Module - 10
Sequential Circuit Testing and Scan Chains
Lecture - 3
Scan Chains based Sequential Circuit Testing - 2

So welcome to lecture number 3 of module tell 10, in which case we are discussing about scan chain based sequential circuit testing. So in the last lecture and one lecture before that we followed that for testing sequential circuits as there is a flip flops, so which actually make a difficult you control the secondary primary inputs and the secondary primary output difficulty to observe. So because of this reason you have found out that sequential circuit testing or a t p g is low difficult than combinational circuits. For combinational circuit a single test pattern can be is the determined which can detect your fault, so that is by sensitize propagate and justify approach.

Now if you look about the sequential circuit which have already seen in the last two lectures. We saw that if you want to test a sequential circuit then what do you have to do you have to first go for time frame expansion method, that is you have to slowly control the virtual secondary virtual primary input or that is the secondary input which are the output of the flip flops. So they cannot be directly controlled. So what do you have to do, so you have to use a time frame expansion or you have that is by means series of sequences you have to control these inputs were virtual inputs and then you can apply the test pattern of the primary inputs and then you can test the circuit.

And we found out that this process is a complex process; because at a you have to control the flip flop outputs which are the secondary inputs. There is a series of pattern may be required to do and you can find out that in the last stage there can be a conflict which can lead to the restart of the whole procedure so leading in a lot of wastage of the computation time.

So then we have found out that when we discussed in last lecture that, to avoid all this complex business we said that can we directly control the flip flops. By say using the set and reset lines. So this was the very good visible approach and we solve that it can be easily done in two dime two pattern we can easily test the circuit, in which case in the

first pattern you set or reset the flip flop as required and then you apply the primary inputs the second pattern and do the testing.

But then we find or found out that have the if there are n flip flop then you required to two n number of the pins in the circuit to do that. With an extremely complex procedure because mean there if the if circuit has around 10 to 20000 flip flops are having 20 to 40000 extra pins is not a very feasible approach. This is because the packages with more than 1000 pins even we have the limitation of our 1 0 2 4 packages I mean that generally have in the market. So going beyond that is very expensive and have a having about 10000 pin outs there in visible situation.

So while the idea was good which convert in a sequential circuit to a virtual primary combinational circuit and in it the testing but, the huge number of pin outs actually care created the (( )). Then what we have done then we have said that now let us not control set and input set and we said liked of the flip flops of the primary inputs making them as primary inputs.

Later then let us use a shift register and we note this shift register in a sequential fashion and the output of the shift registers will be connected with the set and reset lines. So that whatever set and reset lines have to we controlled what we can do we can as required you can scanning the values or you can shifting the values in the shift register and do that.

But then we found out this a good approach because a the two things are there the pin outs are not increase much but, you require another pin out for the put in the values of the shift register you read a different talk for the shift register and these are extra output for the shift register. With three more pins you can do the testing that is you can control the set and the reset lines individually using a this casual register. but, now here the problem is if you have n flip flop then you required 2 n number of extra flip flops in the shift register making is area over and (( ))

Also secondly mean to control the flip flop now you are required 2 n number of clock pulses, because you have to shift in the values of 0s and 1s for the set and the reset lines. These with their n flip flops we saw that there are 2 n lines concentrate the set and reset line. And then you have to shift in 2 n number of patterns or bids in this case to control

the set and reset lines. So that is an actually a cumber sum process then we found out the real great design in (( )) testing that is the scan chain we solved most of the problems.

So what the person said that if you already have a shift register, if you already have a series of flip flops of the circuits why not use them as scan registers or why not use them a shift register? So he said that I will not use any extra shift registers to control the flip flops wherever I will use my circuiting 2 modes. In one mode is the normal mode when the output of the nested function block will go to the flip flops and this another mode what I will do I will connect all the flip flops in the shift register mode and the output of the flip flops will be connected to scan in pin or so the output of the previous of the flip flops.

Already we have seen the architecture how was scan say register works. And this now in the test mode you can shift in values of this scan chain whatever you required to control the flip flops and if there n flip flops you required n pattern to control the flip flops so you have shape you just saved in n number of patterns compare to a shift register approach. And also we have seen that you did not require any extra kind of shift register, so it not require any extra flip flops do this n register base testing. Only the extra requirement is the mask which also very simple because you do not require set reset arrangements in the flip flops.

So the set reset arrangement extra area you can incorporate in the adding a multiplexer. So all the problems almost for sake of sequential circuit base solved by the scan chain problems, scan chain design, the only issue that remained is that to set the flip flops you require n it is the n flip flops in the circuit you required n bits or n clock pulses to control them. So only that part remains, all other things are solved using the scanners scan register based one.

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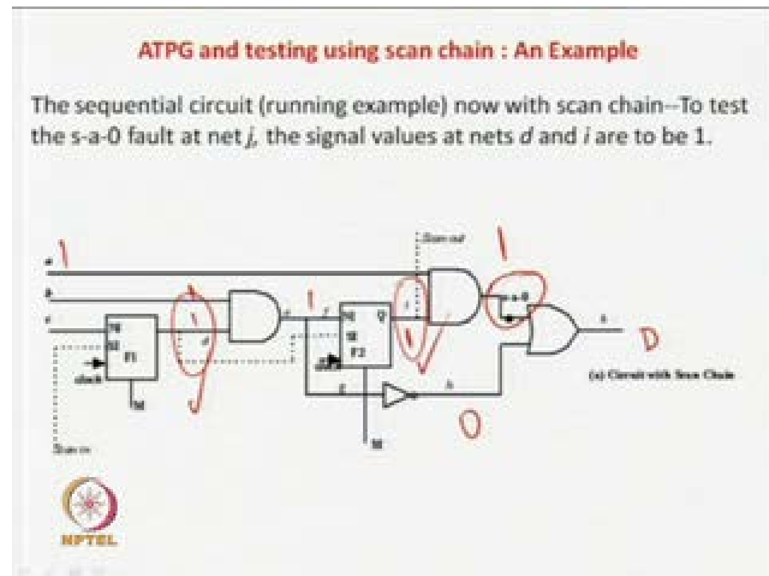

So today what will see, will see in details about the scan chain how that design and how can you optimize on the number n. So if the n flip flops you require n number of bits to control the flip flops. So if you will see with the there we can decrease that and many other things will try to see about this scan chain today.

So first will start with the example. So you remember this is are this is are the old circuit we are considering every day. So in our lecture so there was a stuck at 0 fault and there is a 2 registers if you recall to test the stuck at 0 fault you require a 1 over here so D is propagated, you require a 0 over here so you require a 1 over here so you require a one over here you require one over here Similarly, you require a one over here and also you require a one over here.

So we know that this is one output of the flip flop and this is another output of the flip flop, which has to be controlled the by any means, so you can added you saw that by how by controlling it by is the set reset lines and also saw by controlling it by a shift register where you have put few four flip flops and so on.

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So now will see how it can be done by using the scan chain. So the main ideas are this one is to be one and this one is to be one has to be done. So already discussed what we will do in first state we will make m equal to one that is the removes the next state function block from circuit and the flip flops are connected the scan chain. So as already said that if you make m equal to one that is test mode equal to one if you do then what happens then this series of flip flops that (( )) from the circuit that is the next state function block is the (( )) connected in a scan a chain mode.

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Then in this case you require a 1 over here and 1 over here. So you require a one and clock pulse then you require one n a clock pulse so two one with two clock pulse with will get the flip flops set to one. Now let us just look at the architecture circuit architecture of the bit in details. So what happens so you make a m equal to 1 so this is the normal input from the n s f block, so which is cut you can see this is the output not there which has been cut then if we flop similarly, this was the output of the n s f block which is going to the flip flop number 2 that is also cut by this making n equal to 1.

So what happens this scan in this external thing that is get gradually flip flops output of this flop flip flop get connected to the input of the second flip flop and this final output is the scanner output. So now it becomes a shift register chain. So you apply 1 1 at the rate of two clock pulses then what will have you have one here and one here. So this actually sets your flip flop.

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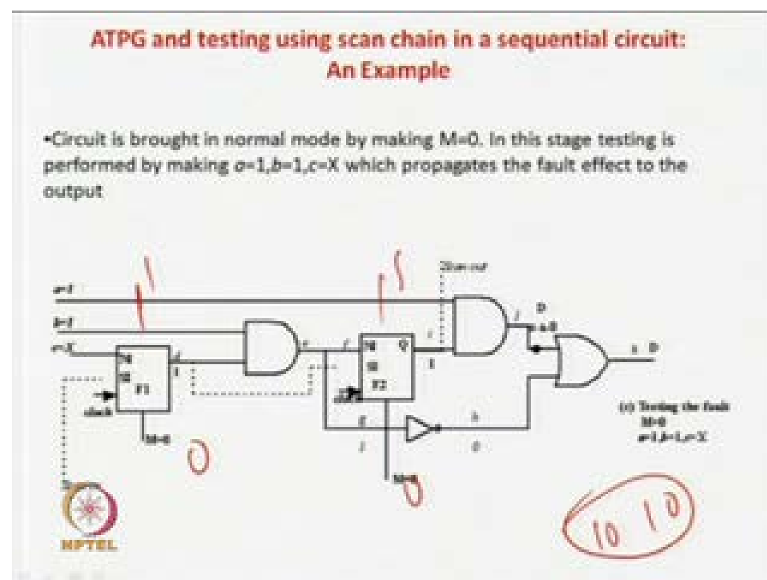

So you can understand that what you have achieve. So in the previous if you are using a scan register sorry scan with the shift register to do this, so you require 1 0 and 1 0 because set equal to 1 reset equal to 0 then again set equal to 1 reset equal to 0, so pattern of 1 0 1 0 is to be shifted kind of a thing to make it but, in case of shift register only you required the pattern 1 1 to control the registers flip flops, so the registers of the flip flops.

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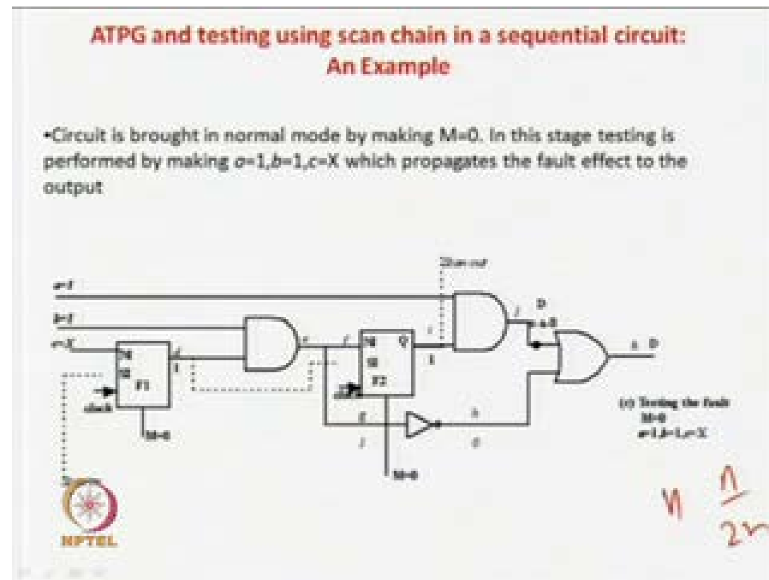

So if there n flip flops so you require only n patterns in scale of scan register base testing and two n in case of shift register base testing. So not only in this scan chain actually solve the problem of the extra number of flip flops in this serial sequel what you call the register but, also you solve the problem of reduce the number of time required to moving the values required to control the flip flops. So in this case it is if the n flip flop maximum n patterns you required to a shifted.

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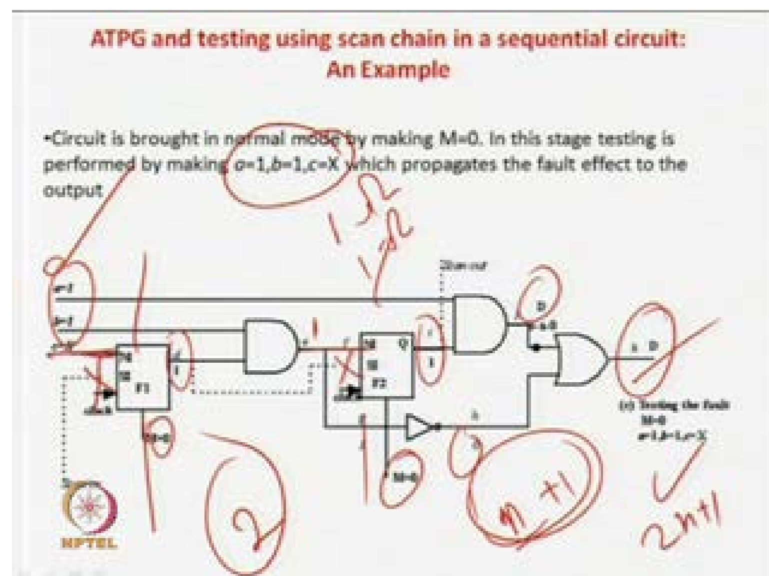

Now what happens so now you are a you get this one as 1 you get this one as 1. now it is done. Now you have to apply a 1 and a 1 as we know to get the flip flops again the fault tested. So now what you have to do you have to make n equal to 0 so already discuss at when n equal to 0 then this scan input or the scan chain gate will de couple of the circuit and the normal n s f block gets connected to the circuits.

So if this is done then what happen so this is the normal operation of the circuit so what you will get so you are having a 1, so I can apply 1 1 over here, so you get a D over here, you get a 1 over here and then you get a 0 over here then you get the output and reduce tested. So this is there is always two patterns require to test the fault. So you should not called it two patterns you should call this is the final pattern which actually applied with the primary output to the test and two bits shift were required one and a clock pulse one and a clock pulse to do this kind of to set the flip flop. So you require n that is here n equal to plus 1 number of patterns should at the fault.

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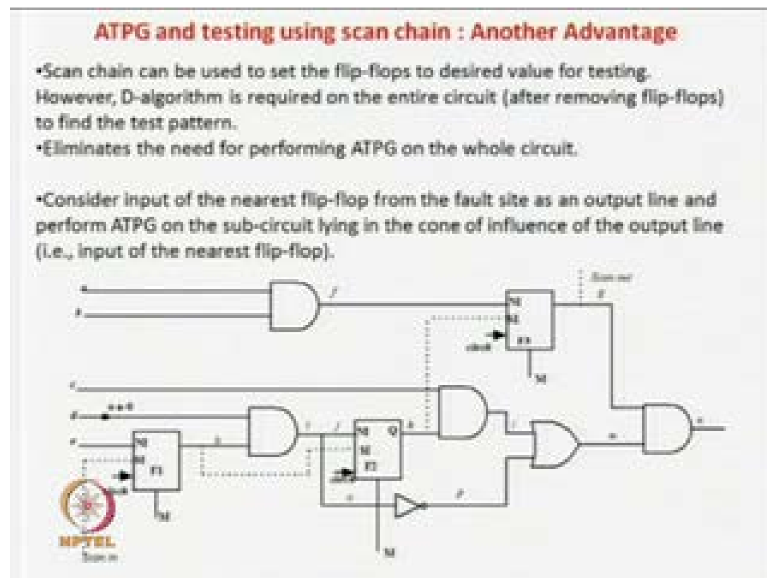

So in case of shift register base testing it was 2 n plus 1 and in case of if you remember in case of set reset line testing so in case of set reset line testing circuit I mean a test pattern you required only two patterns. One pattern was directly required to set and reset this two flip flops and one pattern was this one to do the this thing. But, in that case the external number of pins became so high that actually it fill the fault.

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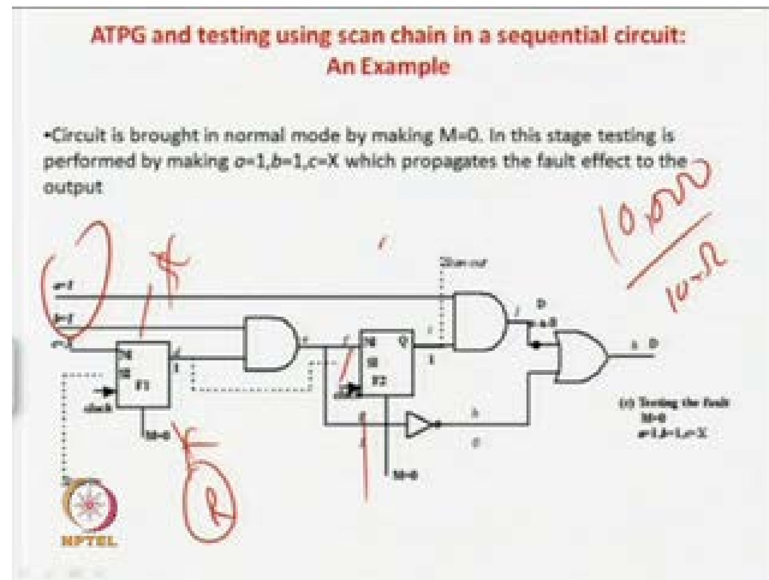

So therefore, you have to go to this scan chain base this thing and everything was solved. So I mean only disadvantage in this case we have found out is that, we require two patterns I mean two n's sorry n number of patterns to shift this flip flops so if there are 10000 flip flops say for example, in our circuit then the problem is that you have to have a 10000 clock pulses to set the flip flop first or reset the flip flop first, and then only you can apply the family pattern.

That is the only problem that is remaining with this scan chain. All other problems have been solve because no any extra idea over it for the shift register and you can say that I have put some multiplexer. So what is the consequence putting the multiplexer does not have any much consequence here that you have to understand. Because already told that when you are having this scan registers you can see we do not have a set or a reset line is not there these lines are not there.

So whatever area we says by putting this so you can say that eliminating the set or reset lines. Now can be we can say that I have got this advantage by I mean whatever I have saved by removing the set, reset lines that part of the circuit I can add for the multiplexer. So there is I mean we should not say that there is exact the same amount of circuit your saving is used by the multiplexer but, what some areas we have said because of not using the set reset lines and we can do it in this way.

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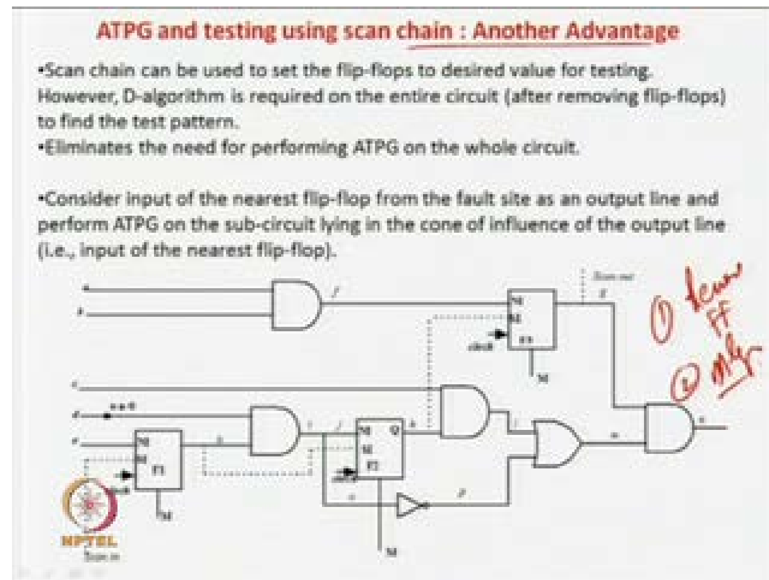

So this way you can understand a this is a basically a you can say broad de coat, un coat saying not is a very absolute terms you suit thing. But, you can think of in this way. So now we are trying to solve at the problem the main problem that remains is n number of patterns to set it. So let us see another advantage, that actually now to solve this problem we will get another bi-byproductive sometime see this another bi- productive we will see get as will see here. So you will get another advantage of using this scan chain as we seen, so one advantage will be this n will be reduced and second we will see that we are getting another advantage so slowly will come out.

So what happen if you saw that if you are using this scan chain till now what about we discuss, so you are using the shift registers mode, you set reset mode so what we have to do first step was a remove flip flops, that was the first step and second D algorithm. So a you remove the all the flip flops from the circuit and we will perform a D algorithm. So that the two basic steps, remove the flip fops and a perform a sorry remove all the flops and do D algorithm. So whole circuit you have to apply D algorithm but, now we will see that by using scans chains you did not to do D algorithm on the whole circuit you can only take a partial circuit and do this.

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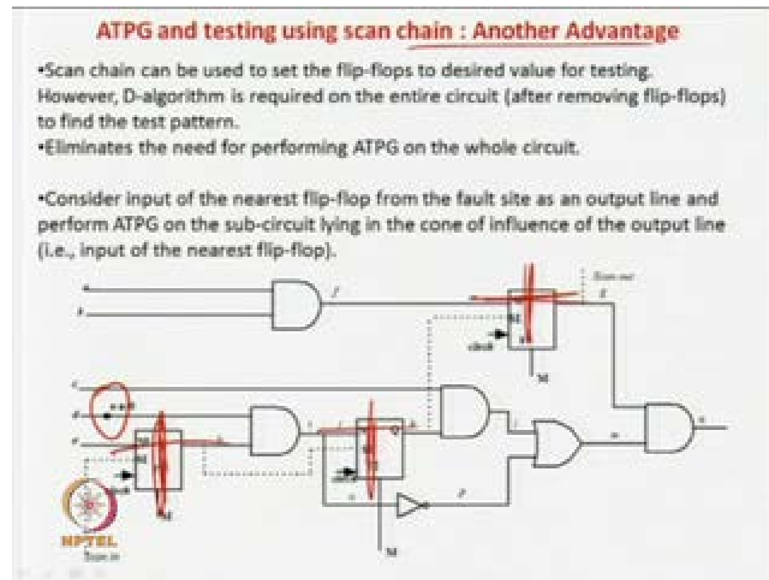

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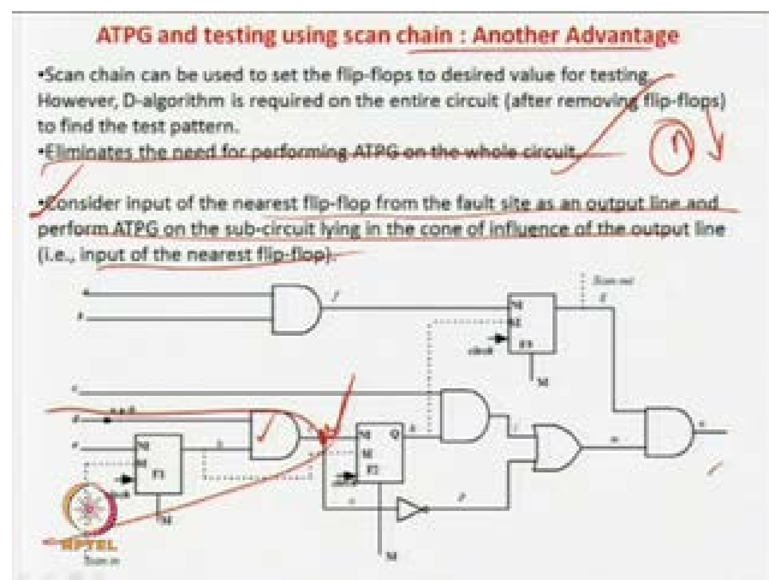

So let us see this a new circuit we have added this part of the circuit to illustrate the concept. So let us take a stuck at 0 fault over here. Now if I say that I want to use the standard which was discussing so what you will do, you will remove this flip fop you will connect them here you will remove the flip flop connectivity as you remove the flip flop connectivity here and do on a t p g on a whole circuit. But, so it takes some time and complexity. But, now will see that if you want to do this another advantage it will see in case of scan chain it would not considered the whole circuit for the a t p g. So what we

will see first we have to find out a entire circuit you required the eliminate the a t p g on circuit.

So new advantage will eliminate the a t p g for the whole circuit as well as this n factor will also come down. So in that you have to find out what you have to consider the input nearest input of the nearest flip flop from the fault size as an output line and perform a t p g on the sub circuit lying in the cone of the influence of the (( )). So what you have to do basically, you have to find out a flip flop actually which is nearest to this fault size.

So in this case you can think that so this is my nearest flip flop input, because this is quit far this output is quite far and this input of this flip flop this flip flop input does not come under the influence of this faults size. So you can think that this is the ne nearest input of the flip flop which is nearest from the fault size. So just consider the nearest input and then make a cone of influence sorry then you have to find a cone of influence.

So what do you mean by cone of influence, cone of influence is nothing but, say for example sorry yes so what do you mean by cone of influence, so cone of influence of this gate say of this gate output is actually input a and b. So that means these output is depended on only on these two inputs and not on any other. So cone of influence of any point on a circuit is all the inputs and the gates which influence, it is a very simple definition. So in this case you see this is the point so how yoywhich gates are in involved in this one, so this gate is involved in this d and e are involved and the flip flop is involved. So only this sub circuit is involved in this one. So the cone of influence is only apart this very small circuit part of, so if I make a cone of influence at this point so I will have only this part of the circuit.

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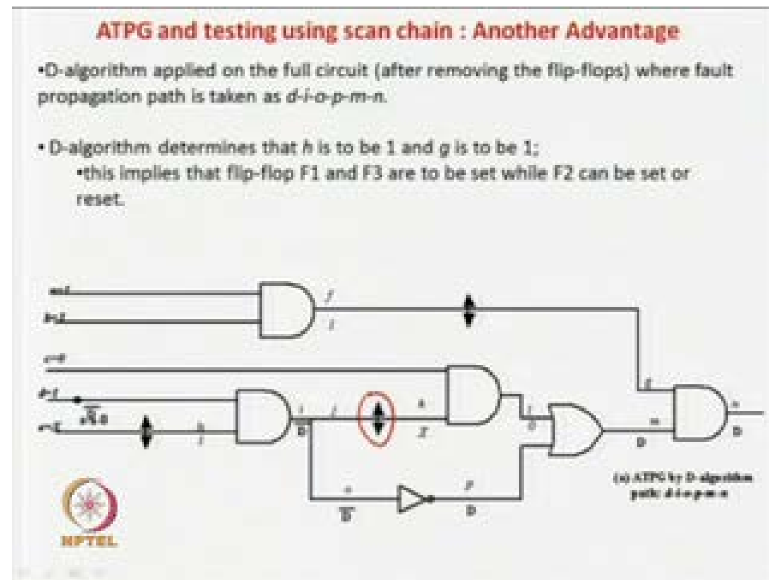

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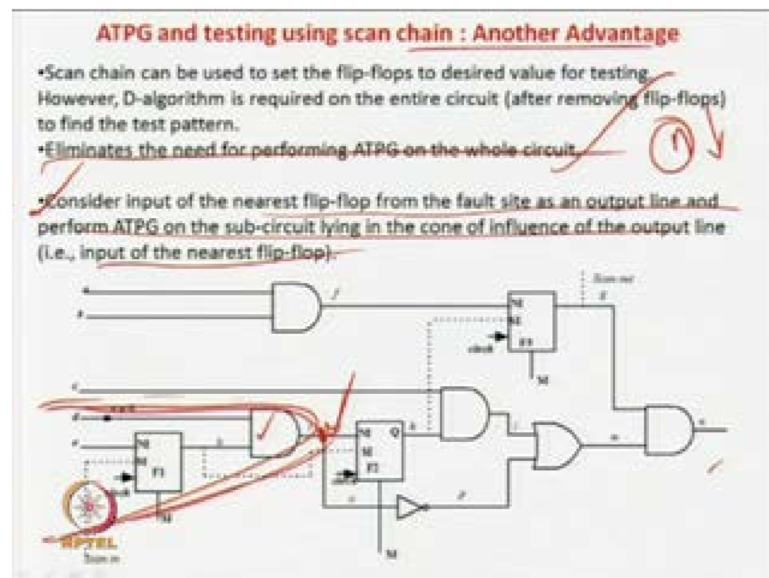

So what you have to consider, you have to consider only this much smaller small circuit for this a t p g. Because you have to first find out the nearest flip flop and you have to do that. So the level just see whatever we have done. So just remove the flip flop all the flip flops are been removed, now you do not consider anything else. So we will show you that advantage in steps, so you just will see the mean that this is this is what is the advantage we are going to get that what we will do is just consider the small circuit only small part of the circuit over here and a t p g and solve the problem. But, if you are taking the normal approaches is removing all the flip flops, doing a t p g and all those

things so it will take a roundabout approach. So we will compare both the approach and so that what is the another advantage.

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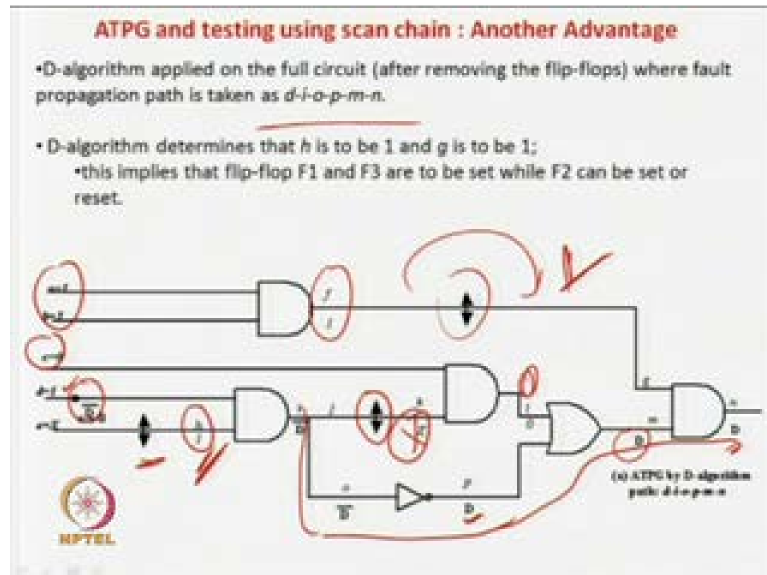

So now let us see that it is whole circuit after all the flip flops are been removed. Now let us consider the paths, this is one is the path so we are taking the traditional approach now, another advantage we because it will show the real advantage of this scan chain business then you have to compare both the approaches that is traditional approach and is scan chain approach within the conditional scheme. That is considered the whole circuit and do that, so that you can see exactly what is the advantage then it will come out but, if I just show you one approach then that is the new approach then that will not u that much high feeling, right.

So let us say the path, so what is the path so let us say the path is d this is the path then you say that i so this is the fault this is the fault path, we are taking this is the i then you are saying o correct, then it is p this p and then m and d. So this is the path the person as selected for fault propagation. Because there can be any another part also if you can see that there can be this another x path this path also you could have taken this is another path like from this there was another path that I have taken for the fault propagation. But, this has not been selected because from here there are two d frontiers from this gate there are two d frontiers one is this from this gate there is one d frontier over here another d frontier to the down lye.

So any one could have been taken but, the person as selected this one so let us go about it. So the stuck at 0 fault so you put a one so you get a d prime over here, now you get d prime over here you require a one over here so if you require a one over here means there is a flip flop over here. So, somehow you have to make it 1, so that you can easily by scan chain by setting it to be 1, correct. Then you take the d over here and then you get a price inverter, so you get d over here right this is a or gate. So you get a d over here you require a 0 over here.

So to require a 0 over here we required a 0 over here and then finally, we get the d at the output so for that you require a 1 over here, so to get a one over here you require a 1 1 over here so there is a flip flop over here so there you have to again get a 1 over here. So that is actually another flip flop so by scan chain you have to control this for output to be 1 and this flip flop out to be one the second flip flop output now is x is not clear.

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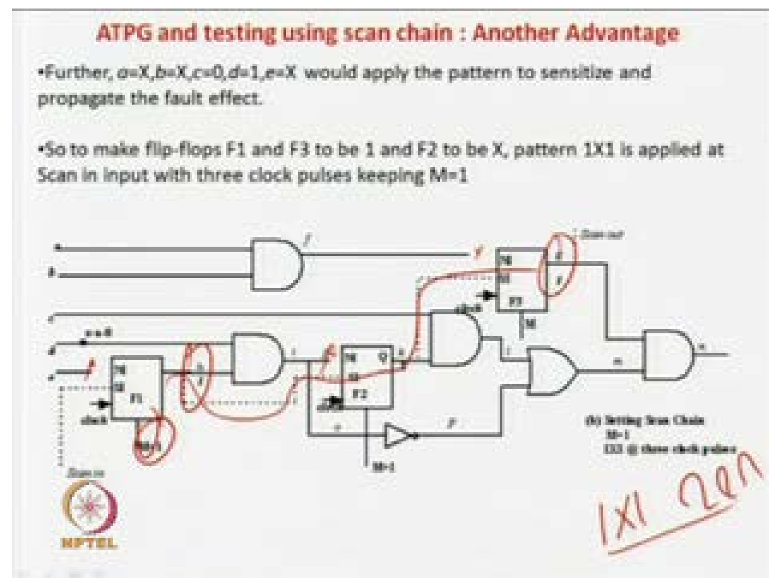

So there is about the traditional a t p g or sequential circuit using scan chain. So there is what we have got so you would require 1 1 0 1 x do not clear (( )) said to be 1 there is f three flip flop has to be set to be 1 the middle flip flop did not be clear do not clear it is an x over here. Then you can test this stuck at fault. Now let us see what happens, so first we know that you have to set this flip flops.

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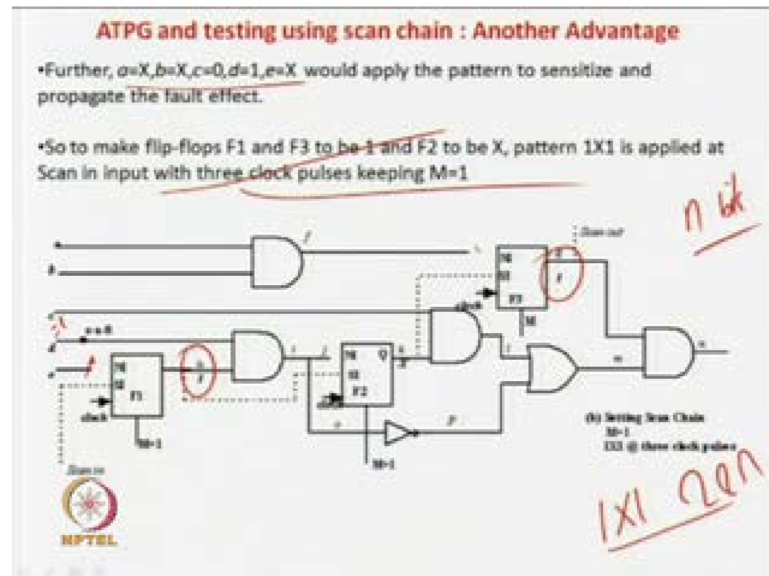

So now set the flip flops means you have to put is mu make equal to one you can see that this scan chain is connected this part and this part of the circuit is totally de-coupled. So what you have to apply you require 1 x 1 and 3 clock pulses because these middle one you do not bother, this has to be 1 and this has this has to be a 1.

So you require 3 clock pulses as already discussed in the traditional free I mean scan chain base testing, so if there n flip flop so you require n bits to transferred. So now if you just do that so whatever the flip flop requirement like this has to be 1 and this has to be 1 you can easily obtain. Now what you do so that is that is been said would apply the pattern to sensitized fault so here actually you have to apply a 1 very that is the that we can know that but, 1 and a 1 has been done. So this is what is the flip flop has been taken care off in this scan chain.

Next what you do next you make m equal to 0 that is our traditional approach and the standard approach of the flip flop scan base flip flop. So once this is done so this scan part is decoupled from this circuit so this part is decoupled from this circuit now what happens normal n s l block output is connected, so you can see that this is 1 so you are getting a 1 over here, so you are also this is not required any more now what we do to make a apply d equal to 1, so this is apply d equal to 1 then what we get is this case so stuck at 0.

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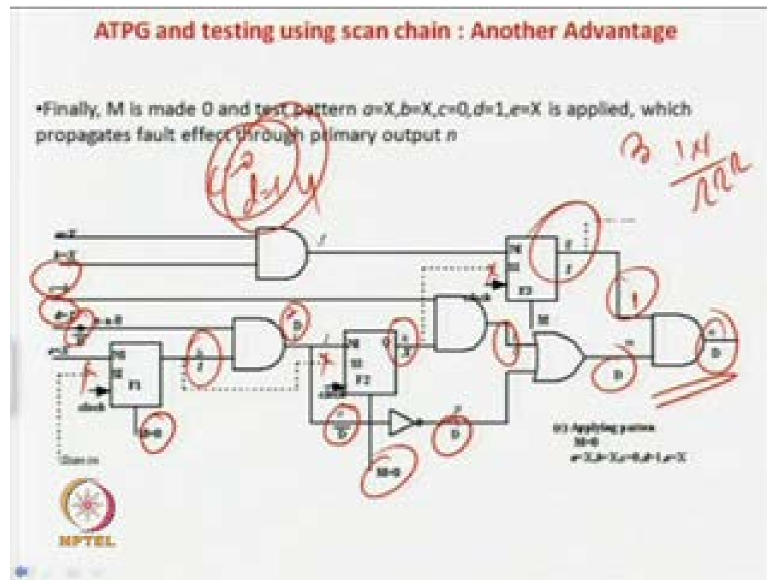

So this d prime over here and then you get a d prime over a output 1 over here by scan chain as control the flip flop so you get d over here sorry you get a this is d prime sorry d prime over here and then d prime is over here and this is a inverter it will be d over here d over a because we get 0 over here by applying c equal to 0 and this is come out close this gate is this is we flow control by a scan chain and you get a advantage and your fully circuit is tested.

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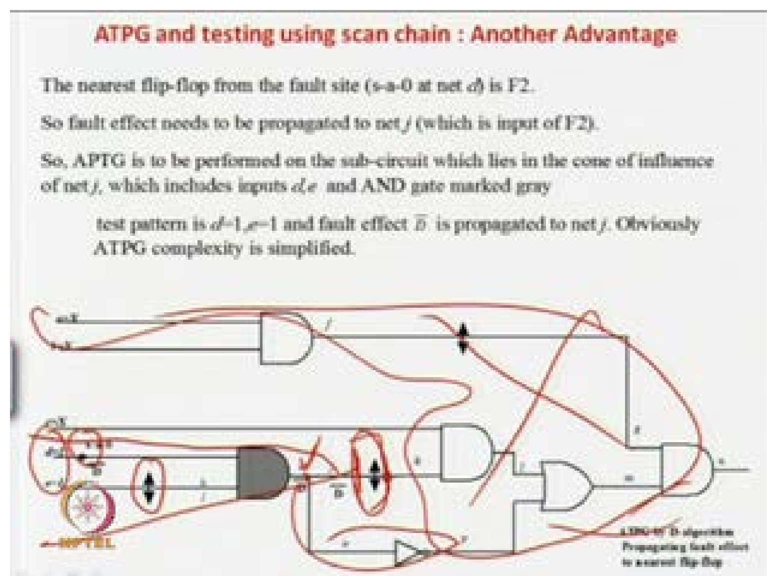

So in this case we required two pattern sorry we required to three pattern, what is 1 x 1, so this one apply a three clock pulses and finally, we applied the pattern c equal to d 0 and d equal to 1 this the pattern we have to other side excess, then we get the circuit to the tested. So 1, 2, 3 and this is the 4th pattern.

So in 4th pattern we have done the testing using a scan chain. Now the another advantage which we are going to see that one we are going to now discuss. So in this case what we have seen, so we have considered the whole circuit for the a t p g that is the one problem and this is the big circuit so combination even the combinational a t p g by d algorithm will take some times because there in this case no back tracks, but, there could have been back tracks and all the problems. So the we are considering whole circuit and secondly n number of test patterns are required to set the flip flops. Because in this case there are three flip flop so we require three patterns do that.

Now again what we are saying that now we take the new approach in which case we saw that this is flip flop is here and this stuck at fault was here, so this was the this is another flip flop was here, so this is the nearest input to the flop flip. That is what is the question so that is which is the nearest from the fault side this is the nearest flip flop when we could have reach from the fault side. So just we will forget about the hole circuit you can think hole circuit will eliminate.

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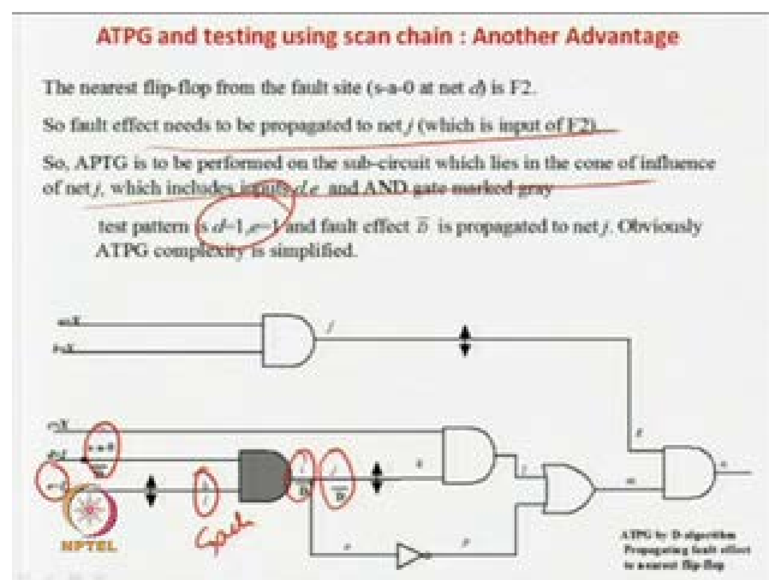

This circuit also you can eliminate, only will consider the circuit from this point that is input this point in the cone of input. So only this sub circuit we are going to consider. We are going to consider this flip flop and from the this flip flop and all the circuit only influencing by the cone of influence by the flip flop.

So only this small sub circuit will come into picture, this gate will come into picture, this two flip flops will come into picture and this two inputs will come into picture, nothing else. So unless we do a t p g on this, will forget the hole circuit. That is the big advantage we are going to see over this. Now what you are going to do, so we are applying this is the stuck at 0 so we have to apply 1 so we get d prime over here now you can require 1 over here correct because you have to fault f affect will be propagated so we get d prime over here correct and for that we require equal to 1.

E equal to one means this a flip flop so this by we can change they we can set it and this is the case and so the fault affects is here which has the input of the nearest flip flop from the fault size. Your job is done, we do not require any other fault of the circuit and see your a t p g even by D algorithm is very very simple over here. So you just consider small this sub circuit in your done your job and you are done. So what is this, the fault effect needs to be propagated to net j only which is the input of flip flop 2.

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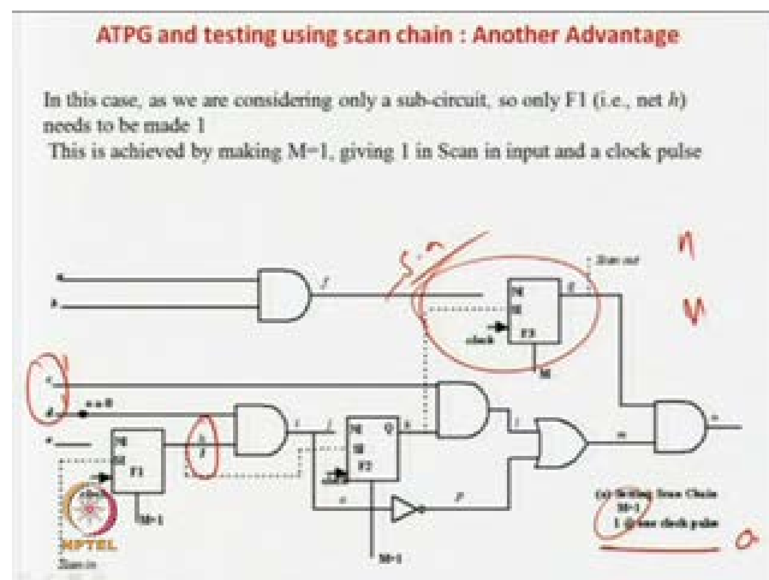

A t p g is performed the sub circuit which lines the cone of influence of this one, which is only the small part, the pattern d equal to 1 will do your testing so your job is done, so

obviously this is a very very simple approach and you have what do you have I can say that your combinational circuit a t p g complixity will be reduced greatly. So that is given now what you do now we what is that is done, so only know that this is equal to 1 and this is equal to 1 will do the testing for you. So for that only one requirement was that so this flip flop will have to be set it to 1 by the scan chain.

So what you can see that you are again the saving greatly because this did not control this two flip flop. That is another important advantage you have remember that we are not requiring to save this two flip flops in the in the previous case we require three faults have to save this flip flops but, you do not required to do all this. Bbecause you are only considering small part portion of this circuit do over job.

So only one clock faults and one flip flop scan in is there, so scan chain is there but, we do not bother much. We just n equal to 1 and setset this flip flop. So we can also think that if there is the fault here, that we can say so in this case this will be the nearest place so in this case to setset this what you called to save this flip flop for some reason or the other, than we have to apply briefly free what you can call free clock pulse have to said the flip flop it is per it from the scan chain input. For in that case you have to go to the worst case by if they n flip flops and we require a n pattern to setset or reset the flip flops by the scan chain.

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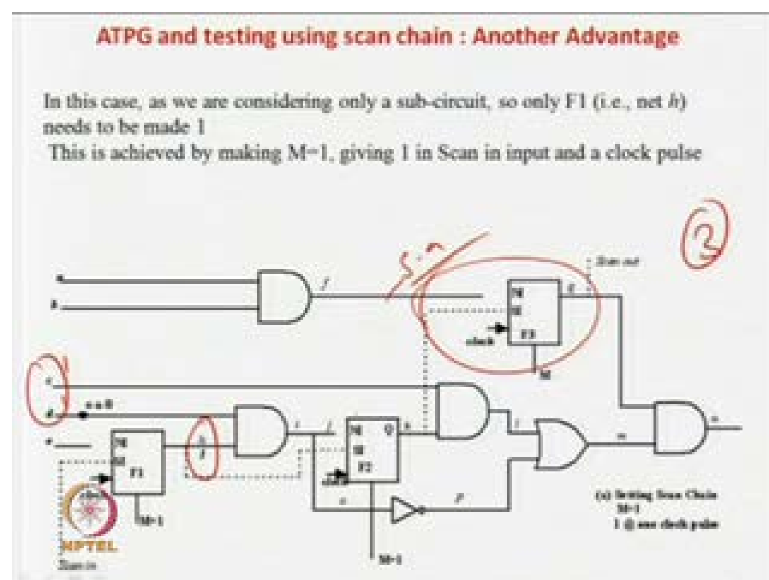

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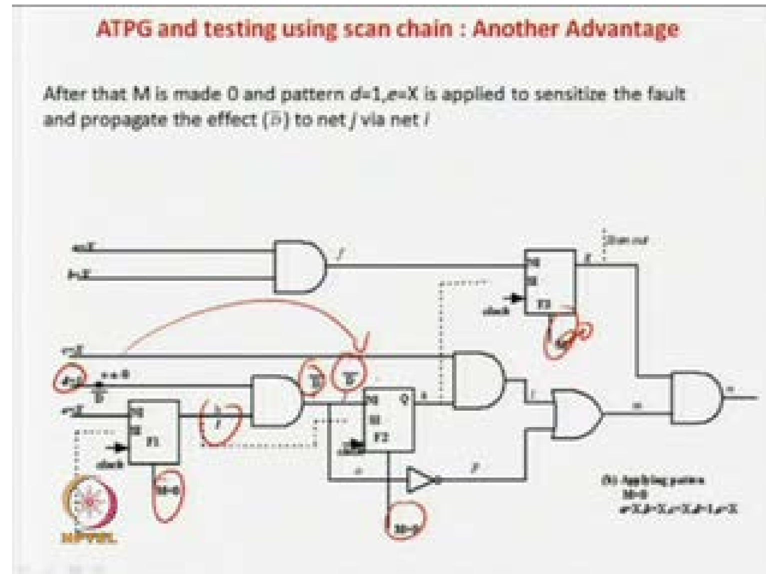

But all the flip flops will not be farthest from the fault side. And allowed if you go for a average so half of the flip flops will be nearest very much nearest to the fault side and half of them will be further. Because every time we are going to in a average case we are always going to find out the fault which is nearest to the flip flops so there will be great deal of saving if you look at the average cases. So in this case say for example, this is the first flip flops have to be consider only one clock faults will set the flip flops as required.

But, if you the farthest we required three. So if you take would have been some of the second one you have to set, you have to set it in two. So, sometimes in average case will be there lot of saving in the number of patterns required to set or reset the flip flops. So in this case there is one, we have save two patterns. Now what you do so now this is done so you do this. Next what you do you make m equal to 0, so obviously the circuit starts operating in the normal way.

So now what you do so you know that you apply a d equal to 1 over here, so you apply a d equal to one over here so this is d prime, so d prime is there and this is 1 d prime over here. So we have propagated the fault value to the input of another flip flops. Now we have to again use another mode which was not required in case of the scan chain be testing discussed earlier. So in the previous state what you do you set and reset the flip flop. You give the primary outputs thats sensitize propagate and justify the fault to some primary output and your job is done.

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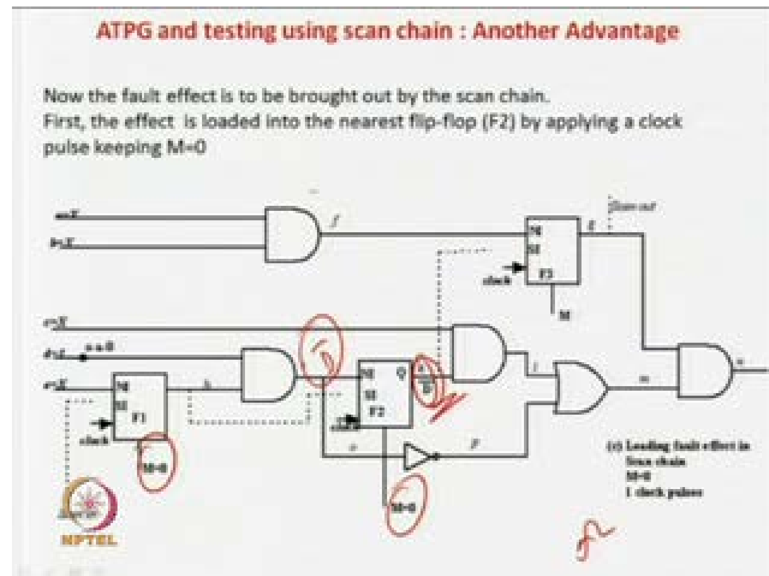

But here the next state for the this advantage to get you are considering a sub part of this circuit doing a t p g on that and propagating the fault affect to the nearest flip flop so again the third step involved, in this third step what will do we again, so this is a actually what I said, so this is I mean this was the case so this I got the fault value I have got over here. So this is the pattern I have applied. Now what you do so there is one more step we have to take into picture that is very important. So initially if you remember the in the last case there two step set and reset the flip flop in the scan chain than get the fault value propagate the primary output.

But here this the another step involved. So in this case again we have to make m equal to 0 and apply a cock pulse. So if you apply the clock pulse what will happen, this D prime the fault affect which was that this input get loaded to the nearest flip flops output will be selected. That is one important thing you have to do. So what is the added step you have done here, the added step is that we have to again go for m equal to 0 and give a clock pulse so that this D prime the fault affect get recorded in one of the flip flop selected.

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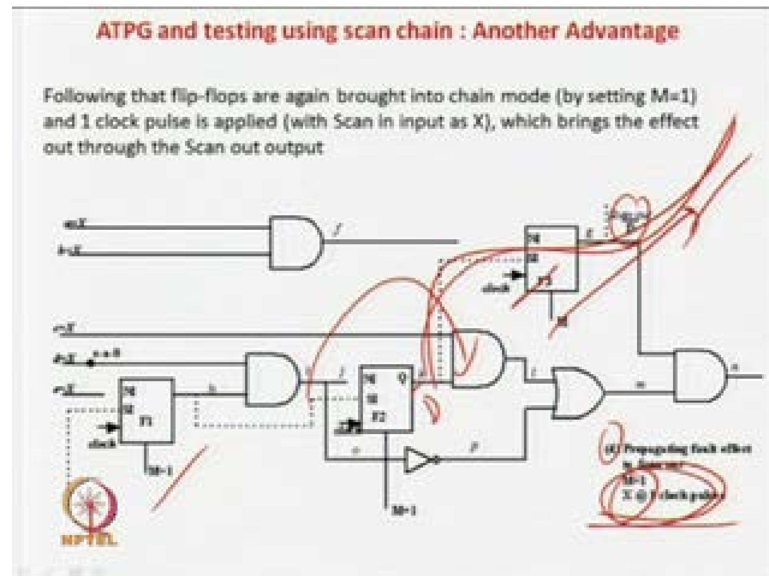

Now again there is 4th step, two more step you have added, in the 4th step what you have to do, you have to put some x in the in the scan in do not bother and keep some clock pulses so this fault affect gets out through your scan output. So two more see what I have done. So in the first case previous approach, so you give a scan chain set the scan chain; apply the pattern and get the fault affect to the a primary output. Your job is done. But, here you have to consider all the faults, set faults the faults to n pattern and all this business where there as well as do a t p g on the hole circuit that was the big problem.

Then how you solved this in this second approach we consider only a partial circuit, which faults under the cone of influence of what? Which faults under influence of the nearest flip flop to the fault side. So once that is done, so what you do you do a t p g on small part of the circuit through there is very less chance of collision and all. So your job is done, so that saves a lot of your time and combination efforts for the combination a t p g.

Now what you do next you next this is done. So next you set the flip flop whatever is required. Now all the flip flops will not required to be set only whatever required set them your what you called scan registers. Once that is done so your fault affect to be propagated to the output of the flip flops selected nearest flip flop is selected. Then there are two more steps to be done. Now you got to the m 0 that is the normal mode and we apply a clock pulse.

So your fault effect will be recorded at the output of the flip flop which was being near nearest flip flop will be selected. Now so that was done your flip flop value it was selected over here. Now what you have to do now you are not consider to propagate the flip flops this fault effect to the output of the primary output. So what will you do use this scan register of this scan output to propagate this value. So you have to again apply the output through this scan chain, whatever was the nearest I mean there is one more flip flop which has been passed to get the output to the scan register.

So you just apply 1 x because you do not need to set or reset any flip flops. We just need to bother out the moving out the value. So we are you give one clock pulse and you are value will be passed out to the flip flop. So here we have to understand that we are not much save there was the clock pulse is because one pulse was equal to set this flip flop, one pulse was there to recording the value and one pulse was there to take out the value. So in the previous case we requires three clock pulse to set the flip flop, here three pulse are required to set the flip flop record the value and bring to the output.

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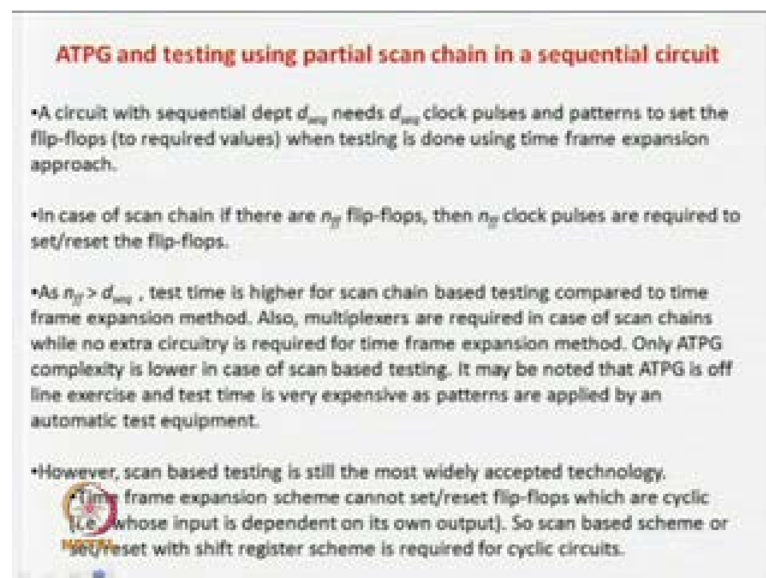

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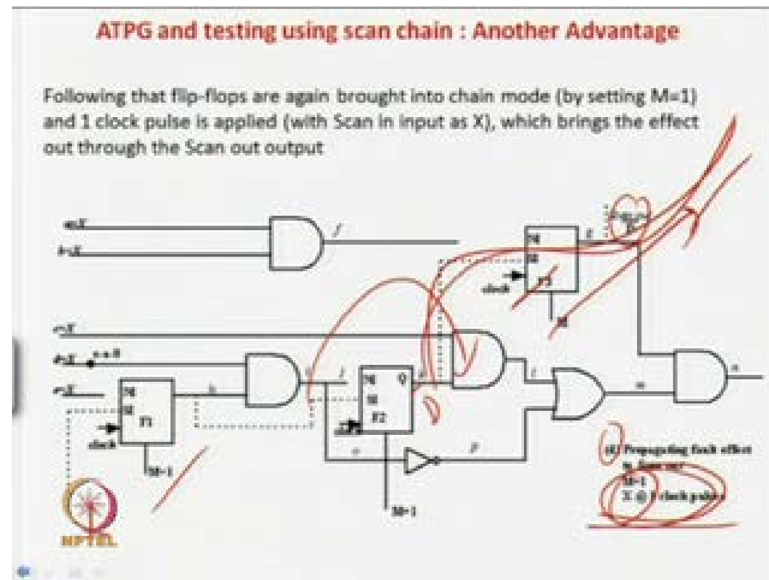

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So there is not much savings is that but, what we say greatly is that we have to perform a t p g are very small part of this circuit and if you do that there will be very very less chances of coalition and we will be always getting successful result. So this is a another very big advantage of combinational edge sequential circuit I mean D algorithm sorry as one is of scan chain base testing that you can perform a t p g or going small parts of the circuit and that will greatly reduce your chances of coalition. And almost all the faults you can test very easily in one go you can go for the a t p g.

So that is what you will see that is what you are going to that is what your one of the advantage though in case of a t p g using a scan chain, that is you have to do a t p g on a very small part of the circuit. And secondly like sometimes you will be saving in the number of clock pulse to set the flip flops.

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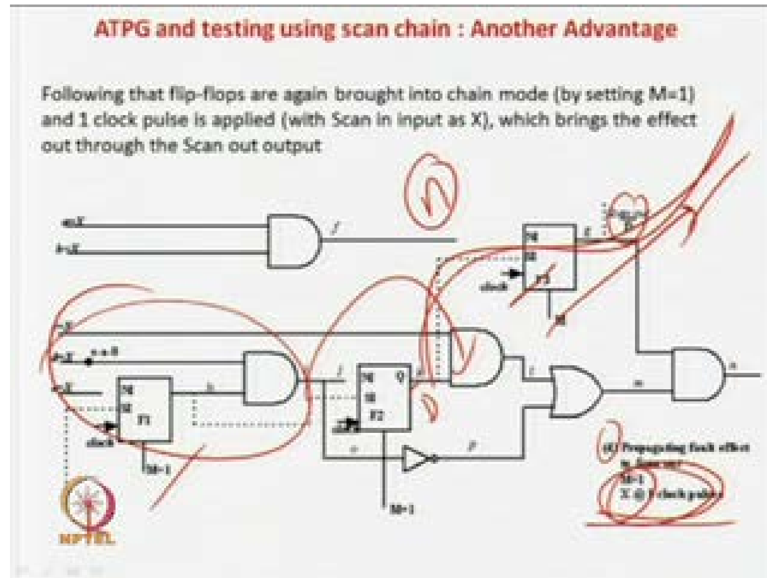

That is added two advantages of you this scan chains. So what people do people generally do not go for full circuit a t p g in case of a what you called scan chains base testing and they do the cone of influence and do it for the partial circuit and then the bring out the fault effect to the scan chain rather than bringing out by what you call the primary output. So now that so we have what we have seen, we have solve the problem we have got one advantage that a t p g has to be done on a smaller part of the circuit.

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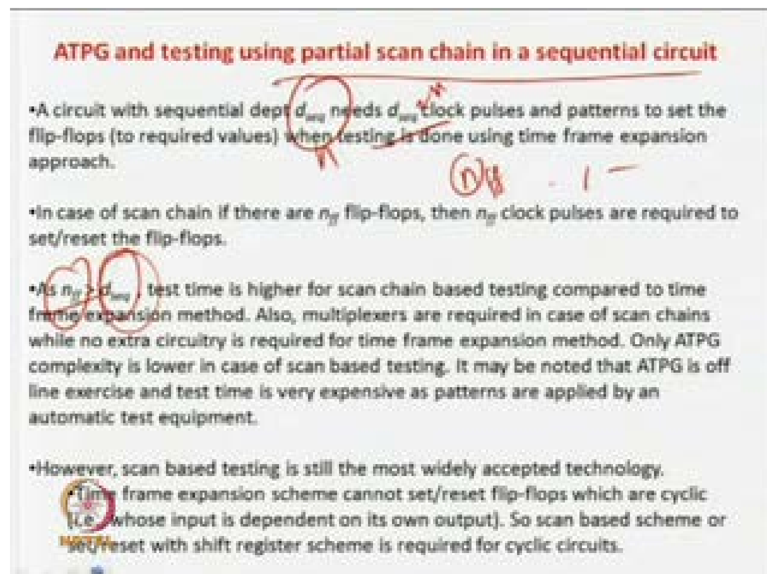

But one and one disadvantage still lies that. n that n factor that if there n flip flop circuit you have required n patterns either the control the flip flop the bring on the values not yet solved in that way. So we are try to solve it in deferent way it is actually call the partial scan chain. So we will see what you mean by partial scan chain. So if you just recall what do you have discussed in scan in the discussed in the previous last two last lecture in sequential circuit testing using what you called this sequential circuit using time prime expansion method.

So what we said that to set a circuit all the flip flop will be do not consider scan chain to set all the flip flop or reset all the flip flop in the circuit using time prime expansion method we require most d sequential number of clock pulse. Because if you assume that all the flip flops are connected in this fashion in your circuit, there may be sequential that is the last flip flop will dependent on the previous flip flop than it depend on the previous flip flop depend on the previous flip flop and so forth. So the sequential depth is maximum in this case. So we are required n if there n number of flip flop so sequential depth max can be n an what is the number of clock pulse is required to the testing a set or reset in case of pure to see I mean what you call this time prime expansion method d sequence, that is equal to n. But, that will be the worst case, when all your flips flops are connected in a chain fashion.

But generally if there n flip flops in the circuit in n flip flop in the circuit the d sequence is not be we convene the max and the lower case equal to d sequence n s f the number of flip flop will be equal to d sequence in the lower case. When everything is corrected in a chain, but, there can be also be the cases when or in the general cases the number of flip flops will be much much larger than d sequence. So if you are considering what do you what do I say if you are using a time prime expansion method then you required d sequence number of bits to set or reset the flip flop or d sequence number of patterns to set or reset the flip flops.

But, in case of scan chine you always required n. n if the n f is the number of flip flops you always required cannot n f s number of patterns to set or reset the flip flop or to bring out the values. So what advantage at least we could see from the what you call the previous approach of time frame expansion method that the number of patterns to set or reset the flip flops is d sequence this is not, in the most case it can be as hihg as higher the n f s but, always it will not be the case, always it may be less than equal to the

number of flip flops. So partial scan chine will take the advantage of your scan chain by approach and your time frame expansion method advantage also it will take because if is this if the I mean what you called this d sequence number is less than the number of flip flops number of flip flops, then you can use less number of time frame less number of patterns to you set or reset the flip flops.

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ATPG and testing using partial scan chain in a sequential circuit: An Example

- "Partial scan"--taking ideas from both time frame expansion method and scan chain method.
- The basic idea used in the scheme is to make scan enable only in those flip-flops which are cyclic and keep the remaining ones as normal.
- So we will have area overhead (because of MUX) only for those flip-flops which must be controlled directly and for the others, time frame expansion based indirect control can be used.

But actually if you remember in case of scan chain as we are discussing you required the single bids to set or reset the flip flops. But, in case of in case of what you call this time frame expansion method it is not bids, it is patterns which required to set or reset the flip flops, is the computationally very expansive. So will take a advantages of both of them and will see what we can do. So will again illustrate by examples.

So partial scan takes idea from both of these method, this basic idea scheme to make only scan enable in those flip flop with a cyclic and remember is normal. So what is the idea, there idea is that we have already seen in one example of the x or gate, say x or gate what we have seen so if your x or gate if the cyclic x or gate cannot be controlled and fault cannot be tested. So for that case it is mandatory that it should be having a scan to directly set or reset the flip flops. But, for other cases you may not have a scan chain, it can because it can be controlled to partial which can be controlled to time frame expansion method.

Because in time frame expansion method the off-line complexity is high. There can clashes and all those things are there. Because if you are remember that when you will computing what patterns are required to control this flip flops in a time frame expression method off-line computation approach. What we say the computation is very very high, why this very very high because may there may be clashes and all those things (( )).

But, once if you are some of found of pattern and the number of patterns required to control the flip flops will be much less then n. It will be equal to d sequence, which is much less then n in may most of the cases. But, in case of flip flops you do not require to patterns to control the flip flops, what you require you require bids. So you are getting of clashes and all is almost 0 but, if there n flip flops you have apply to n patterns to do this control. And so in the real time testing we know the chips are there..

So you require n number of bid patterns to set it. But, in case of partial scan or time frame expansion method you require only this sequence number of patterns to do this. So in time frame expansion method you do lot of time in the off-line, but, when you are going for online testing that is only one chip is plays in see to testing, so you lot do saving this test which is more important if you remember or introduction class. So we have to go so people decided that will take a advantage of both. So will give scan chain to only those flip flops where it is very very difficult to in the cyclic business in the flip flop is not control then you cannot test your circuit all those impossible stuff are there.

There will have mandarin to put the scan chain. Because you required to directly to control this flip flop. But for other cases if you remember where you can do control by the time frame expansion method you better use that because your off-line complexity is high because you cannot control the flip flops using bids, have to do by patterns in case of your time frame expansion method. But, still the number of these patterns are less the compared to n which is the this equals these much less than that.

So what is the basic idea, so we illustrate by example. So let us look at this circuit where this they are two flip flops over here. So this somehow the I have been removed and a t p g has been done. So now you can say that say to test this track at 0 fault over here, so what we require, so we required one over here so the value of will be d over here, so be a 0 over here, so you require a 1 over here that is a well known fact. So this 1 will be required over here. Now get a 1 over here it is obviously require a 1 over here, and to get

a 1 over here you require 1 over here. We get a 1 here. So this is 1. But, a big problem here occurs that to get a 1 at the output of this nand gate you require m also to be 1.

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ATPG and testing using partial scan chain in a sequential circuit: An Example

- Two flip-flops are to be controlled to 1; net *d* is to be made 1 and net *l* is to be made 1. Making net *d*=1 is simple and can be achieved by applying *c*=1 and a clock pulse.
- Control of net *d* via F1 is by time frame expansion method; as d_{seq} =1 for F1, so one clock pulse and one pattern is enough to control it.

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ATPG and testing using partial scan chain in a sequential circuit: An Example

- "Partial scan"--taking ideas from both time frame expansion method and scan chain method.
- The basic idea used in the scheme is to make scan enable only in those flip-flops which are cyclic and keep the remaining ones as normal.
- So we will have area overhead (because of MUX) only for those flip-flops which must be controlled directly and for the others, time frame expansion based indirect control can be used.

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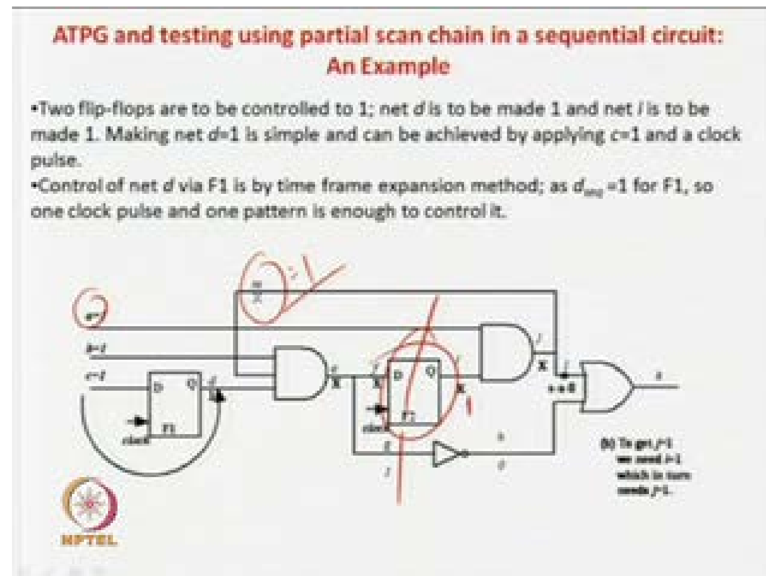

Now this is a cyclic business why? Because you see to get a m equal to 1 you have to make j equal to 1 that is very important. If j is 1 there only m equal to 1 and to get j equal to 1 you have to get m equal to 1. So this is a side line a cycle to get n equal to 1 you have to get j equal to 1 and to j equal to 1 and you have to make m equal to 1 so this is a cycle and this fault cannot be tested.

So what we have to do is that you have to apply a partial scan chain what is the partial scan chain? That is you have to somehow get this value to be equal to 1. So if that is the then you can use that time frame expansion method because here you require a 1 but, you do not require a flip flop over there you can go for a time frame expansion method and you can use this c 1 and in this put together this one but, this one controlling to be m is a very difficult problem because this is cyclic pattern.

So for this you have to require a scan chain or otherwise is not done because what you can do it to get a one over here. So what we can do is that you can somehow make this as one by using a scan chain and this input is directly controlled to be 1 then if you apply this then only m can be directly 1. So using this flip flop only scan you can get m equal to 1 but, for this flip flop you do not require a scan chain but, you can directly time frame expansion method and your job is done.

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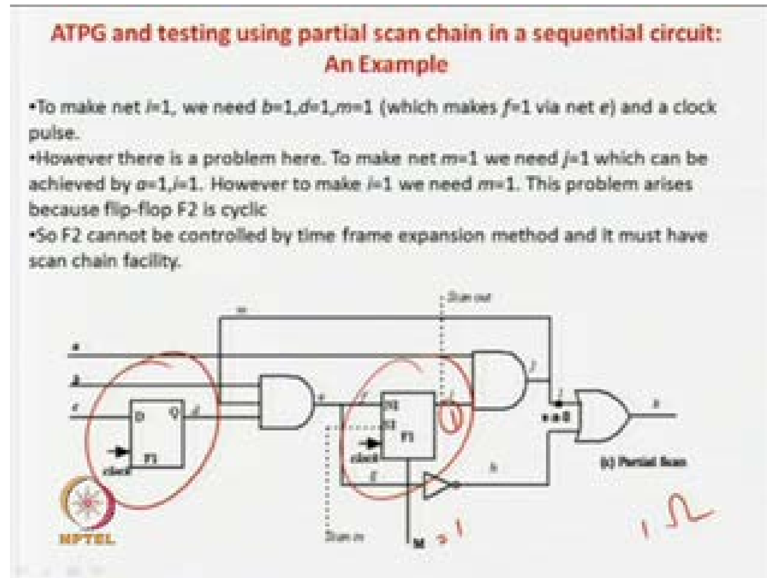

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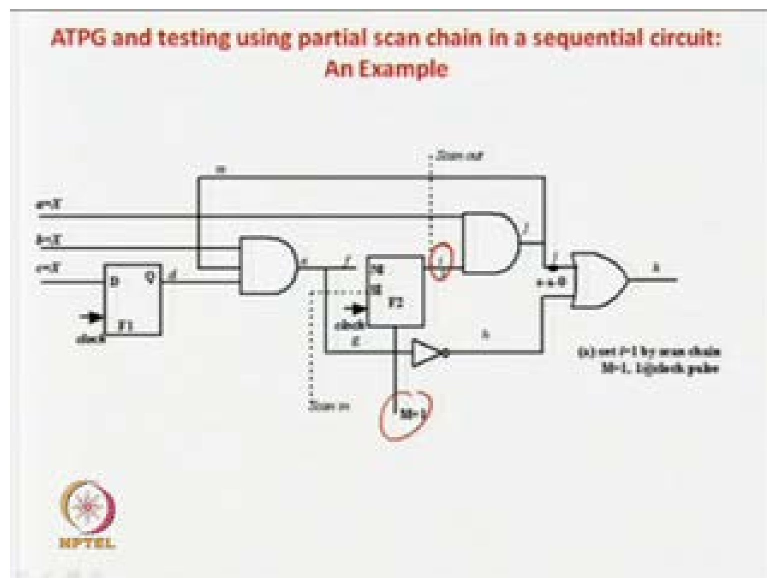

So let us see in stepwise how can do that, so by time frame expansion method you just you make sorry j equal to 1 we get j equal to 1 all this thing has been explained. So let us see what we do so first what we do we make a scan chain. So this is your scan frame and this is your non-scan flip flop that is why we call it is a partial scan chain. So this is your partial scan. So in this case what you do you firs make m equal to 1 you can do then you apply one clock you apply a one and a clock pulse so once you do you get a i equal to 1 definitely will get.

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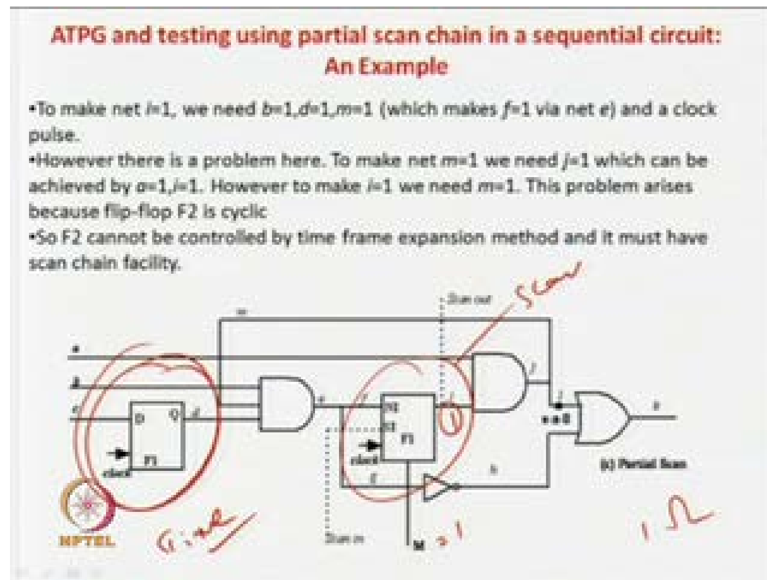

Next what you do? That is what has been done you make m equal to 1 apply a clock pulse you get a one over here that is what is be done over this. Correct? This is what we are saying that this we control by time frame and this you control by scan. Now this is first step. So you just 1 equal to 1 one you get over here.

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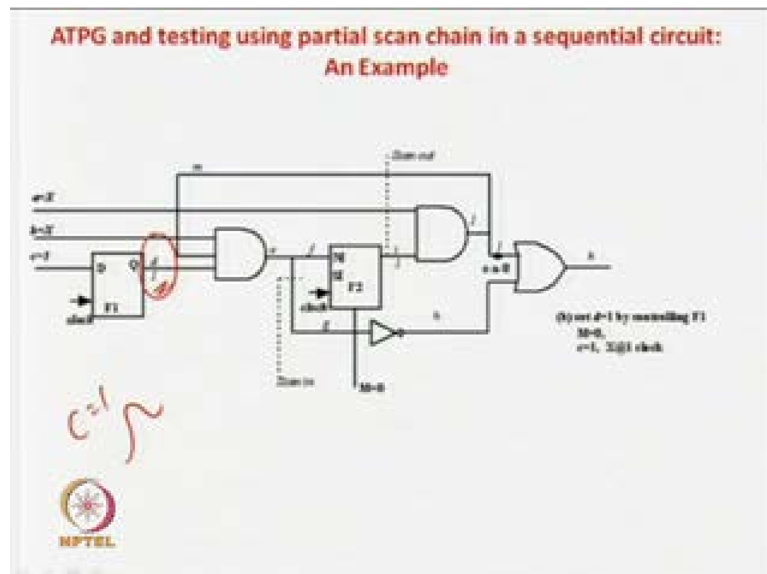

Now what you do? Now you make m equal to 0 so the circuit comes to a normal fashion. Now what you do? Now this is what also requir a one over here so for that there is no

scan chain will not use a scan chain has already said will be using time frame expansion method. So in this case you make C equal to 1 and apply the clock pulse.

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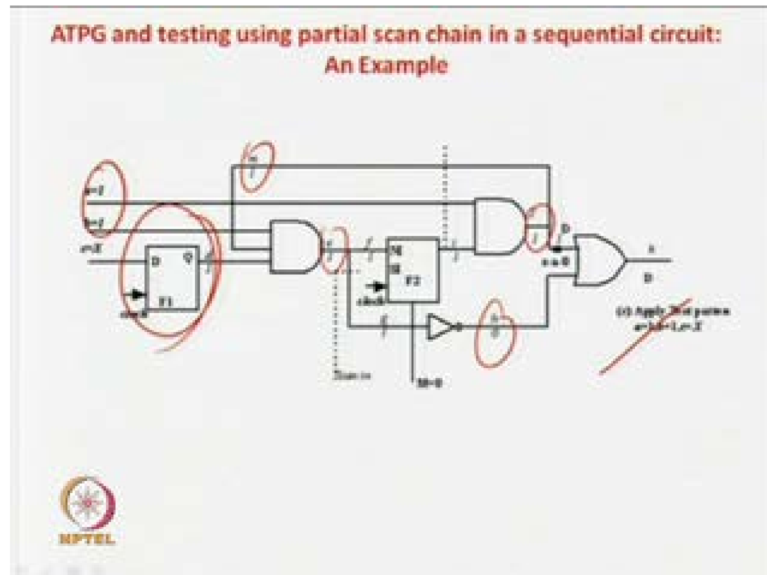

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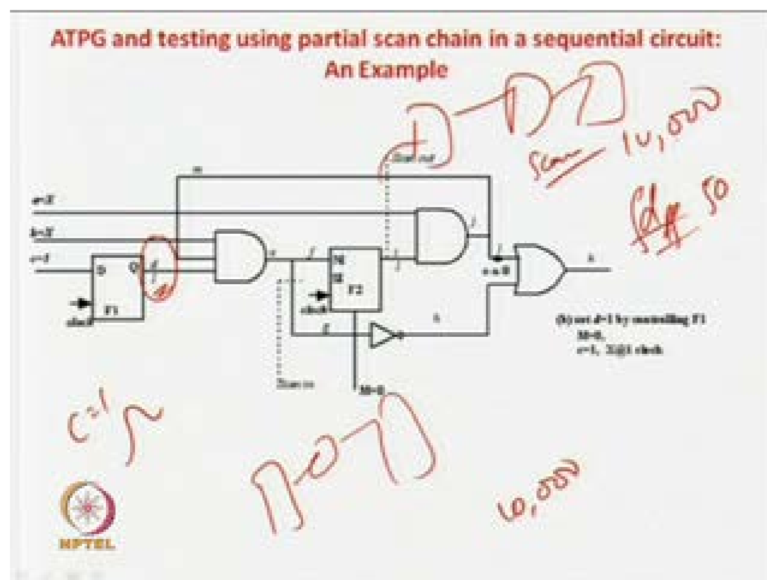

So if you apply the clock pulse what is going to happen? We are going to get a 1 over here that is very obvious. Now you get a 1 over here you get a 1 over here and then you apply a 1 over here and a one here. So if you apply a 1 over you get a 1 over here and then and you get a 1 over here you apply this you get 1 over here this is 1. So finally, this will also be a 1 this will be a 0 and your circuit is going to get tested.

So effectually what you have to done so in this case you do not see much advantage of your this this this this direct primary input flip flop so do not directly get the advantage of what you can see whatever say in to highlight but, what is the basic concept which I was going to discuss on the partial scan chain you have to see it a bit more carefully. So what is the idea we have see that if there are so say if will have use the direct scan chain based approach so what would have been there say there would have been 10 flip flops over here something like this.

So what I mean connect say these are the 10000 flip flops in to change. So what we have to do? So you require10000 flop pulses to set or reset them as required. Correct? But, let us assume that the sequential depth that is d ff sequential depth is say for this flip flops are there say 500 or say in say 500. So what you mean by them that means all the flip flops are not actually by combinational circuit this is a scan. So whenever your correct doing a scan chain then what we have to do? You have to connect all the flip flops as to remember all the flip flops has to be connected in a chain.

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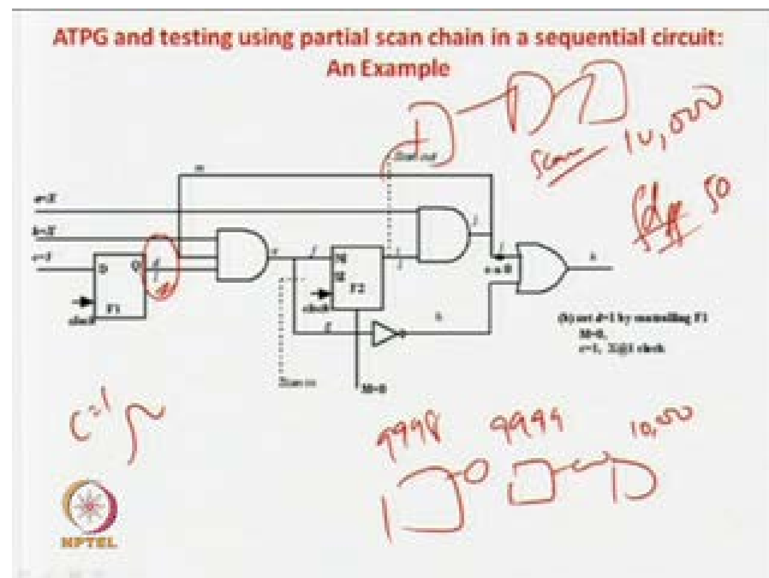

So if there n flip flops you require n patterns to set it. So there is only one flip flop we have to take one pattern. So if there are another 10000 in the scan chain you require 10000 one flip flop pulses to do that but, these sequence there the sequential circuit is must less than that because in the normal circuit topology if you consider all this flip

flops you not be depended another like the 10000 flip flop will not depended on the nine nine nine nine'th flip flops

Similarly, the nine nine nine eight'th flip flop will not be dependent on this. That is it will not require so what can happen is that some of the flip flops will be dependent on the other sense so forth. In the average case you may have 10000 5 1000 or 800 or 100 or something which is less that sequential there that means there are some around say some 500 flip flops there combinational circuits in between.

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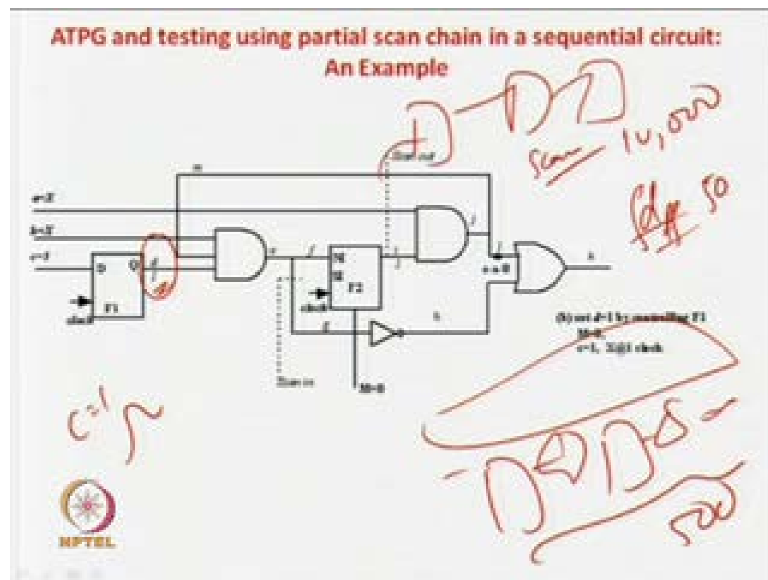

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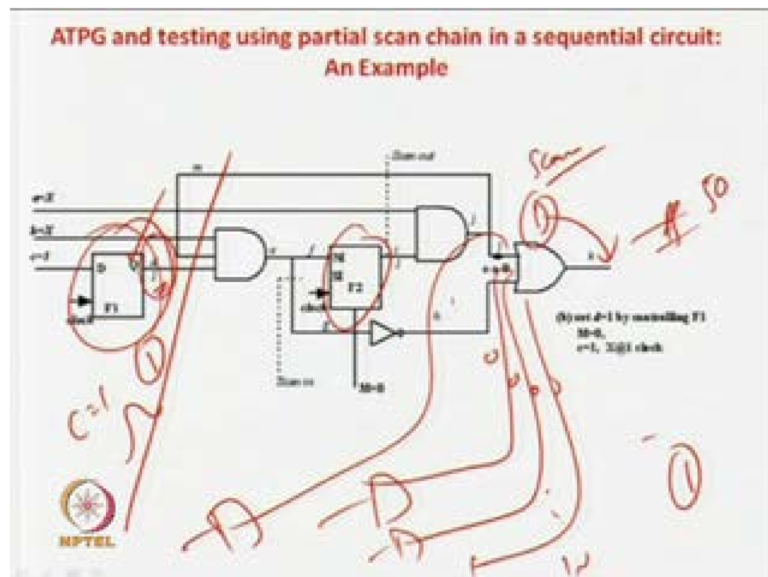

So this 500 flip flops are depended last flip flop depended on the precious so and so for there can be another separate similar chaining like that so your sequential depth will be different or you maximum sequential depth will be much much less than 10000.

So what we can do is that all those flip flops will chine did not directly control because of the cyclic business we keep them in the time frame expansion method. So in this case if you consider this is the only flip this is the dangerous flip flop is sequential depth is 2 because this if you call a output is dependent on this one here this sequential depth is 1. So the overall sequential depth of the circuit is only 1. So what you have to do? you require one pattern to test this one so had they have been example just like triple at the example so i am just considering that this is a this is a or gate with several other say 10s of other flip flops.

So other 10 flip flops are there just consider this. So other 10 flip flops are there say 100 say 10 flip flops others are connected to this one. So there all other flip flops are there so the other 10 flip flops are there kind of dot dot dot and they all connected into the primary input. So what is the sequential depth? The sequential depth circuit is to for this one because again this is a dangerous flip flop kind of a thing because sorry dangerous part of the circuit for testing because the feedback. So this have to control by scan no option about it so done. Now what considering this and all this chain flip flops what is the sequential depth? The sequential depth is again one because this flip flop is dependent on primary input, this is primary input dependent and so forth.

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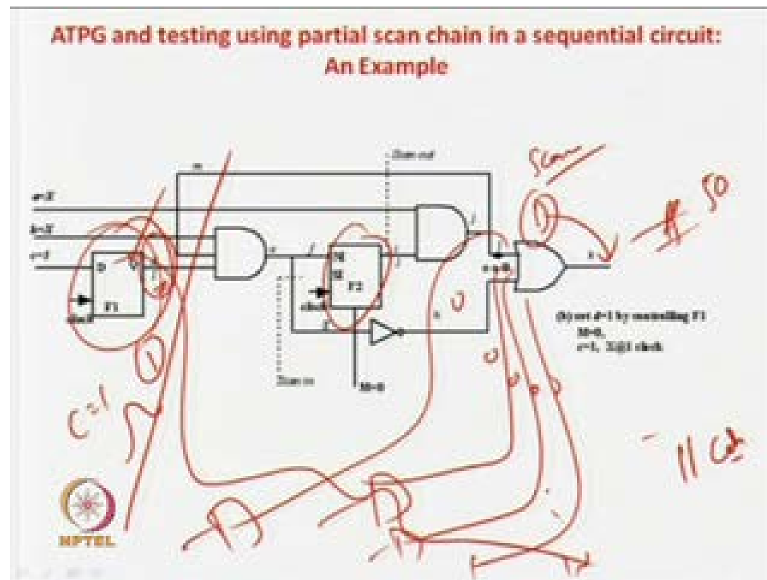

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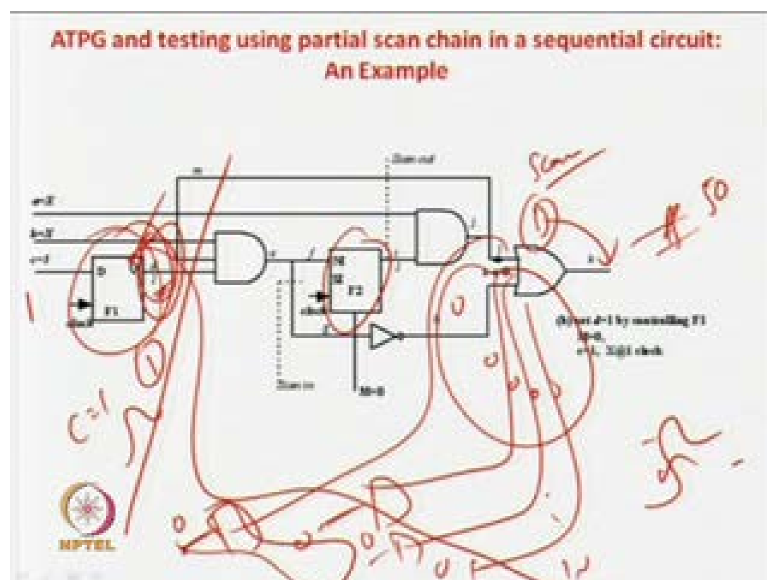

So if you require a scan chain to set all the because is a or gate to propagate the value of D over here. So all this output should be a zero. So if you the scan chain then what I have to do you have to make a scan chain from all this flip flops to this one. So there will be 11 flip flops in series so, you require 11 clock pulses to control this one but, the sequential depth is not 10 or 11 in this case this sequential depth is one because all the flip flops here are dependent on the primary inputs. So what you have to do? You have to apply say in this case a one is require so you apply a one over here and all 0s here you apply and you apply a single clock pulse. So this is what time frame expansion. The

pattern is 1 0 0 0 0 10 0s so once you do that you will get the output of 0 over here and a 1 over here and your testing is done.

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Questions and Answers

Question: How can test time be reduced for the circuit below with scan chain ?
Answer: The circuit has a single scan chain with three flip-flops. So time taken to set/reset all the flip-flops is three clock pulses. To save test time the scan chain can be divided into multiple sub-chains with separate Scan in and Scan out pins. In this case we have divided the chain into 2 parts—one has F1 and F2 and the second has F3 only. So we have two sets of Scan in and Scan out pins. The design is illustrated in the figure below. Now both the chains can be loaded concurrently. So, only two clock pulses are required to set/reset all the flip-flops.

So the so have you been using scan chain so you have to control in this way but, have if you are directly using a what do you called this time frame expansion method then only one if the sequential depth in this case is one. So you will get a one pattern to do that but, here this assumption was the simplistic that all the outputs or inputs of the flip flops or the primary input. So the controllability was easy but, if in you can have a combinational circuit then you have to do some more competition to do this do it so, what is the advantage of the partial scan we have got? The partial scan chain advantage which is got is got is that you may not require n number of patterns to control the flip flops. So that part point is also solved. So what we are doing but, again it is not you are not you are not being able to solve all the problems.

So what is going to be the ideal situation? The ideal situation what has been that we could have totally thrown over the time frame expansion method, we could have already taken this scan chain based approach and then we could have solve that you do not require n number of patterns to set the flip flops but, that we could not do because if you want to use the scan chain totally your scan chain approach then the advantage one at greatest advantage is that you do not require to do a t p g on the entire circuit.

You can take what you can do? You can take a t p g for the nearest flip flop and then you can apply your test pattern you can do your a t p g for the small circuit and take out the value through the scan flip flops and then it is done but, again for driving I mean for setting the flip flop, recording the value at the output of some flip flop and again bringing out to the scan chain will require n number of clock pulses.

So that could not be solve directly using a scan chain so indirectly what people have taken the for that is the best solution that partial you take flip flops for scan able and partially you take them for what you can called this time frame expansion method because, time frame expansion method can be solved, we require less number of patterns to do this only the of line complexity may be high, you know set the flip flop there is only de sequence the de-sequential depth that much is required. So you do that and then if there is some cyclic points in your circuit for that you require a scan chain to solve the problem.

So this is somewhat is the we have want for a trade of and this is way combinational circuits are tested that you go for the sequential approach put partial scan for the flip flop these are not directly controllable of because cycle city cycling problem and for other you use the time frame expansion method and you do that. So this one of this I mean now there can be lot of tradeoffs. So you can think that I will keep only few parts some because if there if the if one scan chain becomes very very long then you can have some problems. So you can think of again going for another hybrid business that some of the circuits some of the flip flops even if they are I mean they are non-cyclic I can go for a scan business because time frame expansion method may be too high in complexity but, so with them I mean see you just see in the question and answer session.

So will come to question and answer ask this questions so two approach. One approach is full scan based technique and second approach was partial scan and partial what you call sequential problem so can there the any third hybrid approach for this one so we will see. So how can test time be reduced for this circuit shown below. So this is another circuit below so everything is scanned scan based. So, now how can you reduce this test time? So if there 3 flip flops so you require 3 clock pulses to set the flip flops because this scan chain will require 3 clock pulses how can you reduce it? So you can say that there is no cyclic city in this business and so what we can do we can go for a what you can call this time frame expansion method.

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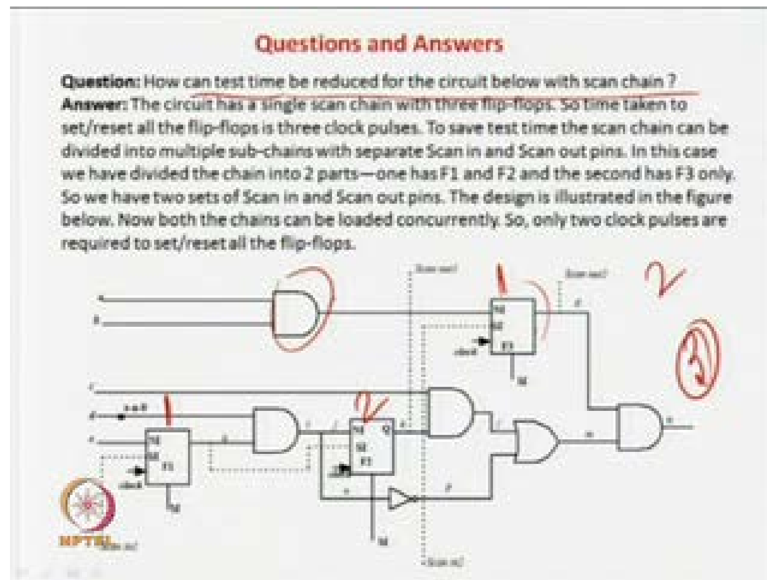

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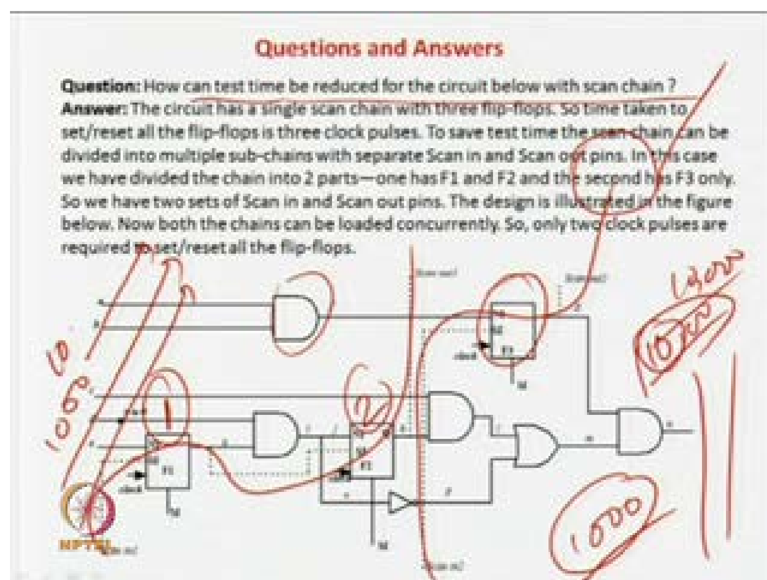

So time frame expansion method what is the sequential depth of the circuit for this, this is two because this is dependent on the flip flop here the sequential depth is 1 and for the circuit is sequential depth is also 1 because this directly controlled by this one. So you require two patterns to set or reset the flip flops but, in case of this for time frame expansion method but, if you are using a full scan chain then you are require three patterns should be so you can say that I can do that but, for that you can tell that because there is some because that in that case in time frame expansion method then your controllability will not be just by 0s and 1s it will be patterns required to control.

So there will be of line complexity but, still you require only two patterns to set or reset the flip flops but, people will have then go for a third approach in which this we called that multiple scan chain in what case this multiple scan chain? This say that do not make a very very long scan chain why we require three pulses to control it? We require 3 pulses to control this flip flops because they are 3 in chain so you say that why are you making such longs scan chains because we will directly want to avoid this time frame expansion method because of the mathematical complexities.

So what this say that make multiple scan chain so what this guy he has done? So he has made one scan chain over here, another scan chain over here. So in this case if you do then they are two scan chains so you can parallel load them and shift the data. So in this case there are two patterns so you require so you can load one here and one clock pulse we load here, second pulse we load this and parallel with this you can load this so if there is another flip flop over here so this two can be loaded here.

So if you are say 1 10000 flip flops say so if you make say one say 10 scan chains so you will have 1000 flip flops in 1 load. Now you do not require 10 10000 patterns to set or reset the flip flops only if you require 1000 to this because you are loading in parallel. So there is one thing that is one greatest advantages how approach which is now widely accepted we will generally do not go for what you called this time frame expansion method and partial scan

What people rather do is that they go for multiple scan chains because I mean time frame expansion method is very difficult to do of line and sometimes there will be clashes and you do not require patterns, you do not require bits you require patterns to control them and so forth. So what people do is that they go for multiple scan chain. So they breakup the long chains into partial chains and you load them but, there is a problem. So if I say that so if you make 10 chains then you require 1000 patterns to bits to control them.

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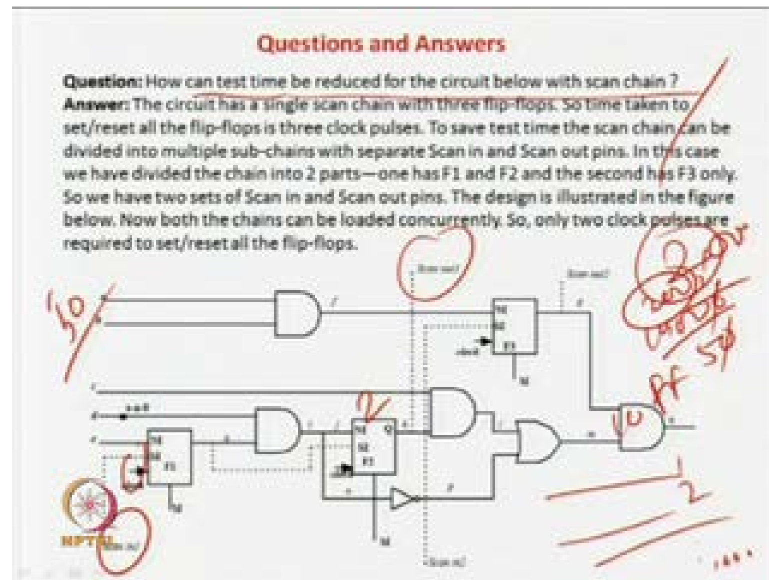

So let us say that I make 1000 such chains. So this 10000 I bring make 10 10000 10000 flops were there. So I bring 1000 chains so you require 10 pattern flip flops for chain. So you are very happy. So you require only so there are each of this chains have 10000 flops sorry you make 1000 chains. So if I if you make 1000 chains then what is going to happen? If you make 1000 chains then if you are make 1000 chains like this say chain 1, 2 dot dot dot.

So 10 1000 chains you make so each one we have already 10 flip flops. So already 10 patterns are required or 10 clock pulse are require to set it. So your job is that but, again here again there is a big problem that is pin out problem is coming for each scan chain you have one scanning pin and we have one scan out pin or you can assumes that the clocks are same but, for again for each scan chain you require pin outs extra.

So if you have 1000 scan chains so, you require 2000 extra pin out which is again very difficult. So always there is a tradeoff. So you can think that I will make say around 50 scan chains. So there will be 100 pins so in a very very complex cheap you can say that 100 pins for testability may be but, this was the higher range. So it will be 10000 by 50 if you go so you get it around 200 clock pulses to do that.

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Questions and Answers

Question: How can the flip-flops themselves be tested in a scan chain based testing?

Answer:

An advantage of scan chain based testing over time frame expansion and shift register technique is the ability to test the flip-flops in the circuit under test. A toggle sequence, 00110011 . . ., of length $n_f + 4$, where n_f is the total number of flip-flops, is applied at Scan in. This sequence produces all four transitions $0 \to 1$, $0 \to 0$, $1 \to 1$ and $1 \to 1$ in all the flip-flops. The sequence is brought out through the Scan out pin. So if a correct toggle sequence is observed in the Scan-out pin, then the flip-flops are working normally. It is shown in stuck at fault model that toggle sequence covers almost all stuck at faults in the flip-flops.

So again always there is a question of tradeoff that what they will do, what will achieve. So testing is or we are said design testing is always about what you gain and what you achieve. So either if you go for totally time frame expansion method then if and if there is no cyclic business in the flip flop then you are at the best though no extra circuit very less number of test patterns to go over testing but, again the of line complexity is very very high and you require patterns to do that.

Then if you go for full scan chain based approach then you require a single scan chain n number of patterns to set the flip flop. So more test time is there but, here the chances of collision etcetera is almost zero because we will take small sub circuit of the circuit part of the circuit to do this scan chains when testability a t p g or small very small sub circuits and then you are but, you require n number patterns to do that.

Then you can go for this partial scan I mean what you can call partial scan chain. So they are here again there is a mix of scan chain and what you call time frame expansion method. So complexity is there but, there you can again you can go for another simple approach you can go for n different breakup the long scan chain into partial small scan chain. It is a very good approach but, again if you are making too small scan size of the scan chains and more number of scan chains you are bringing out but, breaking the larger one into very very small number of very very small size larger number of scan chains

and pin outs will be have. So you have to select the best and the worst out of it which you feel as the best for your design this is how it goes.

So again next question will see how can the flip flop themselves be tested in a scan chain based testing. So if you remember we say that the all fall model for sequential circuit we did not consider falls inside the flip flops because we say that if it is there then your combinational circuit sequential circuit may be converted to virtual what you called sequential circuit can be converted to virtual scan I mean virtual combinational circuits because the flip flops may not change state it may become static and lot of other complex issues will be there making a t p g very very complex.

So we assume that there is no fault in the flip flops but, still we have to trace the flip flop. So how can you do that? Scan chain can easily do that so, in in scan chain base testing if you want to test the flip flops only then you just go for this scan mode make m equal to 1 do not think about making m equal to 0 do not do that make its only a scan chain and then pass this kind of sequence 0011001 is alternative sequence. So there is two 0s and two 1s then 10 01 so this type sequence would give. So you will gain get this type of transition at the output of the flip flops from 0 to 0 from 0 to 1 from 1 to 0 and from 1 to 1.

So this type of transitions you get at the output of the all the flip flops. So if you get them correct you know that your flip flops are fine that flips flop is to toggling fine and so your flip flop can be easily testable.

So scan chain in the end another greatest advantage of this scan chain is that you can also test the flip flop. So again and the end if I emphasize that if there is one very good design or one of the best designs for testing which is been ever developed. So I will say that it is the scan chain because he solved most of the problems that is related to your sequential set circuit testing was hold by the scan chain.

So with this we come to end of this module and this lecture. In the next module and the next two modules are remaining in testing what what we will see there? So next we have seen that this is your of line testing. So in scan chain base testing or whatever we have discussed till now so patterns are generated and once your circuit has been designed so it has been fabricated its place on the tester, your tester will apply those patterns which you have determined throughout the lectures.

We have discussed so some patterns are decided, so those patterns are applied by the automatic test equipment you get the response and you say whether the circuit is normal or faulty if it is normal it is shift to the customer otherwise it is thrown out but, now say for example, you have send your chips now it is put in my laptop or put in the video camera or put in the p c u you are using again it may go back because now what is chips are very sophisticated. So it may happen that even during operation it may have some failures. Now how to test them this is something called built in safe test.

So whenever your circuit starts its operation so it will be testing itself right? So that is one very important paradigm of testing. So that is one part which we are going to see and also there is one thing which are not consider that is the memory. We have considered that sequential circuit we have considered combinational circuit but, we have not consider the third very important an in of circuits which is the memory. So in the next few lectures will be looking at built in safe test and memory testing which will complete our course on this testing.

So thank you with this.