Design Verification and Test of Digital VLSI Designs
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Module - 10
Sequential Circuit Testing and Scan Chains
Lecture - 2
Scan Chain based Sequential Circuit Testing-01

So, welcome to module ten, lecture two, three, so this is on a scan chain base sequential circuit testing. So, if you remember in the last lecture that is lecture one of module ten, so what we have discuss we discuss that sequential test circuit testing as compared to a combination circuit testing using the D-algorithm or sensate propagate and justify approach. So, what we have see in case of combination circuit you sensitize propagate and justify, so one pattern is enough to dictate a fault, but in case of sequential circuit what we have seen that the basic architecture of a sequential circuit.

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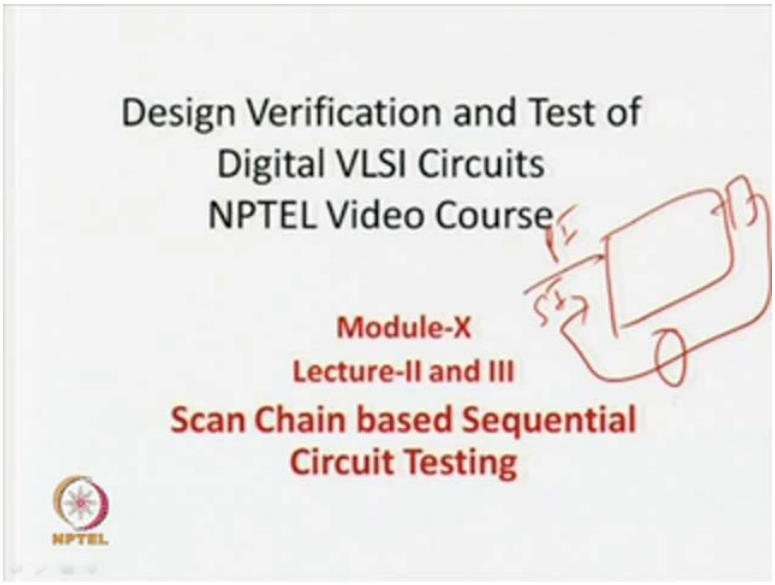

You have some primary inputs and there is a state register and there is some feedback from that and actually this is call the secondary inputs or virtual primary inputs, so as this set up inputs are not directly controllable because there output of the state registers. So, you cannot have single test pattern to test the circuit because you require multiple numbers of test patterns to be precise if this sequential depth of the number of flip flop circuit is sequence. Then, you require the sequence number of test patterns to control in

the worst case to control in all the secondary inputs, now once they are controllable, then you can apply the primary inputs at test your circuit.

Similarly, this output of this is also not directly observable, so make it to observable directly, so you have to again propagate the value through some of the flip flop you take set of another time. So, I mean a so single test pattern, we have already seen is not enough to test the sequential circuit by sensate propagate and justify approach. So, first you have to use the sequence level of number test pattern to control the sequence secondary inputs, and then apply primary inputs.

So, the sequential number of patterns plus one pattern and the again also with output propagate the value the outputs though observe them. So, more than one number that is d sequence plus 1 or some plus k number test patterns are required to test a sequential circuit. So, you know that wherever we are a going for, what do you called this ATPG based testing with sequence sensate, just a sensitize propagate and justify approach and many times, you can lack to inconsistency, so leading to inconsistency.

Again, you have to back track, so you assume that as a sequential circuit testing is order of complexity of combination circuit testing in to number of test patterns should be applied. So, if you have five things that you have also discuss on the time frame expansion method that if there d sequence number of depth of the sequential flip flop. Then, you may required to go to d c minus d sequence to zero level of time frame that is d sequence number plus one time frames are required to do this.

So, you can understand there any last time frame so every step was successful, but in the last time frame it will be inconsistent. Then, whole work is gone and then again you have to start with a fresh one, so because of this inconsistency today we will see what we can do. So, this overall complexity of more than one number of test patterns can be avoided or can be minimized in sequential circuit testing. So, effectively what we have to do, so effectively you have to somehow indirectly or directly control and observe this secondary inputs and secondary outputs respectively if you can do that, then our problem is solved.

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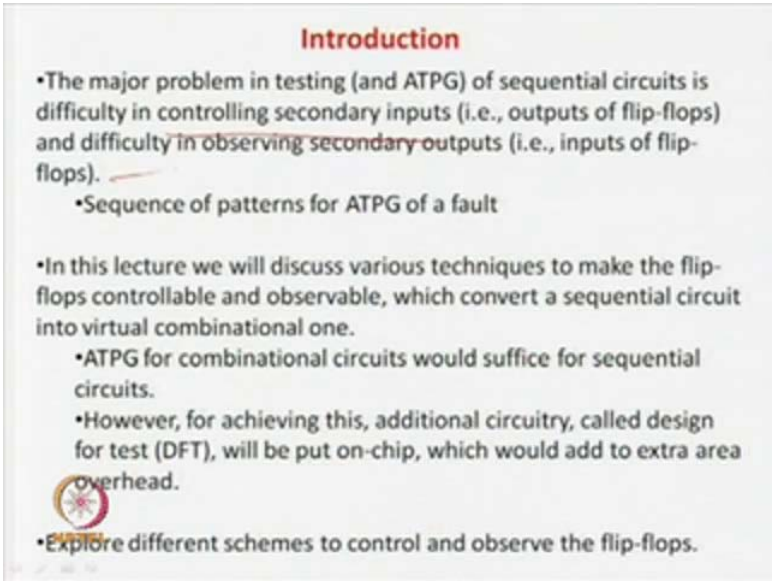

So, let see what will do so as in the introduction we discussing the major problem of testing of sequential circuit is difficulty in controlling secondary inputs and difficulty in observing secondary outputs. Somehow we have done that explicitly or I mean using from other circuit is this is called design for testable or some other arrangements we have to do this. So, that is why we require a sequence of test pattern for ATPG of sequential circuit which you want to make it to one kind of a thing so in this lecture what will do will see how what we can do in this circuit level.

So, ATPG for combination circuits would suffice for sequential that is somehow we have to use ATPG algorithm for sequence combination circuit and do that and say that it is done for sequential circuit. The part which has to control indirectly we use some other technique which is actually call this scan chain and we will see to control them indirectly.

This is this is this is one example of a scan chain design where we in call court concord a simple designs are great. So, if we are doing very complex design, we do a lot of flip flop, lot of gates and all in the very high chances your design is improper or inefficient, but good designs are always simple that is court concord thumb ruling VLSI.

If your design is very simple and you are solve the problem, then you are then you are the greatest engineer, so great designs are always simple. So, we find out that how this night male problem of testing one fault you require the sequence number of patterns to

test the sequential circuit was solved by a person who develop a scan chain. The design was extremely simple, so this is one proof that you can do very elegant design simply.

So, actually convert it all the c combination sequential circuit to combinational circuit and then combination circuit ATPG algorithm suffice for everything. Then, slowly we could do away with this sequential test pattern generation with time frames and all and they last there important and combinational ATPG with design for test pattern modify in the circuit. So, you can directly you can directly control the secondary inputs and secondary outputs observability indirectly using some kind of extra circuit then came into picture. So, for that to achieve that you have to put some extra circuit on the chip which is called DFT, so will be an extra over it.

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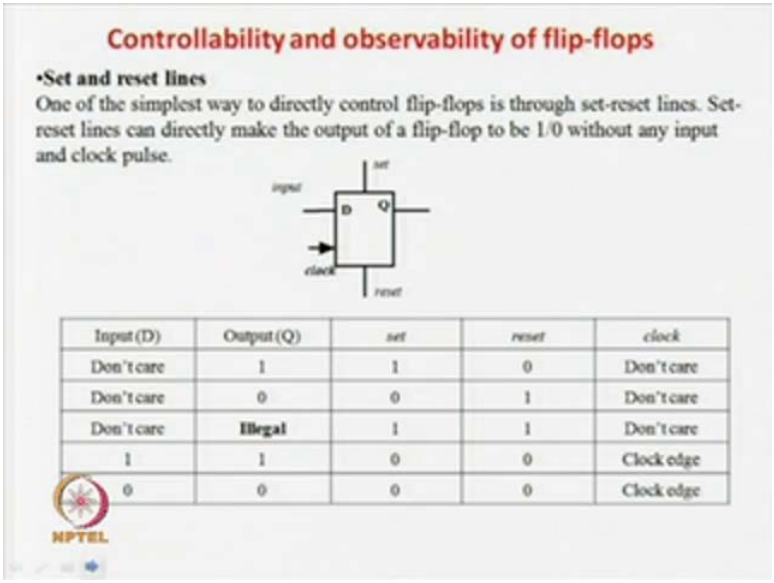

Anyway, that extra over it problem is not much as will see then compare to the off line headache of for one fall generating this sequence number of test patterns. So, how to do that, so one major problem we have seen in the last lecture was to control the output of the flip flop which is nothing but your secondary inputs. So, how can you do that, so one very simple way of as we already discuss in our lectures will be using d flip flop as they are standard use in all BLSS circuits.

So, one way how can you indirectly there is you have to direct indirectly or directly what happen, you can see without using explicit test patterns directly, you have to get excess to the flip flop somehow. You have to control them, so indirectly if you want to control

them, I mean you can you can apply this sequence number of test patterns and go for time frame expansion. You can do it, but here what we are seeing that that these indirect controls we want to do it somehow directly where if directly somehow excess all flip flop and do this.

So, you can understand that if you can somehow get hold of the set and reset pins of the flip flop, then you can always what you can called take control of the flip flop. We will see an examples if you can directly somehow get excess to the set and reset inputs of the flip flop. Then, you can directly say make them 0 over 1 and require for the secondary inputs, so if that time we did not go for this a sequence number of test patterns do make the make this secondary inputs controllable indirectly. So, we can use that, so what is this truth value of the d flip flop you can say.

So, if I make you say reset equal to 0 if you say, then you are and set equal to 1 if you set, then you are going to set your flip flop. So, what is the idea input you do not do not care at that time because you directly controlling the flip flop the set and reset and clock is also would not require. You will directly get the output q s 1 and if you make the reset s 1 and set as 0 and what is going to happen you will directly get the output of the flip flop as 0, you did not apply clock. All those things somehow if you can control the set and reset line externally, then you can directly set this secondary inputs as you require and for the set and reset is not allowed.

It is the illegal condition, but now if you want to operate normally on your flip flop then you set make reset equal to 0 this one and if we apply a 1 sorry if we apply a 1 when you set and reset a 0, we apply a clock age. The next stage you will get one those d flip flop you apply a 1, then you apply a clock age your set and reset should be 0 at the time and next clock age will get a 1 and 0. For the same case, we give input is 0 and apply a clock first your set and reset should be 0, the output will be a 0 is a normal operation our flip flop.

If you want to directly, but not if you want to the clock first to control this flip flop, then you know that this is input there will be lot of combinational clouds, there will be angle set of the flip flop here. So, you require the sequence number of test patterns to if set this inputs, so that you get the design base output as this one, so if you want to get a 0 over

here, indirectly you have to set a 0 here. For that, you may have to conclude this flip flop and so which you require d sequence number of patterns.

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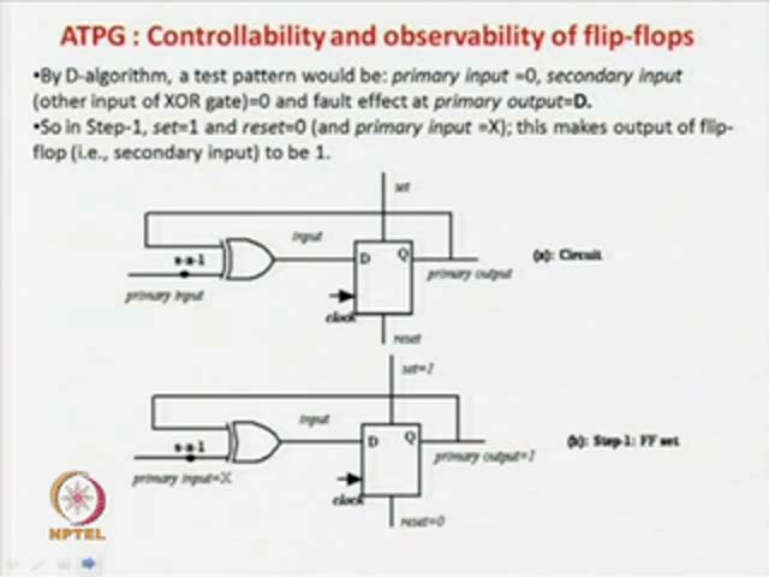

Now, if you somehow control this and this, then directly you may reset equal to 1 and the set equal to 1 you do not if it any it apply a clock first and you will get the output as 0 which is required. So, let us see what we what you gain this you can directly do this, so if it remember by last lecture we said that this is the circuit. You can think that the set and reset lines were not there, so the idea was we are asking can you test this fault, then you find out that the set and reset lines are not there, it was in the question and answer session in last lecture.

Then, we found that this fault cannot be tested because you know that the how this output is react this output is x kind of a thing and for this stuck at 1. We have to apply a 0 and if you know that this is 0 slash 1 and in the case of XOR gate this output will be XOR x prime because x was 0 in case of XOR gate output is the output is whatever is the input here will be the output.

You can apply a 1 over this for this is a fault this x is become x prime, so it will be x and x prime, so never you can get any complete value and you cannot able test your circuit. So, that was the case, now we can see that use of the set and reset lines you have, then what can you do, so for example we know that all the lines are x for the time being, so this is the x, this is the x, this is the x.

So, what we will do, so what we can do that, now we can we have a direct excess with flip flop, so you make set equal to 1 and reset equal to 0. So, what it to wants to do, so without apply in the clock also you have this output will be a 1 this is the output 1 and this output is the one because we have set the flip flop directly using set and reset. Now, this is stuck at 1, so what you can do that so you have one over here you have one over here, so and now if this is this is you got just by a, what do you do the first effort you have to done first step you apply set equal to 1 reset equal to 0.

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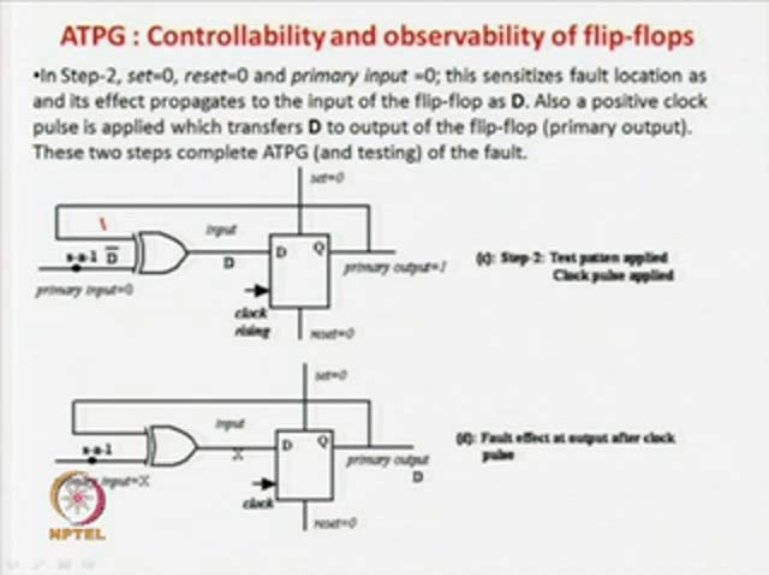

So, you get a 1 over here get a 1 over here, now what you do you make set and reset equal to 0, so what will do happen now the d flip flop will be operating in the normal clock mode. Now, this is a 1 over here, so what you have to do you can apply primary input 0, so normal case zero fault case 1 because this because the stuck at for. So, it is a d over d prime over there and we know that in case of XOR gate if the other input is one then the second is prime is inverted. So, you get a d over here know what you have to do, so this you make 0, now what we can apply is you apply the clock pulse over here.

So, this output will come out of the primary output which will get here and the fault is tested as now become testable when you are using a line. So, this solves the great deal of problem that some of the faults which are un testable if you considered your circuit without the flip flop, sorry without the set and reset know became testable secondly one

more thing is there. So, that again we will see in the other example, so what are the advantages of controllability and observable of flip flop with what you call this.

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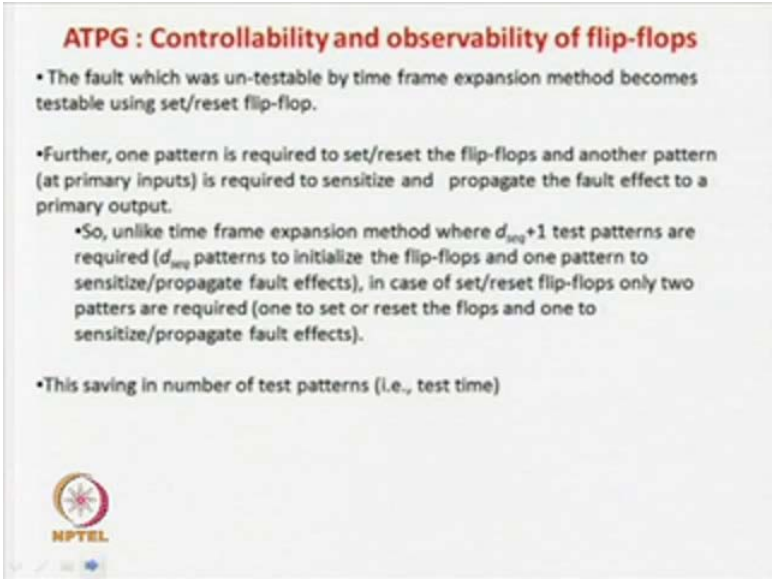

A fault which was un-testable by the time frame expansion method last lecture is now becoming testable using the set reset flip flop that is why so secondly. So, what we have seen is that e, now only one pattern we will see only one pattern is required to set and reset the flip flop and propagate the effect to the output. So, the idea is there if you look at it so only one pattern that is actually that you can call this set equal to 1 and the set equal to 0 that is one pattern will which will set the flip flops. If there more number of flip flop for all of them we have to set and reset is required and there only one pattern will dry your answer to this one.

So, indirectly what you are going have if you set and reset lines in your flip flops one pattern is required to set and reset the flip flop as required for your secondary inputs and secondary output kind of a thing. Secondary input controllability you can directly get by setting as the resetting the flip flops directly by the set reset pins and now one pattern is required to be applied which will sensitize the faults and propagate the value to the some flip flop kind of a thing. Now, instead of these sequence patterns to initialize the flip flop you can have, so unlike time frame expansion where you require d sequence minus 1 patterns required to what you call sensitize propagate in justify.

So, in this case only one pattern is solving the problem or you can call 2, only 2, basically to set the reset of the flip flop and 1 to actually sensitize the fault effect that is by the combinational test pattern. I will get that is this pattern, actually this is you are applying a 1 0 over here. So, this pattern is by combination ATPG and the other set reset you are doing by this, sorry this set you are making as 1 and 0 this is the other test pattern, so two patterns are required to solve your problem.

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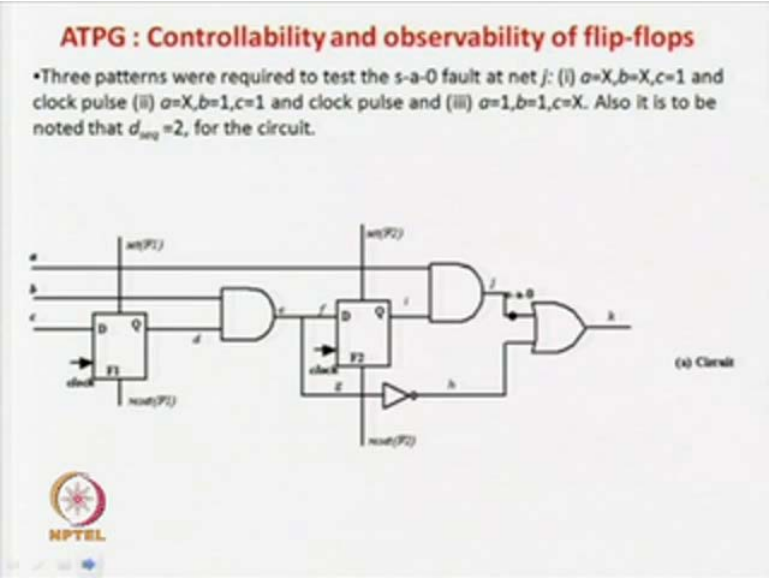

So, these actually says the number of patterns and also the test time, so what we have done by using the set and reset lines we have solved one problem. We have actually going towards combination, I will got to test sequential circuit, now instead of using this sequence plus one or another of this sequence number of test patterns to set the secondary inputs. Then, what we are doing then again we are coming back to applying this d i will got the final pattern to do it. Now, we are you controlling now instead of the order of the sequence of test patterns, what we are doing here.

Now, we directly controlling the flip flop outputs that are the secondary inputs, sorry the secondary outputs by rightly setting or resetting flip flop inputs reset or set likes of the flip flops. Now, you can directly give the pattern required to test the faults, so we have rustically change the order to 2 from the order d sequence plus 1 to order of 2 so this is the very he very great help and slowly we are going to a prime.

We are converting a sequential circuit to a vertical combination circuit for testing and applying combinational test pattern. I am solving the problem now that for a simple example last example, now we will go back do the big example which you have considered in last lecture. So, if you remember this was our circuit this was our fault and they were two flip flop, if you remember, so when we will done d, I will go on there, so we have found out that we require a 1 over here. Also, we require a 1 over here to test the faults because 0, so you require a 1 over here and also you require a 1 over here.

So, if we are applying 1, 1 here, so you will get a 0 over here, so the effect is d over here and this effect will be d over here. So, make a 1 you require a 1 over here, so this also one over here something like this and this was the scenario if you look by the last lecture you will understand. Now, the main issue was here that we are how can we in this this was the secondary input as well as this was actually another secondary input. So, because this is the output of the flip flop somehow how can we indirectly control this, so in this case in the last lecture we have seen.

We apply a 1 we applied a clock pulse when the value came over here after that we applied a 1 over here and this one was already there. We applied another clock pulse the one came here and again this for the same thing this one was retained. So, this one again has to be transferred over here, so all this we have discussed, but we require two patterns to set an this some to arrange to get a 1 and a 1 over here required to test patterns first it was a 1 over here c equal to 1 was here.

So, if you see c equal to 1 was required and a clock pulse then b equal to 1 and c equal to 1 we required so said this flip flop sorry this flip flop output and then finally, a equal to 1 and b equal to 1. We applied to test this fault, so three patterns were required to test the fault so d sequence of the circuit equals 2 that we have already seen. Now, let us see how can we reduce this by using set and reset line of flip flops, now you know that we require a 1 over here we require 1 over here.

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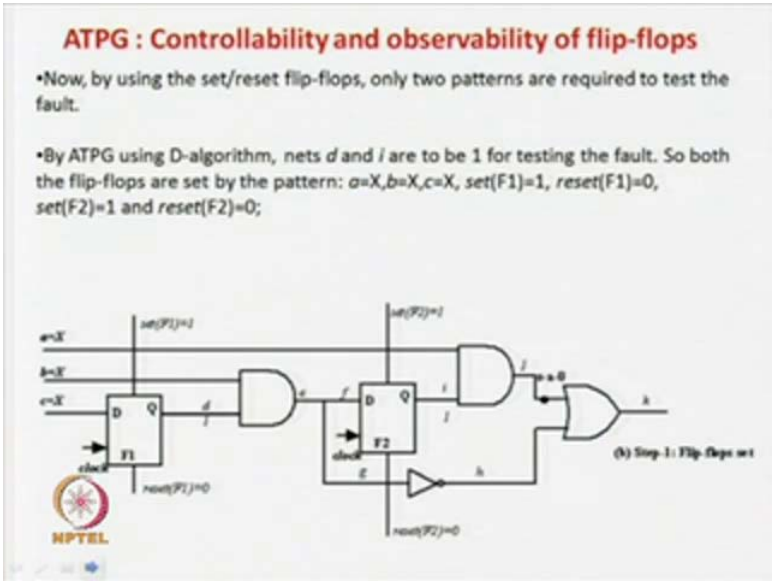

So, now instead of going for time frame and actually doing for a clock pulse what we will do we will make this one as 1 and this one as 0. So, immediately you do that, you get the output as 1 because it will set the flip flop for the same thing for the other flip flop. Also, you make set equal to 1 and you set equal to 0, immediately you get a 1, now your job is done, so you get a 1 over here and 1 over here.

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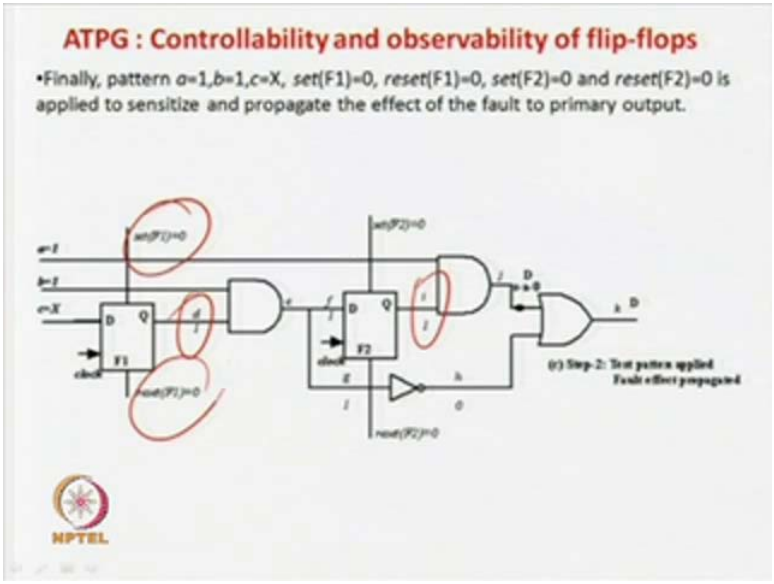

So, what we are doing only two patterns are requires doing this one pattern to set the flip flop and another pattern to test it. So, you make this and this, so this output and this one

are set, now what do you do, so you note you get a 1 and a 1 by resetting this. Now, we have to again go for the normal operations of the flip flop, so you make them 0 as 0. So, that is the normal operation is done, now you make z equal to 1 b equal to 1, so if you do that you will get a 1 over here and this will be a 0 over here.

So, this will be 0 this will be one is the 1 over here and a 1 over here for the AND gate, so you will get a 1 you will get a d as shown where a d has to get a 0 and your job is done. So, you require two test patterns, one is one is to set the flip flop this and this because the 2 a b x are not a b c are not important.

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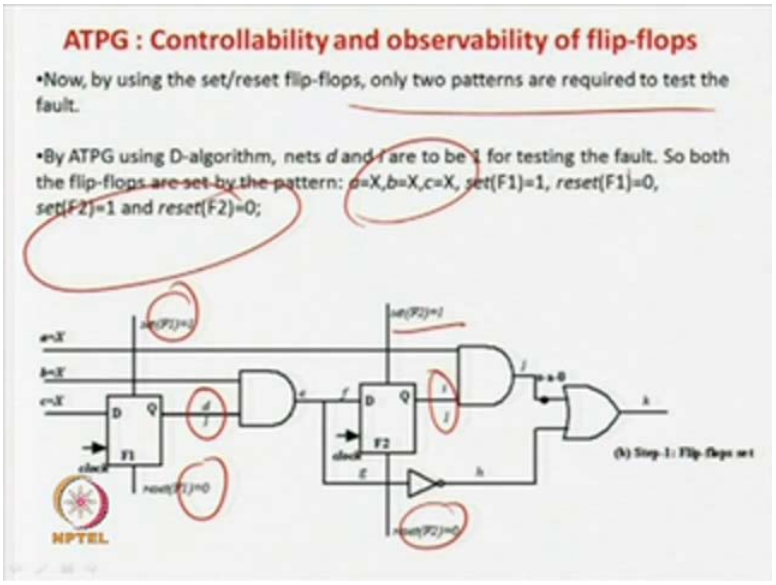

So, you said this to flip flops then in the next pattern, you go you just apply this patterns and your job is done. So, you have to remember that if you can have 10,000 flip flops, only two patterns are required to solve the problem.

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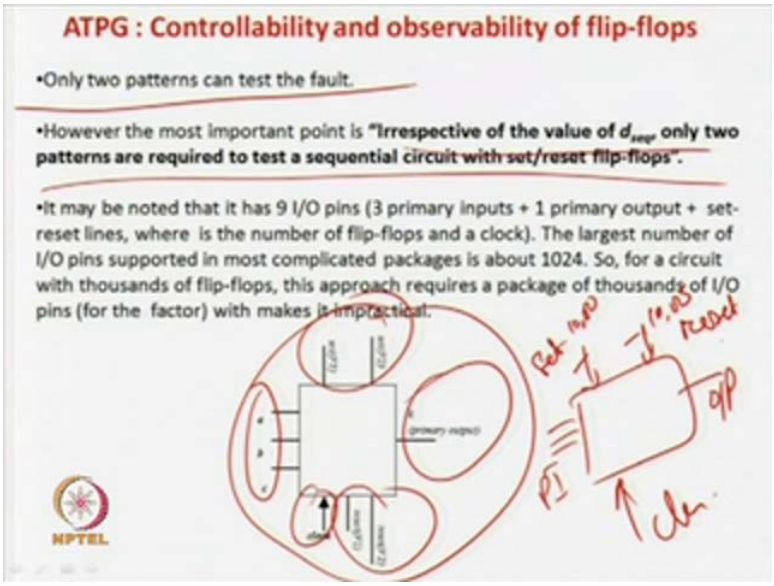

One pattern will be to set and reset the flip flops the other pattern will be for what the other pattern will be just if you can see even if you have another ten flip flops. If you just think about that if you have another ten set of flip flops, then also you did not worry why you need not worry because in case of time frame expansion method what was happening. If you have some something, let us again see back what we are doing, so if you have you have to observed that it is, so you can think that that is a small circuit, so all it to flip flop, so here we are required two patterns.

The idea was not that the idea is if it in your 10,000 flip flops, again two patterns are required to solve the problem say for example, you have some 10,000 flip flop some other stuff is there. So, if you are using time frame expansion method, then one pattern will be required to set this another pattern, it will be required to set this another pattern will be required to set. So, if you have 10,000 flip flops in sequence, so if you d sequence is equal to 10,000 and then you are in a big problem.

So, if you have a 10,000 flip flops in the sequence you require the 10,000 patterns to solve the problem set the primary outputs of the flip flop primary outputs of flip flops are nothing but they are your secondary inputs. So, you have to do that and then one pattern will be applied here to test the circuits, but know you see if you are having direct access to the set and reset lines. Then, what you can do one pattern if you want a 1 over here you make set equal to 1 reset set 0 if you set 0 over here make set equal to 0 and reset

equal to 1. Similarly, if you want again get 0 over here and reset equal to sorry set equal to 0 and reset equal to 1 and all these things.

You want to have you can apply; finally these are all the flips of individually control level that we have to assume. Then, your problem is solved, so two patterns are done for this one, no you see what you see and what you gain and what you lose, so gain is only two pattern two pattern to test the circuits. If as the number of flip flops are there what may be or may be the sequential depth and need not worry at all your job is done. Only two patterns are required for this one, but most important point is irrespective of the value of the sequence only two patterns are required to test the sequential circuits.

So, that is the greatest boon you are getting that you have converted a circuit from a sequential circuit your virtual combination circuit and you are solving your problem. So, d algorithm is doing everything for you need not go for time frame expansion all this, but if you look at those black diagram of the circuit. So, we are at just look at the block diagram so these are a b c with the primary inputs primary output is there and such at one to set lines for flip flops and to reset line put to then a clock if you think that I have 10,00 flip flop.

Then, what will be case this will be the primary inputs this is your output and this will be your clock and how many set lines will be there 10,000 set lines will be there for 10,000 flip flops and 10,000 resets lines will be there for the 10,000. These are the set lines and these are the reset lines, so know you can see the complexity, so 10,000 set lines and 10,000 reset lines are there to do your problem. You can understand that maximum number of output of a primary input output of a chip can be maximum 1024 or something like that 512.

They are very expensive to get a package like this where you can have 512 for 1024 inputs, now if you have 20,000 inputs such packages are not available and you cannot do a circuit like this. So, we have gone one step we have converted a circuit to a virtual combinational circuit and we have solve the problem and now the night may have again started that this set and reset lines are too many in number.

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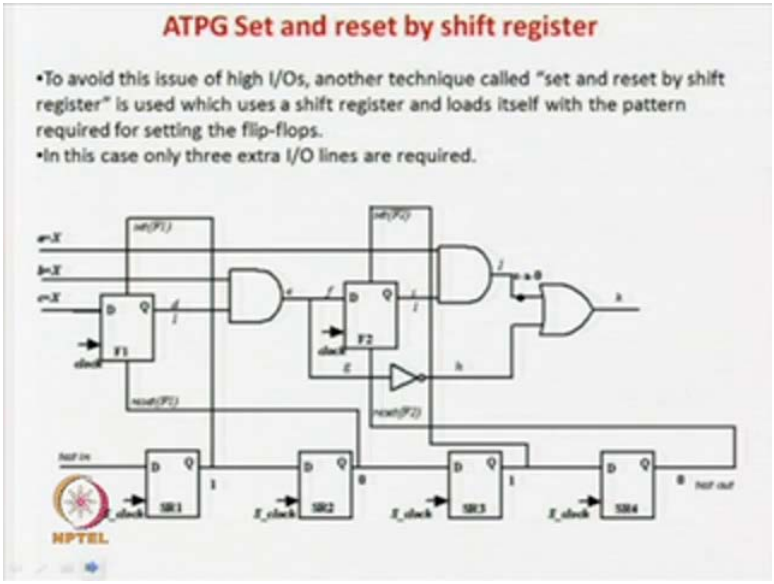

So, how can we do that then the engine is started to solving the problem, so we cannot have we will use the concept of having a set line or reset line we will control them, but how can we control them by bringing them. So, many pin outs, so bringing many pin outs is not fusible because you do not have package or packages means anything which you have seen in the second year classes. You have seen the digital of the black packages are there. This called the DIP, dual inline package, so their silver pins and all, so how many we have seen we have seen around 1024 or may be 30 or 40.

You might have seen for this, but 10,000 or 20,000 is almost impossible and it is not doable at all and also that is an also you require a net is so we have also this is verity in the very first lecture of this testing module. So, you have to require 10,000 plus or 20,000 of the 80 which is also a very expensive equipment and that the number of probes to give inputs to the 20,000 fees is also not fees able, so that idea is dropped.

So, now what we will have done they are saying at ATPG set and reset by shift register now the problem they have found out was you in the same example you are going to check. So, you required a 1 over here and you required a 1 over here that was the requirement, so for that you have to make set equal to 1 set equal to 0 set equal to 1 and set equal to 0 that was a requirement if you remember.

Now, what problem we had the problem is that if you want to bring this pin, four pins, so 10,000 probe means 20,000 pin out should be there. Then, how to do this so people have

say that we cannot have that many bring outs, so how can we solve some people give the idea that we use what is called a shift register base technique. Now, what are the shift register base techniques, so in this case the we just want to minimize the pin outs, so we will have a set of what you called another shade set of register. The set of flip flops which is in a connected in a what do you call a shift register kind of thing.

So, 1, 2, 3, 4, so there are four pin outs, so you have if there n flip flops, so you require 2 n number of scan what we can called shift register 2 n flops in shift register is the idea. So, 4, so here will be 4 or if there 8 flip flops, so there are in the 16 in this case so that will be that is the idea. Now, what you do so that is the problem you are having, now what they have done, they have saying that now instead of bringing this pin out, there will be connected this, so the output of each pin of a shift register.

So, you now see you have two flip flops so I will put a shift register of four flip flops, so if there are 5 or 4 flip flops in the names of the I will have 8. Now, the first output of the flip flops for this shift register will be connect to the set line the second flip flop of will be connected to the reset line. Similarly, the third output of the shift register will be connected to the set line of the second flip flops and last flip flop output will be connected to the input of the reset input this second flip flops. So, now what do you do, sorry now what you require the connection is done.

Now, you need a 1 over here, a 0 over here a 1 over here and a 0 over here, now what you have to do you can say that this you require a 1 at the output here 0 here, 1 here, 0 here because now this input a set and reset lines we are driving externally from anything. So, you are not driving by pins, so if you look at the last lecture last slide if you see so there were external pins there were external pins and you put apply them parallels. It is in one go you can apply all this flip flops in one go, but for that you can set and reset the flip flops, but for that what do you require you require there are the circuit or this chip design or the chip packaging plus 20,000 input output like this.

So, that is, sorry input like 20,000 that is extremely difficult problem, but in one go you could have control all the flip flops outputs directly in one parallel. Now, in this case you require 1, 0, 1, 0, now you know that in shift registered in one go you cannot have one 0, 1, 0 you cannot have directly in shot you cannot having. So, what you have to do you

have to apply 1, then apply a clock pulse then 0, then apply let us see how it will happen, so you required four iterations to do this.

So, first you apply a 0 over here, so this is the requirement, so do not go about this this is the requirement you can think. So, you will requiring the end, so first you apply a 0 give a clock pulse, so the 0 will come over here. Now, you apply a 1 over here a 1 over here now you apply a 1 over here you apply 1 over here and your premium, but then all these clocks are same and this clocks are different. These are the important to know this is circuit clock and this is the shift register clock two clocks are now coming into picture, now you give a 0, now you give a 1 another clock pulse you have to all this.

So, now this 0 will be coming over here, so will give the 0 over here and this one will be here, now you get a 1 over here and a 0 over here these are all actually do not cares now you do not know what is gave you they not credit. Now, you give another 0 over here and give a clock pulse, sorry you give another clock pulse over here, now if you give a clock pulse what is going to happen the 0 will be here. So, this will be a 0 over here and this one come over here this 1 come over here and this 0 will go over here, so this will be the case.

Now, in the n you apply a 1 here and give a clock pulse, so once you do that, so this zero will come here this one will be coming here this 0 will be coming over here and this one will be coming over here.

Now, you have one zero one zero which was require so you require 0 clock pulse 1 clock pulse zero clock pulse 1 clock pulse. So, four clock pulses are required in this case to shift your value require to control n to control the input and the set and reset improve the three clocks. Now, you can say that so if you have say 10,000 flip flops, now what is the case you require 20,000 clock pulses to control this flip flops the answer is correct let me have to do and also you have seen that you are a t a time is very expensive. You cannot have a, you take this type of 20,000 input times you cannot have or it is very restrictive to do it, but now this problem.

They have found out that this problem still remains if you look at a sequential circuit tested this problem people have not be near to solve as of now to minimize the test the this number of clock patterns to take the part. Somehow they are using fault collapsing because you have already seen that fault collapsing algorithm.

So, minimize the number of faults only those things, they will be doing minimize the number of faults, but this shift filling of the shift register will see this scan chain the modulate person of this. That will be seeing in the next, but any way 20,000 of pattern or whatever to said this flips to set and reset lines indirectly or means what we called in an implicit manner cannot be there.

So, this number of test pattern clock periods will be required shift the pattern here which can indirectly directly get access to set and reset line and control the output of the flip flops, but here is the problem here a 1 advantage, did you solving the problem. So, this is the clock for the circuit and this is the clock for this this s clock is the clock for this shift register. Now, this two clocks are keep different, now why it is the idea here is that if you look at these clock pulse, so this clock pulse so this clock pulse is arriving on a drive gate and this again the output is driving another what you call inverter then another data.

So, whenever you get the data whenever this clock pulse comes, the data comes over here so they application of the clock pulse with data will come here say it will take some time for the propagate take over here. So, you cannot have a very fast clock over this period because whenever you apply the clock pulse your data will come here then to get the data here. We can assume that the another flip flop over here to then this data this data the change in data should be arriving over here, then only you can use another clock to figure this flip flop use the q.

So, this is the long path, so this output is there end gate is there then inverter is there then the OR gate is there, then the date will come, so there were some dealing of the data traveling from here to another flip flop input. So, this clock period has a limitation in speed you cannot go for a very high speed clock over here say of this is the slow clock, but if you have this is the safe register. So, this output is connected here, this output is connected input and so far there is no gates here no gate here and no gate here directly you can fill it, so there is no dealing.

So, once you have by the clock the clock comes and there is the data comes and immediately data gave transfer to this input of the data because had they are been a lot of combinational cloud over here. Then, you would have to wait from this data to becoming from here to here then only you can apply another clock pulse. Now, this is not the case

here the output is directly connected from this to this the output is directly connected from this to this.

So, your problem is solved so you can apply a very first clock over here compare to this clock so that you this fill up this filling up can be done in a very fast gate. So, even you have to say for 10,000 s flip flops even you have to have 20,000 patterns to set a reset this lines, but then again your problem is not high. If it is say 10 megahertz clock, so you can use it at 500 megahertz clock or something like that.

So, usually you can also use a gigahertz clock over here and very quickly shift the data, but this will be slow because there lot of combinational dealing in this case. So, the number of test patterns if in case of in this case the number of test pattern were two because in one pattern you set and reset all the flip flops in one go.

Then, we apply the pattern in done it, but in this case the set reset lines have to be filled up in a sequential manner, so number of test pattern required you can see is that 0, 1, 0 clock 1 clock 0 clock 0 0 clock 1 clock that will take around 20,000 cycles if the 10,000 flip flops. That can be done in a very fast rate that can be done in a very fast rate this way and one more point you have to remember over is that.

So, you can ask may be that, so 20,000 clocks periods I mean sorry 20,000 patterns are required 20,000 or a 12 number of the flip flop patterns clock periods are required to shift the data here. So, you can say that if there are n flip flops then 2 n patterns are required to do this to control this set and reset and tools.

So, you can also say that the time frame expansion method also you are also one more saving the same things. So, if there is a de sequence number of flip flops then what you have to do you have to apply in time frame one you said some of the flip flop in time frame to use the some flip flop in the de sequence time frame after de sequence time frame. All the flip flops are said, then you have applied this and you know that this sequence of the number if there are m flip flops. So, here 2 n patterns I mean 2 n series are required, but in case of time frame expansion method only d sequence number of a pattern said required.

You know that the de sequence is del d sequence is sorry the value de sequence will be less than de sequence to n why because if the all the flip flows are tide out in one chain

like in this case 1, 2, 3, 4 all the flip flops are tied out in one chain. So, here this sequence will be 4, but if sometimes it may happen that there are many of the flip flops are in parallel that is not all the flip flops are dependent on the previous one. So, all your de sequence is the maximum depth of the flip flop that may be equal to or less than so you can say that these you call these time frame expansion methods in its time frame.

You control some of the flip flop output, so it may not be two ways, two way means actually double the number of flip flops. So, which is required in case of shift register base testing using same to same then still why you are going for this one why you are not going. I mean this one you can call sequential time frame expansion the answer to give this sequential time frame expansion method is a very complex term, so what may happen is that in one time frame say d minus de sequence you set some of the flip flops.

Then, in time frame this sequence minus 1 plus one you use some of the flip flop, but you are not using this set and reset lines to do that. So, what you are going how you are setting up or d setting the flip flops in case of this say means time frame expansion method we are using the primary inputs only to do that. So, primary input means you have to get axis with flip flops you have to cove some of the combinational circuit like for example, you are seeing that. So, this is flip flop which just have to be control and there is a lot of combinational circuit over here, so you have to control these inputs in time frames approach to get an axis to this one.

If you remember this example like in this example you say that by using the time frame expansion method you cannot trace the circuit because using the primary input output. You cannot control the primary output, but by this d resistor I mean was you set reset line you can directly have this control this. You can test it in other words this this method that is direct axes to the set and reset lines of the flip flop sequence using, so what advantage you are gaining is there is no question of any inconsistency always you can control the flip flops.

So, even you are applying two n number of patterns to set reset and reset lines, but you are never going to have an any inconsistency, so just to apply d algorithm get the test pattern control the virtual primary inputs by the set and reset lines apply the test pattern. You are done, so it is very simply that incase of time frame expansion method you require d sequence number of patterns which is less than 2 n, but at say it is very

complex in nature. That is you may have what is the case that you may land up to a big problem.

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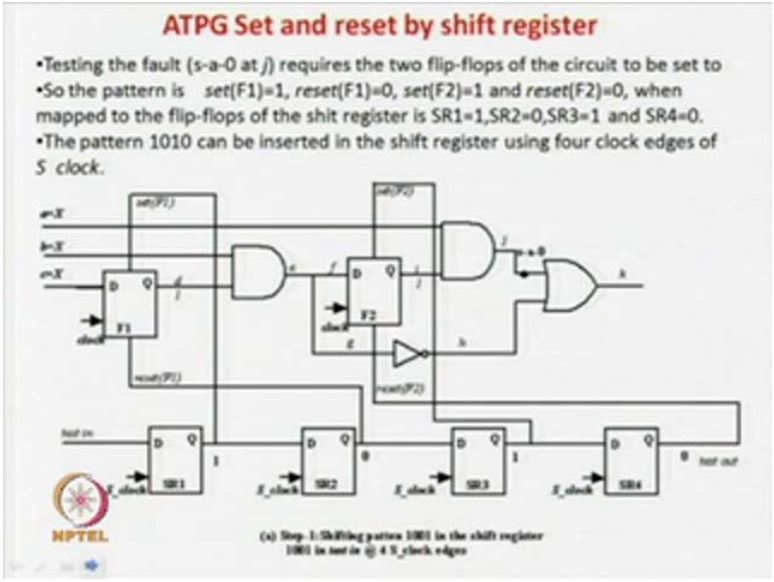

In the last time frame before the circuit you get the inconsistency and again you have to re do so that of line complexity is so high. That may be left slowly moving towards this what you call this time frame expansion method that slowly forgetting and there going for this set reset line sequence. So, you can see that this is what I was discussing, then how can you trace the circuit, so this people have say 1, 0, 1, 0, they have done and they are apply the pattern like 1, 0, 1,0 in four clock edges.

We have done this one so this is how you do the testing that means four clock pulses you sated and you then you apply this 1, 1, so in four stages one, sorry there is a let us have a look at in the steps. So, how you do that so this is the circuit, so you require 1 over here and a 1 over here so you require four clock pulses you shift 1, 0, 1, 0. So, it is 1, 0, 1, 0, you shift it and then you sorry all set are done those how we are apply 2 n number of patterns to do that into two n clock obviously this clock this clock would be much faster than this clock. Now, what you have to do another problem over here not only 2 n, so more complexity we are adding.

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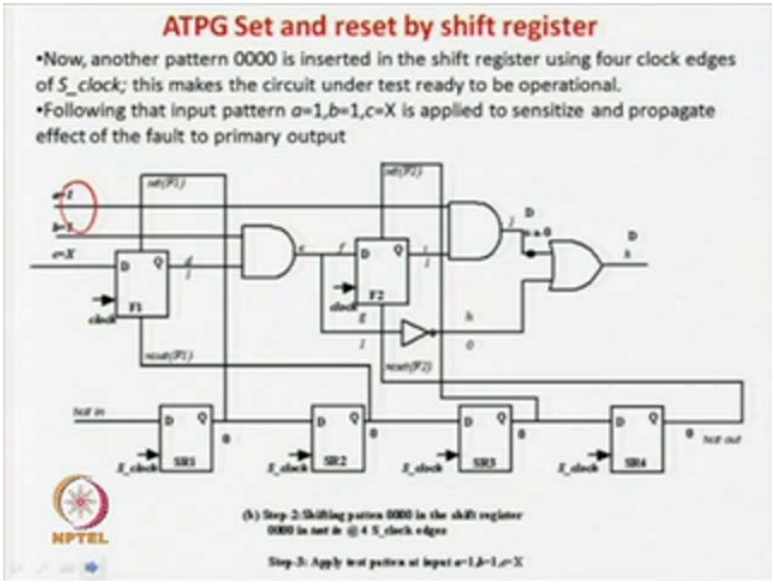

So, now all this lines has to be 0 because now you want to operate this circuit normally if you want to apply and get this d over here. So, again this four you have to apply by 4 clock pulses, so not only 2 n, so 2 n plus 2 n number of clock periods are required to set this flip flop or reset this flip flops are required. Then, again you have to make everything 0 set 2 set 0, so there is circuit becomes normal and then you can apply the pattern to do this clock. So, huge number of extra number of test patterns are require to control the shift resistor to do this set reset controlling and that actually.

So, this design was also not very popular and then actually the what do you can call the main design achievement of testing which is call the most important. If you see that what is the most important design in case of testing I will say it is the scan chain. So, then this scan chain came into picture which actually solve this problem forever, so here will be the partially solve the problem that there is only two pins testing and test out there is one separate clock that is only three extra pins were require.

Now, you require two n plus two n number of clock periods extra to set and we said this shift resistor which are controlling the set and reset lines to get axes, but now but this actually is also taking if there are ten 10,000 flip flops. So, you are having 10,000 or 2 if there is it will n we are saying if there n flip flop then two n number of extra flip flops. We have to add and 2 n plus 2 n extra clock periods are required to control this to do this, so that is a big problem which is give into picture.

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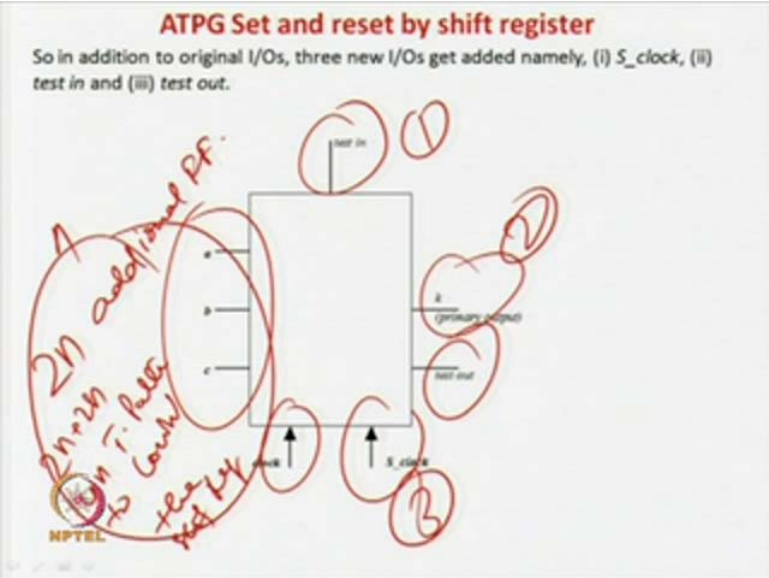

Then, this is our diagram as I said, so a b c are the inputs this is the testing and this is the test out to extra that the shift resistor input shift resistor output primary output and two clock. So, additional pin is 1, 2 and 3, so 3 in 3 additional pins you can do this, but if there n flip flop 2 n additional flip flops you add additional flip flop. You require as well as 2 n plus 2 n, it will give four n test pattern to control this shift resistor, so this is the penalty, we have to apply and actually this was solved by a person.

Then, what will be case this will be the primary inputs this is your output and this will be your clock and how many set lines will be there 10,000 set lines will be there for 10,000 flip flops and 10,000 resets lines will be there for the 10,000. These are the set lines and these are the reset lines, so know you can see the complexity, so 10,000 set lines and 10,000 reset lines are there to do your problem. You can understand that maximum number of output of a primary input output of a chip can be maximum 1024 or something like that 512.

They are very expensive to get a package like this where you can have 512 for 1024 inputs, now if you have 20,000 inputs such packages are not available and you cannot do a circuit like this. So, we have gone one step we have converted a circuit to a virtual combinational circuit and we have solve the problem and now the night may have again started that this set and reset lines are too many in number.

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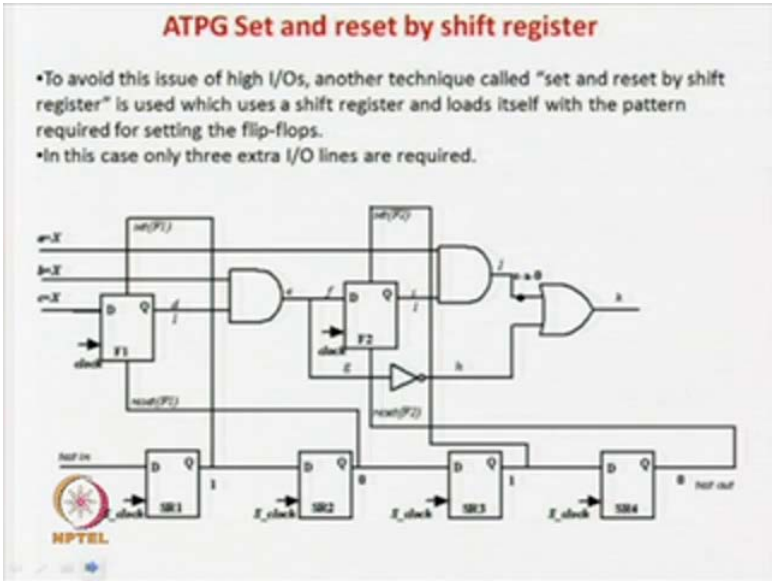

So, how can we do that then the engine is started to solving the problem, so we cannot have we will use the concept of having a set line or reset line we will control them, but how can we control them by bringing them. So, many pin outs, so bringing many pin outs is not fusible because you do not have package or packages means anything which you have seen in the second year classes. You have seen the digital of the black packages are there. This called the DIP, dual inline package, so their silver pins and all, so how many we have seen we have seen around 1024 or may be 30 or 40.

You might have seen for this, but 10,000 or 20,000 is almost impossible and it is not doable at all and also that is an also you require a net is so we have also this is verity in the very first lecture of this testing module. So, you have to require 10,000 plus or 20,000 of the 80 which is also a very expensive equipment and that the number of probes to give inputs to the 20,000 fees is also not fees able, so that idea is dropped.

So, now what we will have done they are saying at ATPG set and reset by shift register now the problem they have found out was you in the same example you are going to check. So, you required a 1 over here and you required a 1 over here that was the requirement, so for that you have to make set equal to 1 set equal to 0 set equal to 1 and set equal to 0 that was a requirement if you remember.

Now, what problem we had the problem is that if you want to bring this pin, four pins, so 10,000 probe means 20,000 pin out should be there. Then, how to do this so people have

say that we cannot have that many bring outs, so how can we solve some people give the idea that we use what is called a shift register base technique. Now, what is the shift register base technique, so in this case the we just want to minimize the pin outs, so we will have a set of what you called another shade set of register. The set of flip flops which is in a connected in a what do you call a shift register kind of thing.

So, 1, 2, 3, 4, so there are four pin outs, so you have if there n flip flops, so you require 2 n number of scan what we can called shift register 2 n flops in shift register is the idea. So, 4, so here will be 4 or if there 8 flip flops, so there are in the 16 in this case, so that will be that is the idea. Now, what you do so that is the problem you are having, now what they have done, they have saying that now instead of bringing this pin out, there will be connected this, so the output of each pin of a shift register.

So, you now see you have two flip flops so I will put a shift register of four flip flops, so if there are 5 or 4 flip flops in the names of the I will have 8. Now, the first output of the flip flops for this shift register will be connect to the set line the second flip flop of will be connected to the reset line. Similarly, the third output of the shift register will be connected to the set line of the second flip flops and last flip flop output will be connected to the input of the reset input this second flip flops. So, now what do you do, sorry now what you require the connection is done.

Now, you need a 1 over here, a 0 over here a 1 over here and a 0 over here, now what you have to do you can say that this you require a 1 at the output here 0 here, 1 here, 0 here because now this input a set and reset lines we are driving externally from anything. So, you are not driving by pins, so if you look at the last lecture last slide if you see, so there were external pins there were external pins and you put apply them parallels. It is in one go you can apply all this flip flops in one go, but for that you can set and reset the flip flops, but for that what do you require you require there are the circuit or this chip design or the chip packaging plus 20,000 input output like this.

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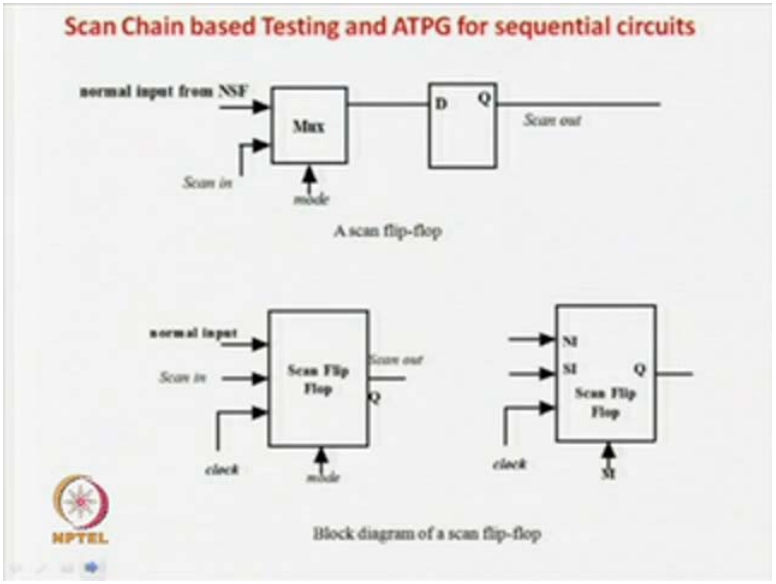

In the circuit, but if I make it the mode one then I will take control of this step. So, let us see how it is done, so this the additional thing I was talking about, so this is your flip flop in before that has input 1 multiplexer. So, this is his control for the first flip flop a normal output of this one and this is be mode, so this is a actually we can call this this block diagram of a scan flip flop.

Now, what is flip flop of a scan flip flops here will have normal inputs scanning that is a special input this is a scan out clock and mode. So, if your mode is equal to 0 the normal input will be flowing in if you have mode equal to 1 then this scanning will be feeding in and that are the two cases. So, this is over scan chain normal inputs scan input clock and the output output is common, this is the block diagram of this one now you see what that has done.

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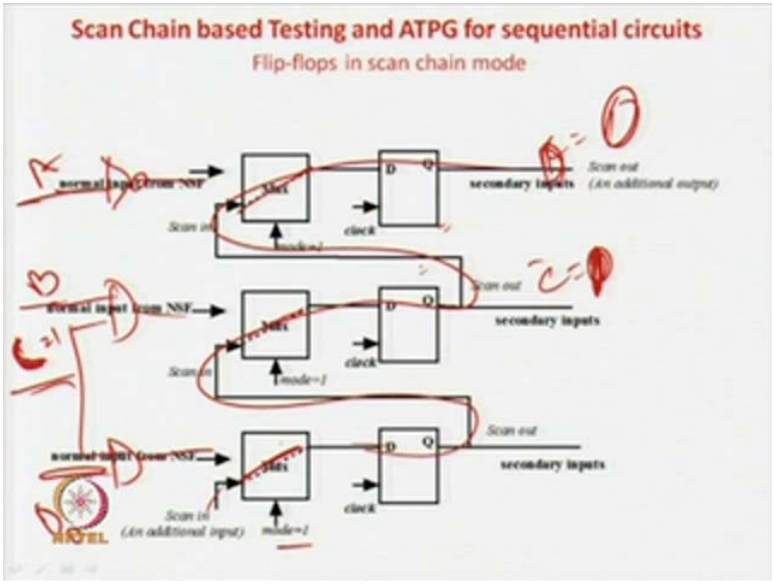

So, now you said that I want to take control of the whole flip flop as I told you, so you may have some inputs like this, so an inverter if you remember, so this one was over inverter. So, there was some and gates over here there are some also and gates over here this was a short this was c this is from here. Now, he says that for some testing you assumed that a for some testing also you assumed that this c as to be a 1 this one as to be a 1 for some fault you required that this as to be a 1 that is this output because this c is that over here. So, you required this to be a 1, so for a some reason you want that and other things this input a, this input b, this is c and this is d.

So, you can call that this d is also connected to this one as this one same case have and you said that you required this to be a 0 for some fault testing because assume that is some fault testing. So, how you will do, so what you require in this scan chain. So, what do you require in the flip flop this output you do not require see you required to be one because this is a virtual primary input or secondary input thus as to be made one.

So, you require controllability of this and this also you want make it to be a 0 because this is connected to this pin which is to be 0. So, how to do that, so if you look at the old story that is control reset, so what we have to do we have to make this a set equal to 0 reset equal to 1 reset equal to 1. So, this will be 0 this is 1, so set will be one reset will be 0 and here it is do not care do not care about this. So, once it is done, so you will get 0 1 and required that you have to make set equal to 0 reset equal to 0 is equal to 0, this is 0.

Then, the circuit will be normal mode and you can do that so for but, for that if you see that if the 6 a flops, so what do you require. So, six flops you require either a three flip flops, so either you would require six pin outs. So, you require either one, two, three, four, five, six extra pin outs a six extra pin outs you require or whether what do you know or whether we have to use a ship register. So, which will having six flip flop and that line makes your life very health because either extra number of thing say now or extra number of what do you can call a flip flop, sorry so what this person as done he has put some extra multiplexer.

Now, we are seeing that already this three flip flop are there in my circuit then why do you want to additionally incorporate another flip flop chain to do that. So, you said that when you are when you have to get the value of one over here and a 0 over here that was required. So, a d over here, so you was to do that, so how why you should use another extra chain. So, he said that I will make my mode equal to 1, so when mode equal to 1. So, this input get connected here these output get connected to here because this normal output from the in output from the eraser block is now cut because a all the modes are one.

These are flip flop, so this is connected to this one, now you see automatically a chain has been developed using this is very important to observe that a chain has been developed not by using any extra flip flops. Again, I repeat not by using the any extra flip flops it has been obtained by using the flip flop which are already develop already was there in the circuit were addition additionally adding some extra marks. That is the only thing is added, now you make mode equal to 1, so you get the chain connected now what you have to apply.

So, you have to apply a 0, a 1 x and you have to apply, so that why I told you that has not been yet solved all that part is not yet solved in the very in matured way that how can you mean reduce the number of the clock be rates to do the testing. So, in this case three flip flops would be control, so you apply 0 1 x and you apply three clock pulses. So, initially this 0 will be a x, will be here this will be x will be here x will be here, then you apply a 1.

So, you will get one over here x and x over here x and x over here then we apply another clock pulse kind of a thing, so get the chain set. So, chain can be easily said over you see

some patterns so that will again see some examples, but in three clock pulses said it, now what you do. So, it is 1 this is, sorry this is 0 this is one and this is x you required, now what do you do, now again you know that some inverters is there some and gate is there something like this.

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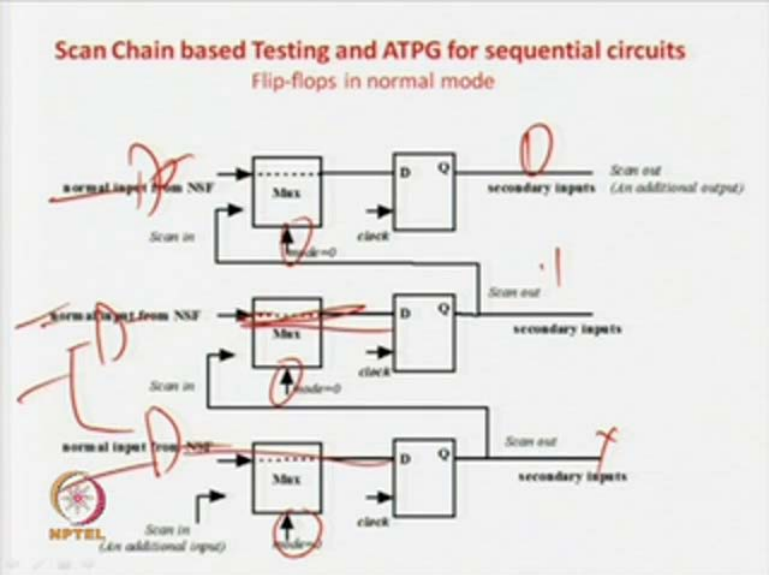

Now, you want to test your circuit we are applying some patterns. So, now what you have to do now again you have to become this chain and make this circuit in the normal mode that is set result board as to be made. So, what you can do you just make this mode is equal to 0, so once if mode is equal to 0 will be there in normal circuit input will be going to the, sorry going to the output something input something flip flops. So, make mode equal to 1 and normal connection is there flip flop you can give it, so here what we have achieved.

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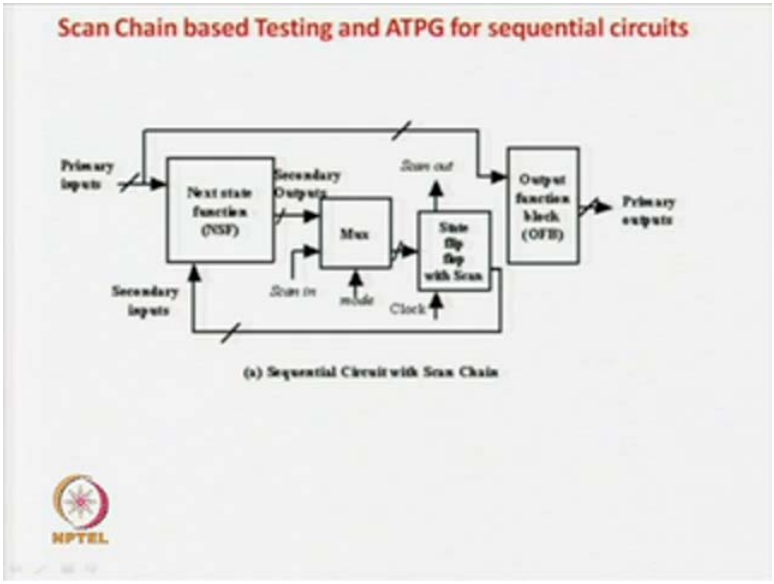

So, this actually the diagram will see what is there, so this is what is required. So, you can see that this is the secondary in outputs this is the secondary inputs this we have to actually controlled. So, what this person as done, so he has done mode equal to 0 if mode equal to 0 the secondary inputs are directly coming to the circuit.

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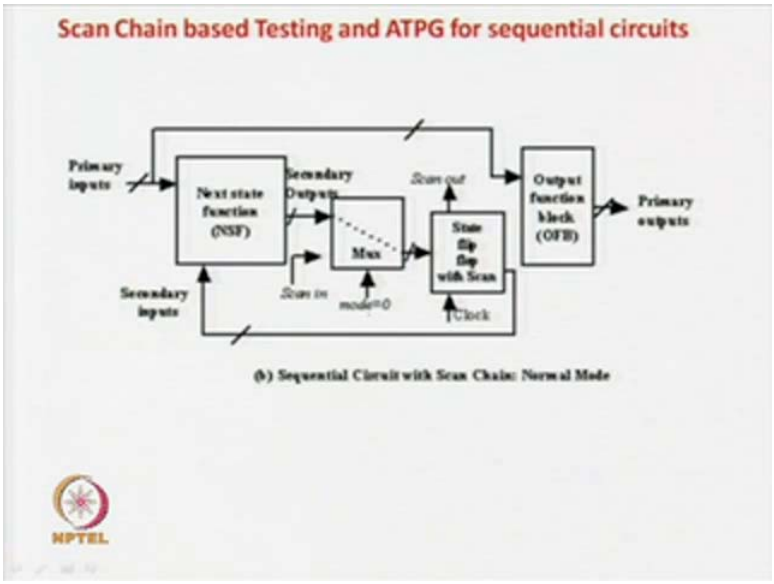

We in this case there is nothing controlling when the circuits are operating normally, now in c what you are doing? So, in this case you are making mode you make as 1 and then what happens you can get directly control of this flip flops you can control.

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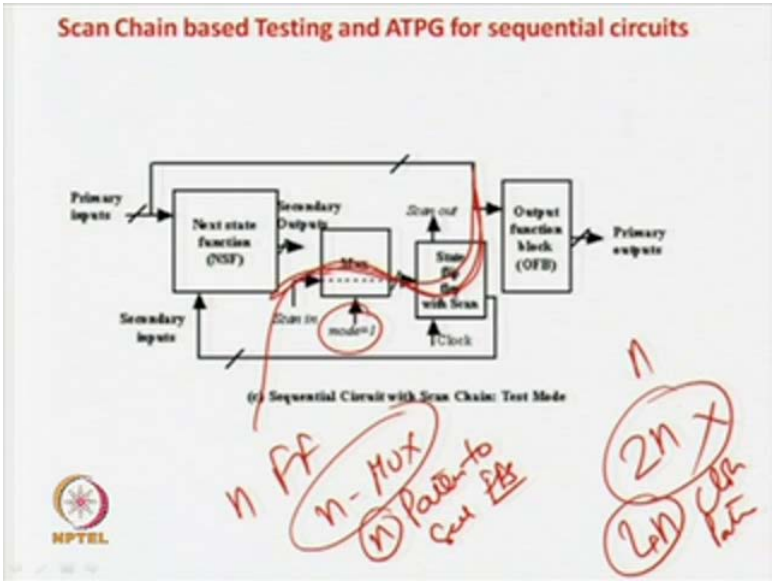

The set whatever value you require you one and then to come back and make mode equal to 0 then this sanction will be decouple there will be no change normal circuit will be there, you can apply your test pattern and to the test state. So, this was over lecture about the scan chain, so next lecture will give some elaborate example say how what is the advantage and what is the disadvantage? But before closing, I will just see one thing that what is the gain we have achieved, so gain we have achieved.

Now, it if there are n flip flops in the circuits we do not require 2 n number of flip flops we do not require 4 n number of clocks and patterns. So, what we require if there are n flip flops we require n mux and it is already two is to one mux with size or it area is much mux less than the number of our flop. So, you just require n flip flops, n mux is equal and you require n patterns to set the flip flops, so in last case you require 4 n. Now, we require only n and instead of 2 n extra flip flops you require just n number of mux. So, we have reached we have reduce the problem a great deal and that actually became the path opening for testing of sequential circuits.

So, if you say what is the best design which is possible has been reporting incase of sequential circuit from my opinion I will be saying is this scan chain. So, now just solve the rod of important problem it as solved like time from expansion collisions or inconsistency it as solved secondly what it has solved. Secondly, it has solved about your

you do not require 8 of flip flops just you require n mux with multiplexer 2 is to 1 with sizes must revolt then flip flop.

Second, you do not require 4 n number of clock period to set or reset you just require n number of patterns to set or reset the flip flops and also you have to observe one thing that here flip flops do not require a set, and a reset line is not required over here we are doing it in the normal way. So, one of the flip flops size can also be smaller, then the set or reset flip flops. So, that you can a you can incorporate this one in size that you can say that if ever flip flop set and reset signals then it area will be larger than the circuit.

Then, a flip flop which does not have a set in the set line then you can think that the mux area you can say that flip flop with line is almost equivalent, so flip flop with the mux. So, infect this a additional mux is not at all a problem, so additional mux we are adding that n mux area we are also saving by not using any kind of a set reset flip flop. So, that is again another great boon we are getting correct and only thing it that n number of pattern will be required to do this. That is only problem that remains and cannot be solved as of now we are just seeing and one more thing is that in case of scan chain.

So, this same flip flop you can see and the same clock is there, but this now the clock is operating in to different mode, that you have to know this circuit complex concept because when the circuit is operating in the normal mode that is in this mode if you can see the circuit is operating in the normal mode. So, if these is the normal mode is there then the output of this flip flop is go to this combinational lot of combinational clouds will be there. Again, you can get the output the outputs, so this is a delay, but so your clock as to be bit low arrange this case, but when you are doing working as scan mode then what is happening this output this is your chain this output is no longer there.

So, your flip flops are only in this mode so there is no combinational delay, so you can use this clock in a very fast rate. So, when you are scanning in the data to set the values in the flip flop you can do it very fast rate because there is combinational delay that much, but when you are in the operating the circuit in normal mode. So, you have to do it in bits lower rate so that this is combinational delay are matched. So, almost all the problems are being solved by this scan chain only one problem that remained is that n number if there n number of flip flops in the wrist case n number of patterns are require or n numbers of bits 0 as 1.

So, require to control the flip flops to 0 and 1, so that is only the problem that remains to be solved. So, in the next lecture on this, what we are going to see we are going to see how we can handle this n clock period business. How can you reduces this is one more and second we can see that what are the other variations or other advantages we get in scan chain with that we close for the day.

Thank you.