Design Verification and Test of Digital VLSI Circuits

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Module - 7
Lecture - 2
Functional and Structural Testing

Welcome to lecture 2 on Functional and Structural Testing, in the last lecture introduction to digital testing of VLSI. So, what we have seen is that in case of circuits testing (( )) occupies an important paradiagm, because in case of circuits, the technology being adapted is so new and it is currently changing in such a rapid way that most of the chips or you can say a high percentage of the chips may have failures or defects, that is the yield is sometimes as close is as close as 50 to 60 percent.

That is why we have to find out that which of the chips are functionally correct and which of the chips have fault and then we have to bill them appropriately and then we have separate, we have to separate that before we send them to the market. So, that is why testing in circuits is such an important domain, that we have already seen in the last lecture.

Then we have seen that function I am sorry testing of circuits or any system; maybe in the last lecture we have taken the example of a NAND gate, so we have seen that testing can be as simple as just checking the functional properties like for 2 input in NAND gate, it was offer all inputs like 0 0 0 1 1 0 and 1 1 and we just checked whether it is functionally proper. Then it can be as exhaustive or as complex as finding out whether the layout from which the chip is or the NAND gate has been designed is proper like the metal deposition should be proper the thickness between two nets, which is being laid out for the NAND gate has to be proper distance of say some x micron, which is as per the designed rule checks and so forth. Then there can be delay for then there can be so called the tungsten element fades and test, so we have seen that starting from the simple functional testing of the trough cable.

It can be as complex as checking the layout, but now the problem is that as we have to test millions of circuits for a sample ran and the number of gates in the trans in the circuits can be as large as millions. So, to test a circuit in full depth that is may be to the

layout level or at the transistor level it may take decades or years, so that is why we cannot go to that level of exhaustive testing.

So, at best what is feasible because our idea is that as we discussed in the last class our motivation was that, we have to apply as minimum test patterns as possible, that is as low test time as possible, but at the same time we have to have a very good what you call confidence or the or you can say that the accuracy of the test.

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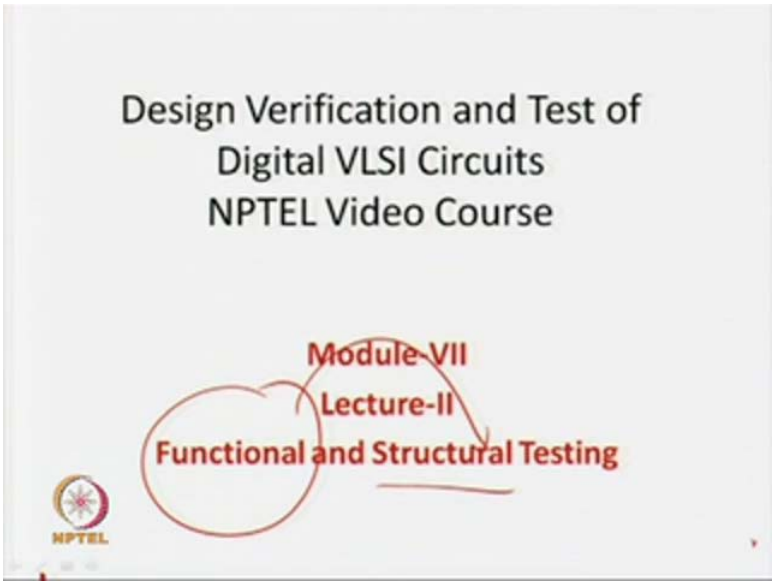

So, that is why today we will see what is actually called structural testing and why we have to move away from functional testing to structural testing, that is the main, main motivation of today's lecture. That functional testing that is in terms of the truth table that is of was the simplest testing in the last class, after that there was transistor level testing, there was delay testing and so forth.

And even we will see today that functional testing that is simple the truth table testing that also takes a very long time, and is not feasible to apply in a real circuit where the number of samples are in lenience, so that we have to move to structural testing, so that is what will be our focus today.

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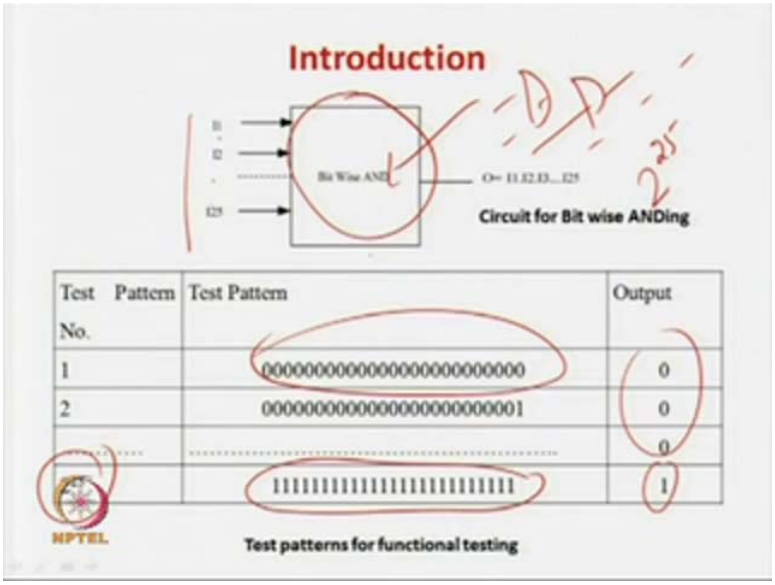

So, let us start with an example, so you can see that this is a 25 input NAND gates, AND gate circuit, so it actually it is a dot product of all 10 25 inputs i 1 to i 25 and inside this you can have a series of what do you call NAND, AND gate logic I mean logic circuit. This is not shown because it is quite large circuit, so we can understand that if I have to do functional testing for this one also we have to apply patterns, which starts from all 0's, that is i 1 to i 25 all 0's, and we have to move for all 1's.

So, we require 2 to the power 25 testing patterns to test the circuit we start from all 0's and end with all 1's, and what is the expected output for except in the last thing is it is and for all the inputs and it is i 1 dot i 2 dot, dot, dot i 25. So, for all cases the answer should be 0 except in the last case the answer is 1, so for exhaustive testing you require the applied order of 2 to the power 25 input patterns, which is very, very large. If you think that if I can even apply a test pattern in the nano second range, but if the number of this circuit is in lenience you will take days to do the testing.

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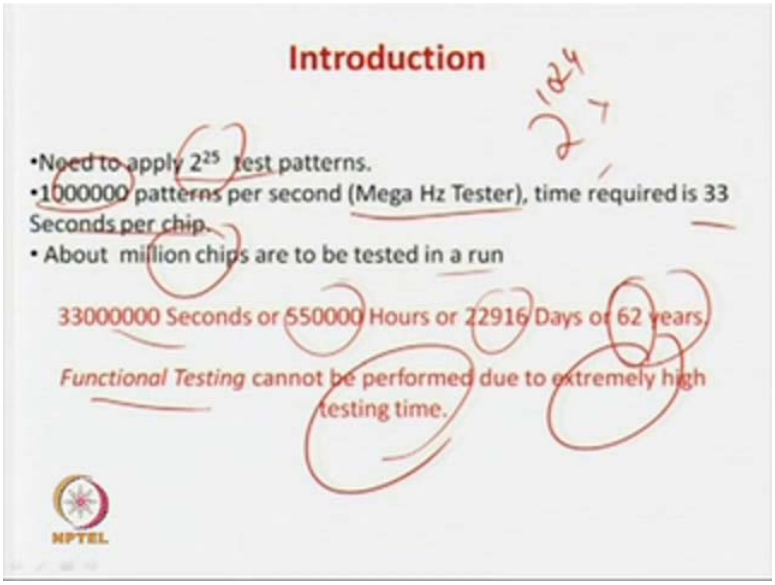

So, it is not actually feasible, so we will progress and we will understand more into this 1, so you can see we require to apply 2 to the power 25 test patterns for test default and we remember that we are not doing a delay testing in this case. If we have to done a delay testing in this case, then we have to apply this pattern followed by this pattern, then we have to apply this pattern followed by this pattern, so you can understand that we have to apply a more than double the 2 to the power 25 kind of efforts, because in all in 2 to the power 25, we just do a functional test.

Now, if we have to do a delay test that is delay test is one is the rise delay and one is the fall delay, which we have seen in the last class. So, for rise delay we have to apply this pattern followed by this pattern, then this pattern followed by this pattern and so on, till this pattern and this pattern. Then if we want to go for this sorry the fall test that is from 1 to 0, if this pattern has to be tested at speed then you have to first apply this pattern followed by this pattern then again this pattern followed by this pattern and so on.

So, you can easily find out how complicate the testing will become even for a simple circuit which is having which does the end of 25 units. So, that is why it this is not at all possible, so even if we the if normal functional test with 25 inputs no consideration for delay at all, you require 25 test patterns for delay it becomes more complex. And if you assume that we have a megahertz tester that is it applies, so many test patterns in a

second we require 33 seconds per chip to test the circuit and remember it is only simple functional test and in generally we have about one million chips per run.

That is once we go for fabrication we do not develop or I mean fabricate one or two chips in a single run we have around millions of circuits, so millions of chips have to be tested in a run. So, we can find out if you do the calculation you will require this many seconds or this many hours, this many days or some huge number of years to do the functional testing for a simple circuit having 25 inputs. So, for functional testing cannot be performed due to extremely large number of testing, that is what is the idea, now you can think about this is only a circuit having 25 inputs and the rate circuit is as simple as 25 doing a ending of 25 inputs.

Now, you can think of a circuit like a Pentium chip which is in our processor or you can think of a graphical processor circuit, which can have 500 towards the inputs or longer than 24 inputs then the number of inputs required will be 1024. And then you can understand instead of this 62 years, it can be 62 decades or it can even be something which our testing will start in our lifetime and will be not alive to see what is the output. I mean may not be feasible in our lifetime, so we can understand that it is practically impossible to apply functional testing.

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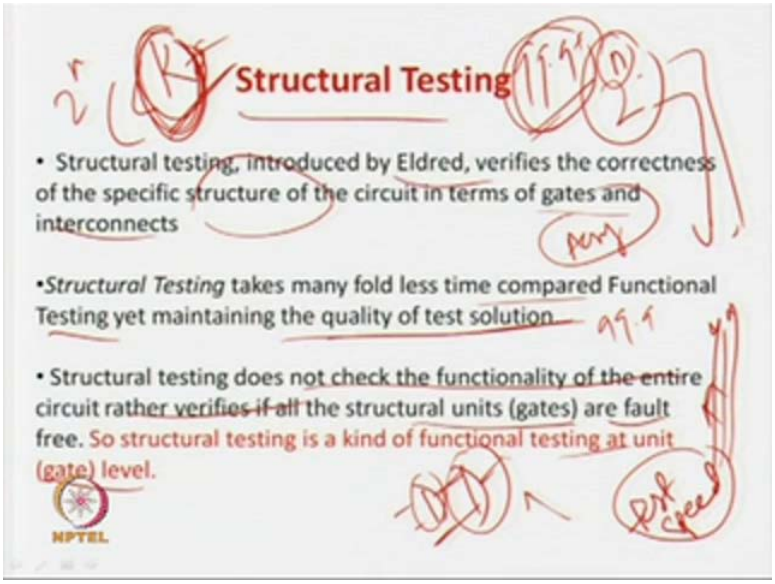

Now, you see, so what is the solution, the solution is that we have to bring down this number that is order of 2 to the power n, where n is the number of inputs this order is

required to do our functional testing. This we can bring down the number of test patterns we can bring down or we can move up the test speed, test speed, this we can move up, but moving test speed.

You can go up to megahertz you can go up to gigahertz, but going to terahertz or it is higher, than that we will require a tester which will be so expensive, that you can never make up a profit by selling the chips. We can make profit by selling the chips, if the yield is low that is if the fifty percent of the circuits are defective, so you can throw out 50 percent of the chips, other correct 50 percent, you can sell in the market.

And you can make a profit that is absolutely fine, but you can I mean to get the idea that if we have to test a chip in the terahertz the test equipment is so high that you can never make a profit, out of I mean use using the tester, and testing the chip and making a profit out of it. So, 80 equipments which I have shown in the last class is a very, very expensive equipment and that is the main reason that why we have to we cannot concentrate on or we cannot do that we can take the test to gigahertz or terahertz or any level.

So, what is that is I mean research is still going on to find out, if we can have a cheaper testers, which can apply test patterns in a fast rate, but this phases are very difficult phase to go on, but, so what people have researched and what people have found out. That if we can do somehow bring out this 2 to the power n, if this number can be brought down then the number of test patterns which has to be applied can be brought down, but still if you can have a good accuracy.

Then it can be a very good pattern of testing or you can say that it is a very good achievement, which you have made and this is absolutely what people have discovered by statistics, by statistics means a statistical results or history have a very important role in testing. So, in testing what you do you apply a certain kind of test strategy, and then you see what is the outcome for around say 2 to 3 years in different manufacturing industry.

For example, some let us assume that somebody has found out a technique in which we can apply only k pattern to test a circuit, when k this is very, very less than 2 to the power n. Then we go on using this number of test patterns and then we keep on testing with circuit and then we keep on finding out that keep on doing the billing, that this is a

normal circuit, this is a defective circuit, but we do not apply to the power n, we apply only k number of test patterns. Now, you have to find out the accuracy that what wrong you have done, that is if there is any case where, you have shift a faulty circuit telling that it is a normal 1.

So, if that is called inaccuracy in testing, but history by history people have found out that there can be very good strategies of determining this k number of transistors. Where, the accuracy is very, very high even it is as high as 99.9 percent plus, so that was a very surprising or what do you call very nice invention or discovery you can say in which people have found out that you can find out there are exist strategies. In which you can find out the k number of test patterns where k is much, much less than 2 to the power n, and still your confidence or your accuracy in testing is as high as 99.9 percent plus.

So, therefore, people research actually started taking more in this direction on reducing the test pattern other than making the test pattern application faster by expensive equipments. So, this bringing down this test patterns to k in number from 2 the power n can be possible through structural testing, so we will see what is the structural testing, he is the gentleman who introduced structural testing and he says that he verified the correctness of the specification of the structure of the circuit in terms of gates and interconnects. Like in a very simple way you say that I have a this is my circuits, so what the circuit does is actually makes an and of input 1 input 2 and input 3.

This is actually a functional test, but for structural test what we will do is that we will never verify, that whether the circuit is doing this ending of input 1 input 2 or input 3 correctly. Rather, what we will do is that it will find out whether this gate operating properly this gate is operating properly, and whether this interconnects that is the watts are correct or not.

Either nothing to do that whether it is a AND gate or whether it is a OR gate or with the multiplier it has nothing to absolutely nothing to do with this, it only verifies that individual gates and individual interconnects are proper or not. If that is fine then they say that the gate is structurally tested to be fine, and people have found that if we can do a proper structural testing then it it is equivalent or as accurate as a functional testing to a very, very high degree say about 99.9 percent plus.

So, the main area that or structural testing or the testing area the research mainly started moving to developing good strategies for structural testing, in structural testing it takes many fold less time compared to functional testing yet maintain the quality of test solution that is around 99.9 percent plus quality is maintained. So, as I told you the structural testing does not change the functionality of the entire circuit it has nothing to do whether the circuit is an adder or a subtractor or a multiplier or as strong as a processor.

It only checks whether the structural units generally in the units or gates in the general level the general definition are fault free as well as the interconnects or the leads are faulty. So, start you can tell that structural testing is a functional testing at the gate level, you just verify whether the gates are functionally correct as well as the leads are functionally correct. So, that is the generally we say that structural testing we do we are doing functional testing, but only in the gate level and not higher than that.

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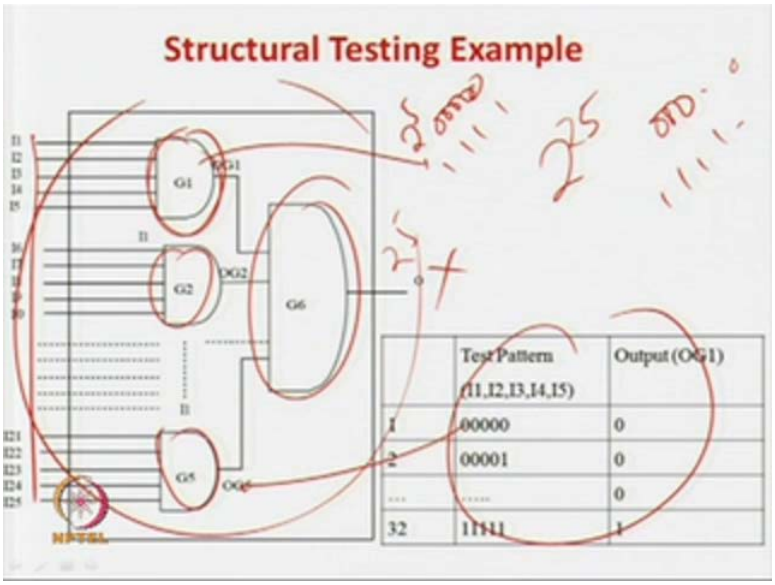

So, let us try to explain a structural testing by the example, which we will concentrating in the first slide, so this is again a the same circuit which actually does the ending of 25 inputs. Now, structural functional testing is order we require 2 to the power 25 inputs, where we started from all 0's to all 1's, now we will see what we do in this structural level. In structural level all the gates these gates are individual elements and we have to

find out, whether these gates are functionally proper or not and we have to find out that whether these inlets are correct.

So, I mean we see that if you test the gates automatically nets are checked, so if you want to find out whether this gate is properly functioning or not then what what are the patterns you have to apply 5 inputs, so 2 to the power 5 patterns you have to apply. So, the what will be the they will be 0 0 0 to 5 watts these are the patterns required to test each AND gate.

So, this implementation of the 25 leveling ending is done by 5 AND gates and there is another AND gate which is actually doing the final next level of this thing. This is how implementation there can be any other implementation of this function, so for this for this gate you have to apply 2 to the power 5, for this gate you have to apply 2 to the power five patterns and this gate you have to apply 2 to the power five patterns and again for this gate individually you have to apply 2 to the power patterns.

So, each gate now I am testing individually, but I am not testing the entire interconnection or what do you call the entire circuit entirely I am not testing, I am testing each gate individually, so number of test patterns equal to test each gates individually is this one that is 2 to the power 5. So, now, we can see, now what how many patterns we require for this is very less it is 2 to the power 5 into number of gates is 1 2 3 4 5 and 6, so this is 6 into 2 to the power 5, which is much, much less than 2 to the power 25.

So, see what we have done if you go for the functional testing of the whole circuit then you have to apply 2 to the power 25 25 inputs 25 inputs are available. That is a very high number, but now if I want to say that I want to i want to test this separately i want to test this separately and so forth, then for each gate you require 2 to the power 5 inputs and number of gates required is 6, so 6 into 2 to the power 5 25 is a much, much lesser quantity than 25. But, what I have not done, I have not done the integrity testing, but people have shown statistically that if you take this structural testing still the accuracy of functional testing is as high as 99.9 percent.

Now, you have to understand one very important thing, so what we are doing here, so if you are going for a structural testing you are applying 2 to the power 25 vectors, but now if you are applying functional testing then you are applying 6 into 2 to the power 5 test

vectors. So, the number of vectors being applied is a very less number of vectors, so you can this call this 2 to the power n and this is actually called k which is as per our last discussion, so this k is much less than 2 to the power n.

So, structural testing is telling you that you have to apply some 2 to the power k inputs, now which 2 to the power k inputs is also being told by the structural test which will elaborate later, but there is one very important thing you have to note that we said that structural testing is a very nice thing. So, you can test each gate individually and you have to apply only 6 into 2 to the power 25 sorry 6 into 2 to the power 5 test vectors, which is much, much less than 6 2 to the power 25 test vectors.

And the accuracy is 99.9 percent plus which has been seen through history and statistics, but then what we have to pay see the thing is not very simple. This gate if you want to test, so you apply 0 0 0 0 0 0 1 and so for this truth table you have apply, but you have to observe this output that this output is connected to this gate right and this is a circuit this is the circuit. So, this line is directly fitting into this end, so this thing is not available for the output to be observed, so one thing you can do is that you can bring this as a separate pin out from this circuit.

Then it is very easy you can apply this five inputs and you can observe this at the output, similarly for this gate also this gate is directly connected to this AND gate inside and this is not got out in the chain. So, you can test this circuit fine you can easily apply the test patterns, but you cannot observe it directly, so you can bring the pin out, so that is one thing, so for all such internets you have to bring pin outs. So, now you have decreased the test patterns from 2 to the power 25 to k, but k which is actually 6 into 2 to the power 5, but now you need to bring lot of pin outs from the circuit that is actually a very, very difficult situation, because if you have 1000 nets which you have to observe.

Then you have to have around 1000 extra pins in the circuit which is again a very infeasible situation, so we will see how to handle this, so this is the polarity of the structural test. Secondly, if you have to test this gate, this last input ending then output will be observed because this is directly coming out of the circuit, but now see again this inputs to this end gate are not directly controllable, because they are being fed by this five end gates.

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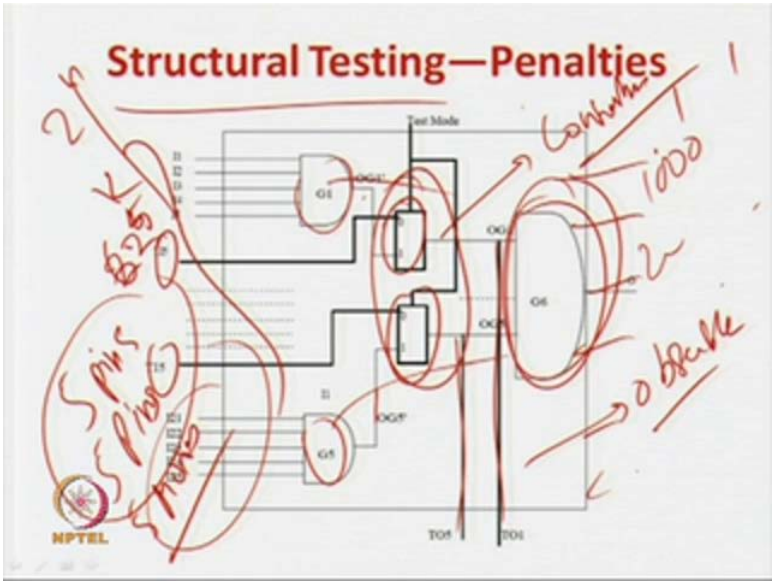

So, this gate is fitting this gate is fitting, so you cannot directly control them, so for that you have to make a very different arrangement, so we will just see, so for these cases for the output, you can say this for the outputs this gate and this gate outputs, so which we have brought them as separate pins. This is one kind of a penalty, so if there is around 1000 such nets to be observed, then you require 1000 pins extra which is infeasible.

So, we will surely see, how we can do away with this, but another more important problem that that arise now is that see this end gate this end gate is directly this was directly connected by this one and similarly for this. Now, what that happened is you have to somehow somehow what you have to do is that you have to control this gates, now you cannot observe this right, so this this gate is not directly controllable.

Let us again go back to the original figure, so you can see, so now what you do somehow you have brought pins out and we can we can observe the value, but this gate this gate is driving this and gate. So, I cannot apply any pattern over here directly, so there should be some extra arrangements, so that I can somehow apply the pattern here, so how can do this because there is a some gate like this say for example, this is connected by another gate.

Now, you want to apply some pattern here, so how can you do that first you have to decouple this gate, you now otherwise this gate is driving this gate, so somehow you have to decouple this gate and then you can apply some pattern. This is how it is being

done, so you see what they have done, they have put a 2 is to 1 multiplexer here and then they have said that there is something called a test mode they applied. So, when you say that the test mode is 0, then what happens this output, so they sorry let us say that you apply one over here first say, if the test mode we apply 1.

So, in the test mode if you apply one, then what happens the output of the gate is through this flip 2 is to 1 multiplexer gets directly connected to this AND gate and the circuit function normally. So, in this case also if it is 1, so this output is connected here and it fits the AND gate and the circuit is doing a round a round operation, but now when I want to do a test operation.

So, if you do a test operation, so what you need to do you need to somehow ensure that this guy is decoupled that is this gate should not be able to control this, and this gate should not be able to control this and we should be able to put some values here. So, now, you make this test pattern as test mode as 0, so if you make this test mode as 0, so this guy connection is crossed by this multiplexer similarly, this is one this gate crossed and there are some extra around pins controlled pins which gets our direct access to this gates.

So, in this case there you can apply 0 0 0 0 0 1 or whatever you want, so now, what see what we have done, so there was our this is the gate and this is the line, so there is a internal gate say some other gate which is driving it. Now, to apply a test pattern because, now our idea is to test this gate individual other than the whole circuit, so what we have to do, so this some other gate is driving this gate. So, in the test mode somehow we have to make this gate unable to drive this and there should be some extra pin outs which should now be able to drive this gate.

So, that you can apply test patterns as you like, so that you can test this gate individually, so this is possible in this case or in all cases by using what do you call 2 is to 1 multiplexer, so basic architecture is something like this it is case of 0 and one this is called the test mode. So, when the circuit is not in a test mode or normal operation, then the normal net which is to be fitting is connected, so it fits there, but when you make the test case test mode equal to 0 that when you want to do the testing.

So, this normal cloud or normal combinational thing which is fitting this gate is decoupled, and this separate pin out is called the test pin you can call then this gate is

connected to this gate, so which is driving it and you can apply test patterns to test the circuit directly. So, this is called controllability, so what we have to do in case of structural testing there are two things one thing is observability that output of these gates has to be observable.

So, this you can very easily do by bringing these two extra pin outs that is called observability, this is what observable. Now, you have to also apply to test these gates because these 2 pins you cannot control directly, because these gates are fitting, so what you have to do you have to put this 2 is to 1 multiplexer arrangements. So, that these lines also become controllable this are actually become controllable (( )), so what happens, so in structural testing what we have done we have brought down from 2 to the power n to some k, so in this case this was see 2 is 6 into 2 to the power 5, but what we have to do we have to have some extra pins.

So, how many extra pins for this 5 gates, we have to have 5 pins extra and then again that is for observation, observability and now for controlling this inputs of this gate you require how many control pins that is there are 5 pins for this. So, you require 5 extra pins that is the control pins here, and as you are less what do you have to do as well as put some multiplexes, so how many multiplexers you require in this case. So, in this case multiplexers will be also be 5 maxes, so this is how this is how it is a very difficult problem or you should not call it a difficult problem, you say that you have to apply some more penalties.

Like structural testing is bringing down the test count, but you will require extra pin outs and you require extra multiplexers. So, extra pin outs is very difficult because if we have 1000 lines then you require around say 2000 extra pins or something, so a circuit having extra 2000 pins is a very infeasible situation.

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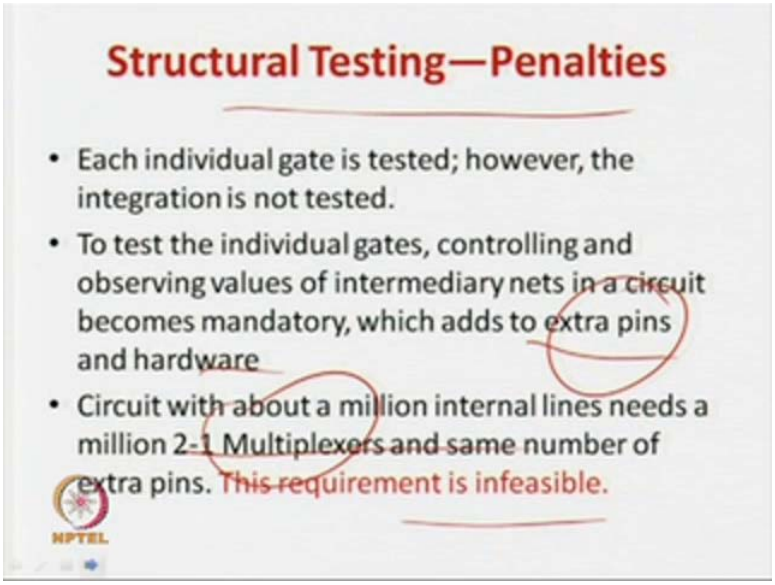

So, let us see how we can handle this, so this is what we have been discussing the number of test patterns requires in this case will 6 into 2 to the power 5, which is around 160, which is much, much lesser than 2 to the power 25. So, if you are having same tester which is one megahertz tester, then the time required for testing is only this seconds, and if you have to test a million million samples then you require only 16 seconds.

So, structural testing is what has to be adopted, but that is very good, but the penalties of extra pins extra maxes somehow we have to take take this things into feature. So, now, we will see how we can handle this that is people have people could have not yet solved the the functional testing is very good because you need not have extra pins, you need not have an extra maxes, but still you have to number of test patterns are very high 2 to the power 25 in this case.

And the frequency if you have if you cannot apply the test patterns at very, very high speed then this timing is infeasible, but in structural testing you can see that in 16 seconds we can test one million samples, but extra pin out and extra maxes are there. So, research now have been done, which we will starting in this course and mainly we will see something is like lecture today also, and how pins and multiplexers can be brought down that is feasible, but still taking the test frequency higher and going for functional testing is a difficult problem.

So, that is what about the structural testing penalties which we have discussed, so you require what you call extra pin outs and some multiplexers, so I mean this requirements are actually directly infeasible. So, you cannot have that high requirements, so let us see how we can handle the problem of extra pin outs and extra multiplexers.

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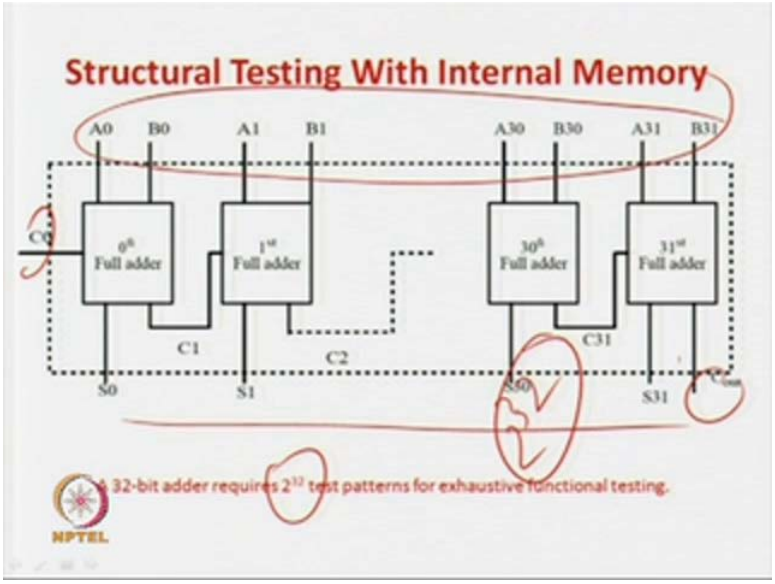

So, we will take a very simple another example with of of structural testing with internal memory, so our main goal is that we cannot have, so much amount of pin outs. Say for example, I say that I give you 2000 flip flops or I sorry I say I give you 2 to 2 is to 1 multiplexer 200 300 500 1000, whatever is possible I will give you, because they will only increase by circuit area.

But, if I have a chip size of this much, so there is a fixed number of pins which can be applied on the circuit, if this goes to 20,000 or something then it become infeasible to manufacture a device, so 20,000 sample chip will may be as larger as this what do you call this, whole what do you can call even may be as large as your what do you call your laptop.

So, this one chip size may be as large as you laptop if you require, so called your 20,000 input page, but this is also not a very good idea, but still I can say that I cannot make manufacture a chip with sizes about a laptop, but still I can have a chip and I can give you another big area in the chip itself where you can have 20,000 muxes. That is still possible not desirable, but still possible, so let us see with an example, how we can do

away with this major major nightmare problem of the pin outs, so first you have to handle the bigger problem that is of the pin outs, and then we will see the problem of the lesser dimension that is actually the multiplexers.

So, this is a what do you call a little carry order you can say 32 bit repel carry 32 bits are the inputs and this is the carry this is the sum and then you can have a carrier so; obviously, if you want to do a structural testing you require 2 to the power 32 input patterns which is again infeasible in terms of time.

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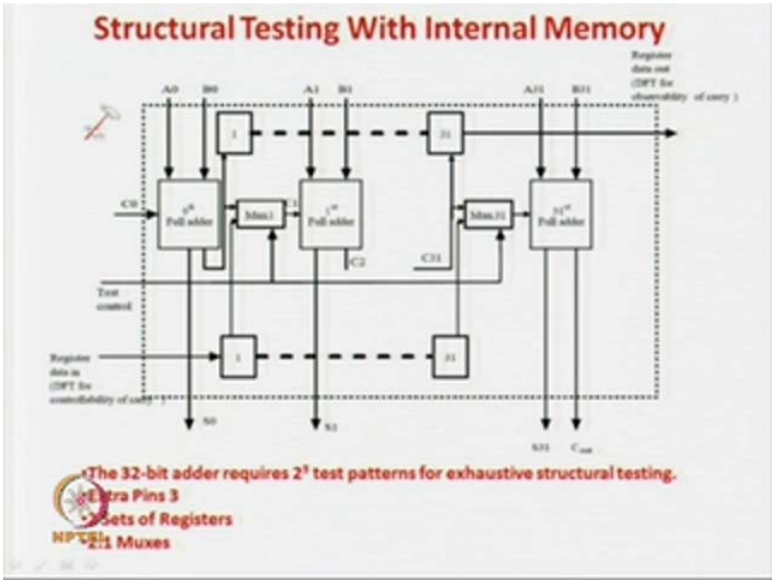

So, how to handle this, so let us do a structural testing here, so structural testing in this case, in the last case the structural testing was the gate was the unit that we were testing a gate at the unit level and we were testing the interconnects. Now, in this case we will not consider gate as a unit level, we will take it up much to a broader level, where each full adder is the unit, so we will consider this as a unit we will apply the patterns here and we will observe the patterns here.

So, there will be there are some more gates inside or for this testing, this kind of structural testing we are considering this as our unit, so you see structural testing as I told you is a functional testing at the unit level. So in the last, in the general example which we follow throughout or in the last example the gate was the unit, but now for us this full adder actually is our unit. So, to test it we as you know that the full adder has the three

inputs this is the A B, this is this carry input, then we have to sum, and then we have to carry out.

So, now, we have to apply this three inputs that is 2 to the power 3 inputs only you have to apply per half I mean full adder, then you have to see 2 outputs, that is the sum out and the carry out. So now, if you look at the structure, in this case it is very simple to apply the inputs because they are all available at the pin outs and we are going to test each individual stuff at a level, and also the sum output is may be simple you can easily get this amount put and also the carry output.

Now, the problem is that for individual I told you that these are the inputs, this intermediate carry that also has to be observed, this is the that is this is the intermediate intermediate carry, this intermediate carry is going from here to here and here to here, so this also you have observe. So, once is this thing was there we can take a pin out, but as I already told you that bringing that pin out is infeasible in terms of the number of pins, so somehow we have to handle this one, so how it is handled, so in this case people have applied a very simple logic.

So, in this case we have a what do you call sorry, so we have a simple shift resistor, so what do you do, so if intermediate carry output of this gate is fitting this for the time being forget about the multiplexer. This will fit to the next level of the adder and also the same time same thing is writing to a shift resistor, again there will be another element of this shift resistor which will be again fit by the output of this gate. Similarly, the output of the second last full adder will again go to fit the last full adder as well as it will also write the 31 shift resistor, so we have a 32 bit shift resistor here.

So, now, what is happening, so whenever we get the output the sum you can observe here, so what you are going to apply, so you are applying applying all the data's for a full full adder, now one this sum you can directly see here and the carry is propagated from this one to this one and so forth. At the same time instead of drawing the pin outs of this carry, so what you are doing we are fitting it to a intermediate, which we are having a shift resistor, so we are fitting this resistor.

So, when all the testing is done, so all this units of this shift resistor have the values of this 32 bit intermediate carry, then you can apply 32 clock pulses, so that this data is correct. So, now, in this case you require 32 clock pulses to get the result, because now

we are not bringing this parallel this output of the carry, rather what we are doing is that we are fitting this carry to this units or shift resistors.

So, now once the testing is done the shift resistor will be loaded with this value, and in single go you cannot have the result, we have to shift to the result in a sequential manner, so 32 clock pulses will be required or I mean order of 32 you can forget about the last carry bit, so they have to be shifted out of this this thing. So, now, still you cannot say that I have totally done away with this pin business, because we require one extra thing that is this if there will be a clock for this shift resistor, and as one pin to bring it. So, what we have to achieve, so if you directly bring out this carry outs from all these adders then you require say around 31 or the order of 32 kind of pins.

And now what we have achieved we require only one clock pin and one shift pin that is shift out you can call register out, that is observation from the carry, so instead of 31 or 32 pins in this case we have bought what do you call 2 pins we have done with this. But, what is the penalty paid now the penalty paid is we require 32 clock pulses to get the value, now there is another point that is about the observablility.

Now, if you do get this full adder, so what do you have to do again the this full adder, these two are the inputs A and B, which can be directly controlled, but there is another full adder here which is directly fitting to this carrier. So, somehow we have to again when we are going to test this full adder we need to somehow decouple this as in the last phase example of the AND gate we have seen, so you have to decouple this somehow and then we have to apply the test pattern whatever is required.

So, same philosophy we apply we apply 2 is to 1 multiplexer over here and there is the test control, so whenever test control is say 0 or what whatever, so you get in one control this this output of this will feed, this the output of this will feed this and so forth. And wherever you are test mode the what will happen this guy will be discoupled, this guy will be discoupled, this decoupled and you can have a directly control of this what do you call this multiplexer, sorry this and this carry through the multiplexer.

So, in this case you have seen what happens, so in the test mode this is decoupled and this you can have direct control of this carry by this multiplexer. Now, in the last example we have seen that to control this we have directly bought this as a pin out, we

have directly brought this as a pin out, we have directly brought this as a pin out, which was again actually taking a huge amount of area, sorry huge amount of pin outs.

So, now, again to solve the problem they have again put a shift resistor over here, so whatever carry values you require at this, at this, at this you can shift it in a shift resistor slowly that will again take 32 clock pulses, because now you cannot feed everything directly. Here, to do slowly in 32 clock pulses, but now this again only another pin out is required, so instead of directly controllable pins, which we could have brought out and also the observable pins which we require to be brought out in the previous example.

Now, we are putting a shift resistor, so this shift resistor is requiring only 2 extra pins that is actually your clock pin and your shifting in pin, so that you can get the data ready in this in the individual points. It of course, takes some clock period, but you are hugely reduced in the test time, I am sorry you are hugely reduced in the number of pin outs, so structural testing with internal memory reduces your your pins pin outs, but we actually require more number of same number of multiplexers.

But, now you have added two new shift resistors, but as I told you increasing area in a circuit is still feasible, but we cannot allow to increase 64 more pins, because you require some pin outs for each of the outputs of this carry last is already there. So, we requiring 31 pin outs to observe the carries and also you require 31 pin out pins to control the individual carry, so this is not at all possible.

So, that this actually more 60 to test a circuit you cannot develop your pin counts or hammer such a huge number of pins, because they are in circuit itself or the package itself will be having, so many pins, that one chip can be as large as your may be your laptop. So, by using this internal shift resistors we have solved the problem, so so in this case we have solved the problem, but again we have added some more area which is for the resistor, now we will see how can we again solve this problem, how can you minimize this area of the extra this thing.

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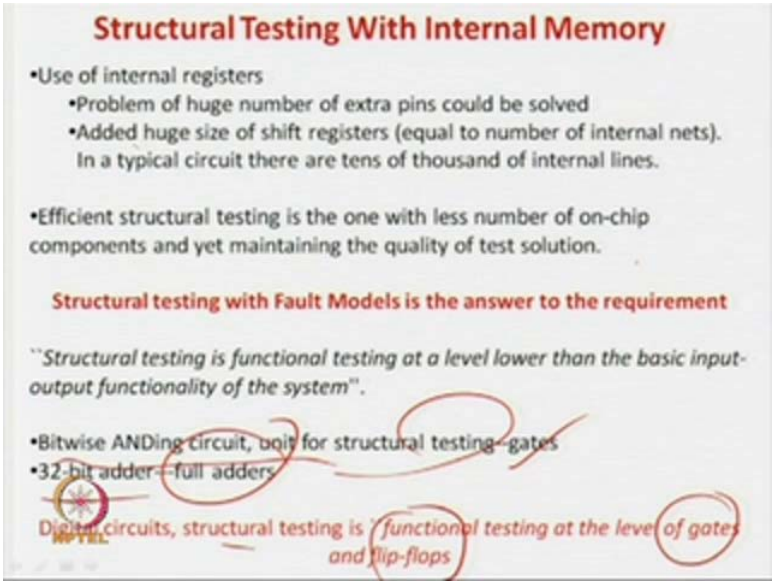

So, you see what you have discussed that if you are doing structural testing with internal memory we require internal registers that is file, but the huge number of pins have been solved, so what is the number of shift resistors you can see that is equal to the number of internal lines have to be tested. So, if there are 10,000 say internal lines then you require around say 20,000 I mean 20,000, then you may require order of 20,000 blocks or 20,000 flip flops in each shift resistor.

That is I mean for each let you require one element of this shift resistor shift resistor consists of one flip flop per per net will control, so that is also a very high in number, but still that is less amount of a problem than the pin outs, but now we will see how we can also handle the issue of this large number of pins, sorry large number of this internal shift resistors.

So, now we will see structural testing with fault model we will actually solve the problem that we will see, so now, we can say that the some key terms like structural testing is the functional testing at the lower level than the basic input output functionality of the system. That means, what, so if you have a circuit says like this, so if you want to do a functional testing then you have to say verify that whether 2 to the power n systems are very fine.

I mean 2 to the power n number of inputs are very fine, but now if you are going for structural testing then you can break up your circuit into individual blocks, and then we

find out whether you assume that you have to just test whether this blocks are individually correct or not inside this things we are not bothered. So, in the, in a general structural testing in which we is the term which is used in testing, the basic block levels are the gates even and sometimes we can even go up a bit higher.

Like in the previous example, our unit was a full adder we were not bothered to go inside the adder and test it, but whether we were finding out that structurally the interconnection should be fine, and our case we were functionally testing the full adder. And inside we were not going and structurally, you were testing that is whether each full adder is structurally proper or functionally proper or not and the full 32 bit adder we were testing structurally.

In other words our full 32 bit adder was the unit or the functional circuit, so that was the functional element and the block levels were the full adders. And we were testing these were the as the units, but in the example, in the example before that our circuit was 25 bit input and the and our individual block was the gate. So, in testing in the taxonomy or in the terminology of testing what do you called this unit is the gate, so we do not I mean generally do not go to an abstract level like adder or a something like that our unit is generally testing.

So, in this case the bitwise handing unit the structural unit was a gate, and the 34 bit adder the full adders were the units. So, in digital circuit structural testing basically functional testing at the unit of gates and flip flops, so flip flops and gates considered as units in the general structural testing terminology.

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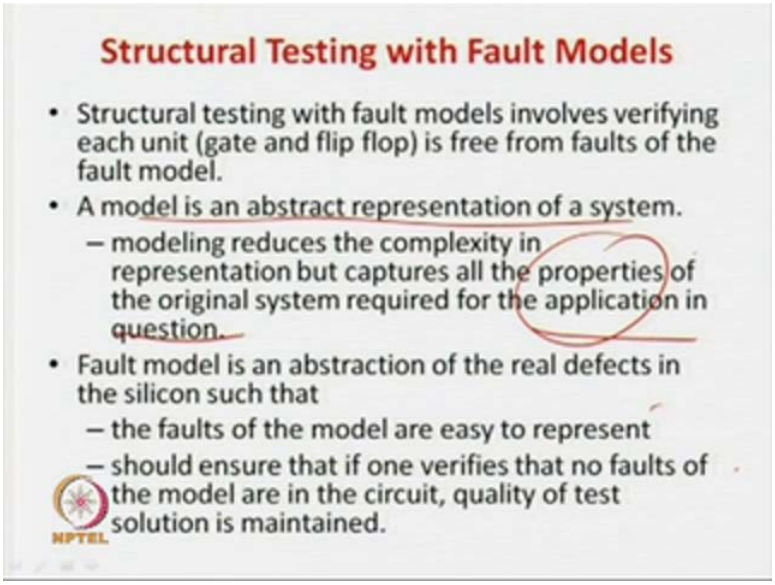

So, only for the example we had showed you for the full adder, but you cannot go think that is a general terminology kind of a thing this was only for the example to illustrate that what is the structural testing and what is the functional testing. So, till now we have seen that functional testing is difficult, because of the exponential number of test patterns and structural testing is beneficial, because it can give you a very less number of test patterns.

As well as you can have what you can called we can have k number of pins I mean sorry k number of test patterns, which is much, much less than 2 to the power n number of test patterns yet the accuracy is very high, I mean as large as 99.9 percent plus. But, what we have problems the problem is the huge number of pin outs and also there can be large number of internal 2 is to 1 multiplexers and what do you call registers.

So, we have seen that by using registers, we can still save a lot amount of the pins, but still the number of registers was yet the problem, so number of test large number of input patterns, we solved was in structural testing then using the internal registers we have solved the problem of large number of pin outs in structural testing. So, initially what we have functional testing then, that is 2 to the power n, so you use structural test then we brought it down to k then we have large pins large pin pin outs then this we have solved using these registers, so now, we are in a position that we have a huge number of registers.

So, this is what is flow, so now, what we have to solve we have to see how we can solve the large number of registers in and also 2 is to 1 multiplexers in structural testing. So, again what came into this solution is structural testing with fault models, so now, again what we have seen in the last example that we have a structural testing like a gate as a unit as a gate or a full adder then what do you verify, we verify that whether the AND gate is functionally correct that is 0 0 0 1 1 0 1 1.

And in case of full adder we have to verify whether it is doing the addition very sum and carry out is proper or not, but if I go for a structural testing with fault model we will even forget that a AND gate is a AND gate and a full adder is a adder. So, what we will verify is see given an AND gate, we will assume that we do not have any fault from the fault model. So, we will see I mean elaborating this, but now the philosophy in structural testing with fault model is that we will not even think that AND gate is a AND gate, what do you call full adder is a full adder, that is we will completely forget about the functionality of the units.

So, what is the model basically if you ask me, so model is a model is basically a representation of the circuit representation of a system in a very simple way, but it actually have to have all the properties or as high amount of properties, which is required for the particular application in testing. For example, now our problem is to test the circuit that is we have to verify that whether the circuit is correct or whether the circuit has any defects or not.

So, for that we if we have some model then our model should be enough only because see our testing our goal is not to find out whether a AND gate is a AND gate or a OR gate is a OR gate. Basically, our main goal is to find out whether the circuit is having any defects or not or the circuit is having fault or not, so for that if you can find out any fault model which need not be functionality of the gate, but still if it can serve the purpose of testing then we have got a very good fault model.

So, the for a fault model basically reduces the complexity of the presentation, but at the same time you have to understand that it represents or it does your job or does the job of or meets the specification for that particular context in this case which is a what do you call in this testing in this case is testing.

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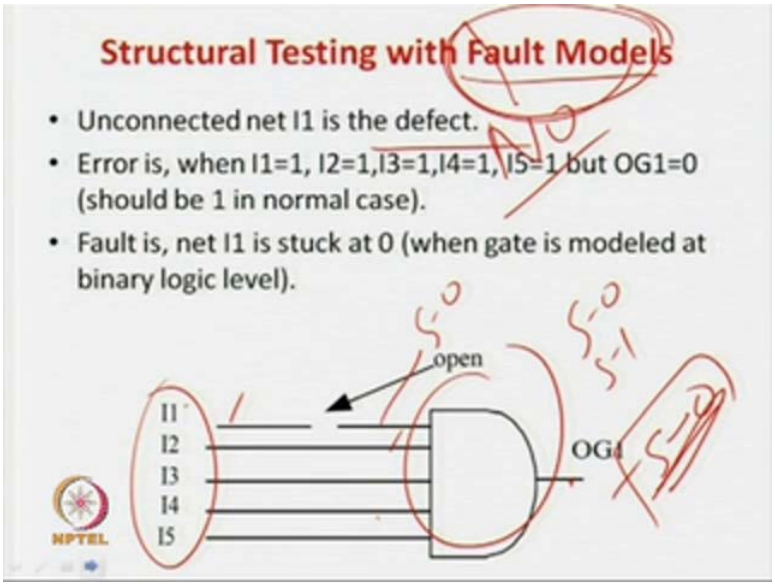

So, we will take an example, so you can understand better, so this is a and gate, so we have already seen that and in case of NAND gate is, so complex it has a transistor level it can be fault layout level it can be fault, so lot of faults can be there. So, for example, let us assume that this is a start open fault, this line is somehow cut this input is somehow cut, so this is actually called the defect that the layout is not proper this layout should be metal should be like this, but somehow there is an opening, so this is called the error, so there can be hundreds of or thousands of defects sorry this is called defect.

So, there can you can say that this is the wire, so the wire is as thick for some place maybe the wire is not cut, but the this is a very this has become very thin, so that can be a defect, so they it can be saying that somewhere the line is big thick that can also be a defect. So, that is very difficult you cannot do all the testing in this small amount of time which is given, so in this case this is start open somehow this is the defect, now what is an error, so error is actually representation of this defect.

So, in this case if you apply everywhere 1 1 1 and so forth, then the answer should be one in the normal case, but in the fault in the error case it is 0. So, error actually represent the manifestation of this defect, now you can see now I can say another way that there is a fault, so this is the error is the manifestation of the defect and fault is the logical representation, so you can say that this net is stuck at 0 and also this net is stuck

at 0. Because, whatever value we apply this can never be 1 and this gate can this gate can never be 1, so structural testing or sorry fault model basically says in this 1.

So, I will I will just say in in another words, so if you want to do a structural testing of the gates, so you have to find out that you apply 0 0 0 0 0 to all 1's and then you have to find out whether the output is 0 and 1 in the respective cases. So, that is about the structural testing of the gate at the functional level, because I told you structural testing is the at the gate level is functional testing of the gate or that requires lot of resistors and so forth.

So, now, what in fault model it says that that is I say that if this line is open that is a defect, because now because I am doing testing, so I am not interested to find out whether this gate is structurally correct or not. But, whether I am motivated to know that there should not be any defect in this circuit, you know that is testing in case of circuits is not to guarantee or not to ensure that the gate the circuit is functionally proper.

That you have very difficult because it takes very long time, so I want I want to do is that, I want to find out that there is no defects, but testing for no defect is long time because you have to is lot of physical defects, there is lot of crystal defects and it goes into physics. So, what I can say that if I say that this line is stuck at 0 and this line is stuck at 0, in this case because in this case if it is stuck at 0, if you apply anything this line can never be one and similar in this case, so I can say that this line is stuck at 0, so if I can ensure that this line is not stuck at 0 stuck at 1, this line is not stuck at 0 and stuck at 1.

Similarly, for this case and similarly for this case then I can say that my AND gate is not having any kind of stuck at 0 or stuck at 1, so we are not saying that the gate is a AND gate and is properly behaving or the functionality is correct. But, we can only say that the structural testing says that this AND gate does not have any stuck at 0 at this point and neither in this lines, so this is actually called structural testing at the fault model.

Now, what is this fault model in this case the fault model in this case is the stuck at 0 and stuck at 1, because these are digital circuits, so each line can be either normal stuck at 0 or stuck at one, so this is how it can be done. So, now we will see how we can or I mean be in this lecture or in a few more lectures we will see, how this (( )) structural model helps us to reduce the problem of resistors.

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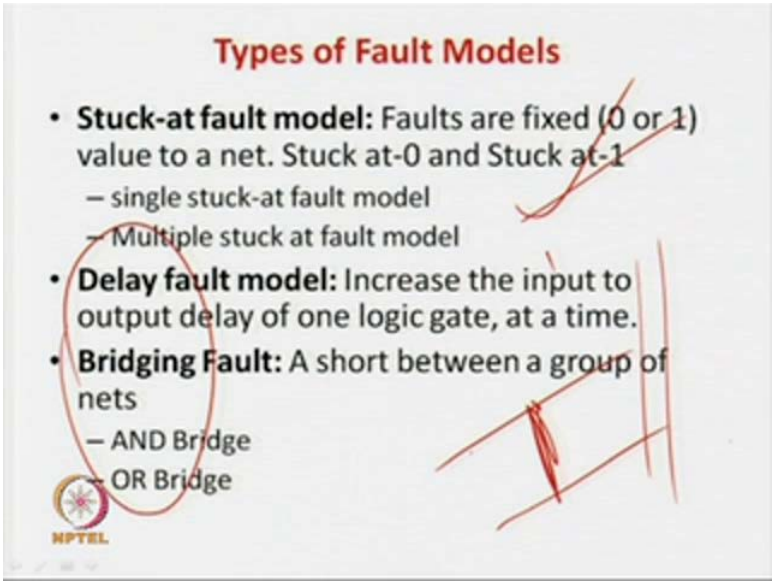

So, there are difference for models, so struck at fault model is what each line can be stuck at 0 and stuck at 1, so there can be a delay fault, so in delay fault the lines do not have a stuck at 0 or stuck at 1, but in the normal time. If you require n amount of time fault to write from 0 to one in a delay fault the delay will be higher similarly in case of this is rise delay similarly there can be a fall delay, so the delay will be higher.

So, this is about a delay fault model, so that is circuit is normal or the logic is normal, but there is a delay to rise and fall. Then there is an a bridging fault that is in between two lines there can be a short, so these are some complex fault models which you will not study in this course, mainly we will see at the stuck at for which is the most widely accepted fault model, because it has been seen that if you can adapt to this fault model a large number of faults of this nature and more advanced nature gets captured.

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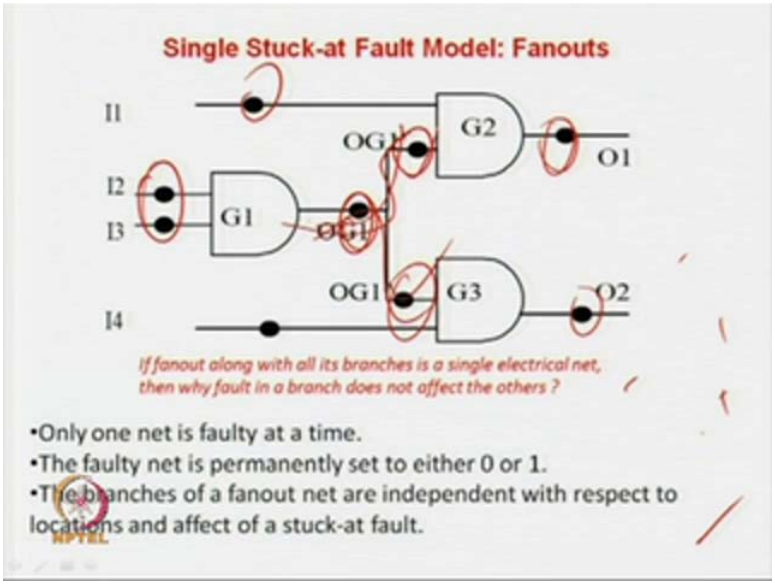

So, we will see this fault model, so let us see how how a fault circuit with a fault model with nuclei, so there is a circuit now we in structural testing what we have done we have to test this guy individually, you have to test this guy individually, and this guy individually. For that we have to bring you have to observe this at the output, so you have to bring them to the output then we have to control, these two guys to test these two things.

Then you have to put a 2 is to 1 multiplexer here and then we have to either bring this controlling lying out or you have to have a 2 bit, what do you call register here to control this things. So, that was the main difficulty in this case, pin outs here reduced by the what do you called registers, but we could not have done about the registers, that problem was still remaining.

So, now in this case what we have done, so if you are doing a structural testing not at the functional level that is the fault level fault model level then what we have to do we have to verify, we do not have think that this is a AND gate, we do not have to think this is a AND gate and so forth. We have to just verify that this line does not have a stuck at 0 or stuck at 1, this line does not have same stuck 0 stuck one and so forth, so we are all the full circuit we are breaking down into individual nets.

This is one net, this is one net, these are the two nets, these are the two nets. And this we will see these are fan outs this has to be handled separately we will see, so each of the

nets we have individually, concerned considered and apply you have to apply a test pattern which will verify that none of the gates have a stuck at 0 or stuck at 1 fault. So, now we are doing a structural testing, but this is not at a functional level and it has been shown that you can if you can do this then also the test coverage is as high as again 99 percent accuracy.

So, slowly we have to see how in a few lectures down the line we will see, how this structural testing with this fault model will help to reduce the number of registers number of pin and everything will be very (()), but for the time being just take it for granted take it from my side. That if you can if you even test a circuit forgetting about the functionality of the AND gates and just verify that this nets do not have a stuck at 0 and stuck at 1 faults still the coverage is as high as or you can say that the accuracy as a 99.9 percent plus.

But, there is a very interesting fact here which I should mention that this is a individual net fine, this is a these are two individual nets fine, but this is a single electric (( )), but still this stuck at fault model is that you have to consider this as a individual net, this as a individual net, and this as a individual net. That is a fan out, if this is a fan out you can have a stuck at fault here, then the stuck at fault may not be here, you can have a stuck at fault in this then this two lines are free of stuck at faults.

Then it may happen that this guy is not having any stuck at fault the third net can have a stuck at fault, even this whole line is electrically single, but this are having 3 faults, 3 individual faults can be there. Then now you can ask me the question why is it, so the answer is this has been found statistically, that is because the circuit generally do not have a stuck at fault.

Now, only what we are verifying that we are saying that if you apply test patterns which verify that this lines or this circuit is free of stuck at faults, then then you can say that what you can say that, so the what what I was saying that we are not in fact, testing we are not testing what. So, we are not trying to ensure that our circuit is free of faults which you are we are we are trying to ensure say that as we are not trying to say that the circuit is not done. Rather what we are saying we are trying to say that our circuit is having not stuck at faults, that is what we are trying to say then you are saying that no stuck at faults stuck at 0 stuck at faults are no their.

That implies that circuit is 99.9 percent plus chance that normal, but we are not actually telling the other way round, that we are not claiming we are not saying the other way that if the circuit is normal then no stuck at fault this is not our claim kind of thing. So, what we are trying to say that we are verifying that the circuit is having no stuck at faults, then it is 99.9 percent chances that the circuit is a normal (()), so they say that if we treat this as a single net, then it has been found out I mean by statistics of the history that if we only consider this fault then the accuracy is lower.

So, we have to also consider this as a individual net this as a individual net, so basically this is a model, in reality circuit does not have stuck at faults kind of (()). It is not as good or as neat as a single stuck at 0 and stuck at one only we are verifying that no stuck at fault implying that the circuit is normal, so for that reason we have to also consider this things.

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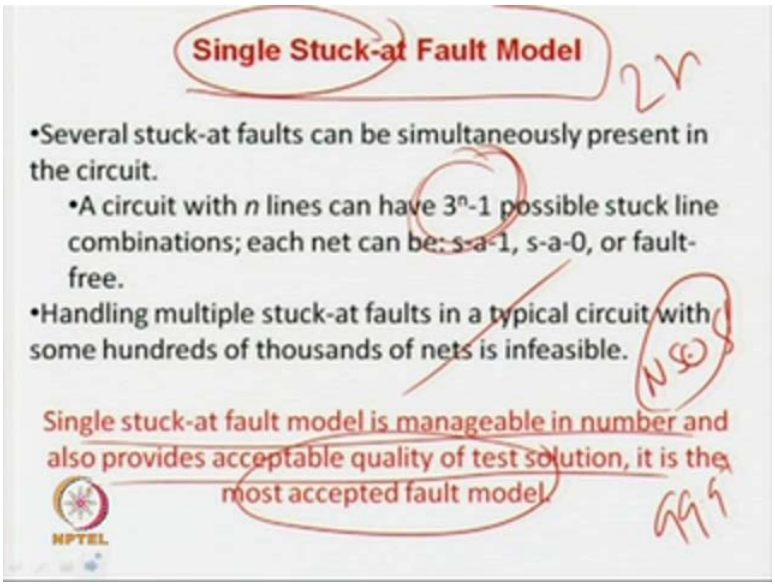

So, generally you can ask me that how many stuck at faults at a time, so basically the idea is that we we can you can say that, you can have 1 lines each line can have a stuck at fault. Now, pair of lines can have a stuck at fault, 3 lines can have a stuck at fault and dot, dot, dot, but if you consider this the number of stuck at faults will be extremely high it will be actually three to the power n minus one because normal stuck at 0, stuck at 1.

So, if you consider all combination which will be 2 to the power 3 3 to the power n minus 1 with a huge number of faults, so you cannot do away that thing, because it is

very difficult to handle it. So, again statistically it has been found that if you consider single stuck at fault, that actually what is a single stuck at fault you have to think that only one fault at a time, I will all consider all the stuck at faults that is true, but first I will find out that this fault is not there.

Then I will assume that if I find that this fault is not there that is very good, then I will test for this one this fault is not there, then it is fine and so forth. So, I will consider one fault at a time, so if if there are n nets and I consider one fault at a time, so how many faults are there is actually 2 n. So, if I consider all combinations, that is this line, this line, this line, this line and so forth, all combinations if I take it is 3 to the power n minus 1.

But if I consider that only one fault can happen at a time, but I I will consider each one, but individually 1 1 at a time, then it is only 2 n and statistically it has been found that even if you are having taking single stuck at fault model. That is handling multiple faults is very infeasible with huge number of nets, but single stuck at fault is manageable in number and it also provide acceptable test quality. That is we are taking one net having a stuck at 0, at a time verifying it is not there, then you are considering the same net with suck at one verifying it is not there.

And stepwise one at a time for each net, if we verify then it is called single stuck at fault the number of faults are 2 n, if the number of nets are n then the number of faults are very manageable, because a 10,000 lines in a circuit means only 20,000 number of faults. And then you can say that an (( )) that the this is a very acceptable fault model, because what do you call this is a very acceptable, because this type of testing will be less (()) the accuracy is around 99.9 percent plus.

So, that is why the single stuck at fault model gives only 2 n faults whereas, the number of nets in the circuit as well as it is the accuracy is also 99.9 percent plus, so people have found out that single stuck at fault model is a very good and a widely adapted fault model.

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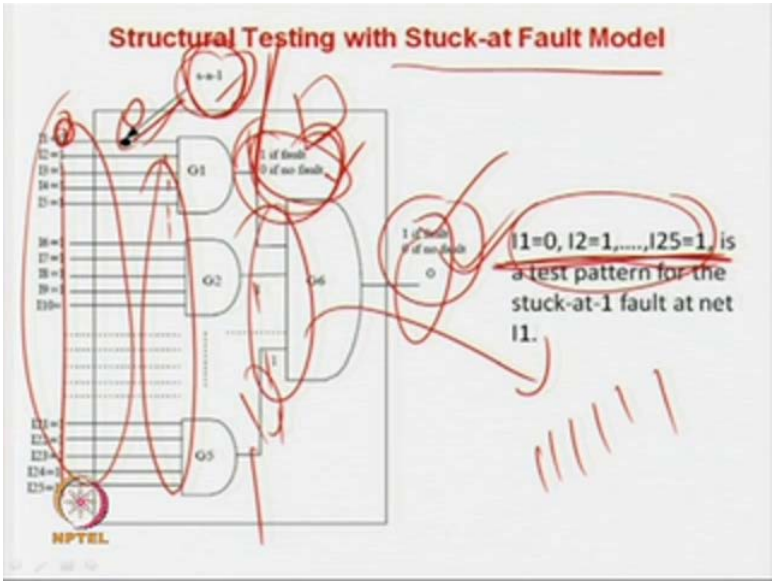

So, in all future discussion we will be using a single stuck at fault model, so some examples, if I can ask you how do you test using a single stuck at fault model, so let us consider this circuit, so let us say that this net is now having a stuck at 0 fault, so to test a stuck at 0 what you have to do you have to apply a one over here, because this stuck at 0. You can assume that the electric bulb is fused, so to test that the active bulb is not fused what we have to do we have to put the switch on, so in this case it is stuck at 0, so you have to apply a one over here, so you have to apply a one over here.

Now, you can understand that to see that whether I mean that is what will happen if the circuit is having a fault, you will get the answer 0, because of the stuck nature. And if the circuit is normal you will get a one, but now it is an AND gate, so if I put a 0 in the last net say this net I put a 0. Then what will happen irrespective of fault is there or not the output will be 0, because this guy will be controlling this output, so to avoid this what we have to do is that we have to apply all the other lines as 1 1 1 1 1.

Then what will happen I will apply also 1 at this line, so what will happen here if I apply 1 at all the lines then what happen in the normal case, the answer will be 1, but if there is a stuck at 0 in this net the answer will be a 0, this is for the fault and this is for the normal, but if I somehow apply a 0 over any other cases then this effect is not brought out in the picture. Similarly, so this is what you are getting 0, if the fault is there and 1 if

the fault is not there, so again this out this has this effect has to propagate to the output, so what I am doing I am not as I already told you neither I am putting any pin outs.

To observe this output neither I am going to put any multiplexer or any register for that, so now, the fault effect is here, that is 0 if the fault is there and one if the fault is not, but I am not able to observe it, because I am not I have not got any pin out here, so no pin out is here, so I have to propagate this value through this gate. So, now what I do is somehow I get a 0 over here then the propagates propagation is not there because 0 will be propagated, so what I i have to do, so to keep this effect here I have to apply one over here, I have to apply a 1 over here and so forth.

So, to get a 1 over here all the inputs of the all other and gates should be 1, so the input pattern 1 1 1 1 1 1 all 1's, if you get the answer one then you can say that the stuck at 0 fault is not there, and if you get answer is 0, then you can say that a stuck at 0 fault is there. So, by applying this pattern you can ensure that if the answer is 0 the stuck at fault is there and if the fault answer is 1, then no structural fault is there, so structural testing with fault model stuck at 0, 1 fault by applying this pattern.

What we have verified that without using any extra pin or without using any extra stuff, we have verified that our with that our stuck at fault 0 fault is not there, or if you simply reverse it if you say that there is a stuck at one fault over here. Now, same thing it is stuck at 1, so you have to somehow apply a 0 over here, so I put a 0 in this case and because of the observability thing I told you that the fault effect this effect that if the circuit is stuck at one here i put all 1 1 1 1 in this input of the AND gate.

So, if the circuit is normal, so this is 0 you applied the answer should be 0 and if this net is somehow stuck at one, so you will get a 1. So, this thought it has to be this effect it has to be propagated to this AND gate all the other inputs have to be 1 1 1 1, so the pattern this 1, that this net is 0 and all other are 1's will actually propagate this fault effect to the output. So, what is the effect, the effect is one if there is a stuck at one fault here the answer is 0, the what do you call the this circuit has no fault.

So, this is the pattern which verifies that there is no stuck at one fault at this level, similarly we do not require any extra net or any extra controllability to test this one, so we have seen that structural testing with stuck at fault model is a really a very helpful in

this saves that we do not require any extra pin outs as well as we do not require any multiplexers or what do you call the register.

But, somehow we have to find out which pattern to apply to test this stuck at fault fault, so for this net we have tested for stuck at one and stuck at 0. So, we have found that if all 1's we apply we can test for stuck at 0 and if you apply this pattern then you can apply test for a stuck at 1 fault. Similarly, we have to find out patterns and repeat it for all the nets here all the nets here and all the nets here, so this is actually called test pattern generation which we will slowly see.

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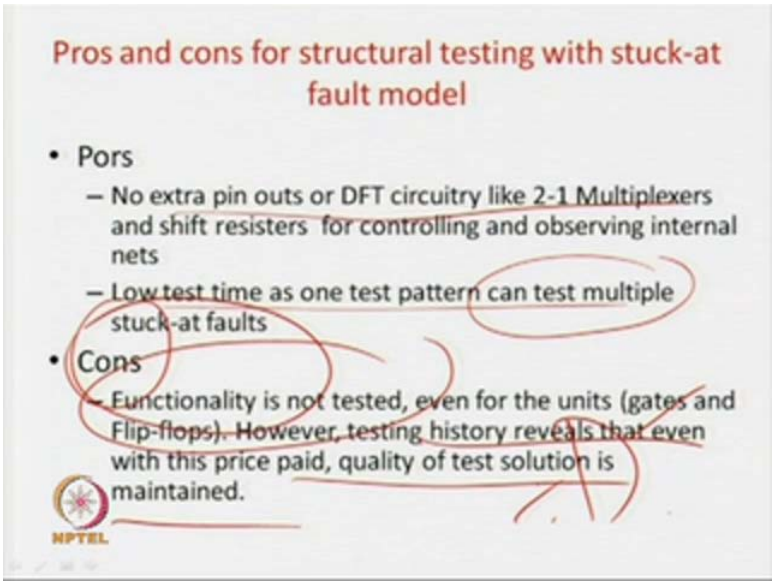

So, what are pros and cons with structural fault model, the pros are we do not require any extra test pin or any extra multiplexer or any extra stuff like registers, etcetera multiplexers pin outs etcetera to do the testing. So, we are able to find out that there is no stuck at fault just by giving some inputs and test time is very low, because we will see how we this things we will see later the test time will be lower because in one test pattern you can test multiple stuck at fault.

Those that things will slowly come into picture and what is the cons what is the disadvantage, the disadvantage is that functionality is no longer tested, AND gate you are not testing you are just verifying whether there is no stuck at error stuck at fault are there or not. But, still history has told that even if this functionality is not tested even at the unit level still the test quality is guaranteed to a very, very high level.

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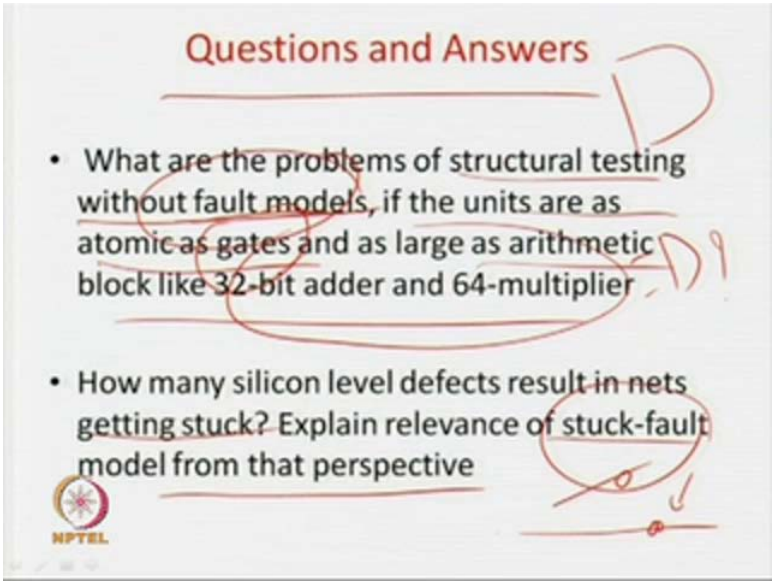

So, that is why a, what do you call structural testing with fault models is widely accepted, so before we finish our lecture today, so we will go for the question and answers, so we will be putting the questions today. And in the next lecture maybe or just before we go to the modification of what we have finished today, we will go for the answers of the question. So, what is the questions the first question we should be answered is that what are the problems of structural testing without fault models.

So, we have seen that the structural can be testing can be done with fault models and without fault models, with fault models what is the advantages no requirement of extra pins, no requirement of multiplexers, no requirement of what do you called flops and sorry resistors and all those things are not required. But that is, but if you have finished with that is with fault models and so the question we are asking is what is the problem of structural testing without fault models, which I have said if the units are gates as well as the units are larger.

So, one thing you can say about this we require a large number of flip flops we require large number of resistors we require large number of extra pin outs, but you have to answer what is the impact without fault models means you require lot of extra arrangement like pin outs. And I told you gates I am sorry resistors pin outs, then you require 2 is to 1 multiplexers then you require what do you call resistors and so forth, if you are do with with if you are doing without fault models.

Now, if the units are gates what is the impact and if the units are very, very large then what is the problem, so we have to think of the answer in this way we all know that this extra stuff will be required if you are doing without fault models. But, what is the impact if we consider gate as the block and if you consider adder or half full adders half adders as the as the blocks then what is the impact, so that we have to see. The second question is that we have found a structural testing with fault model is very good.

Then, but is this really happens that the nets really gets stuck at 0 and stuck at one as neat as that or as simple as that, if it is not, so then why is single stuck at model, so relevant that we can do the whole amount of testing. And we can assure that functionality is tested structurality is tested, I mean we should not say that functionality is tested we say that we can say that 99.9 percent, you can be sure that if there is no stuck at fault in the circuit then the 99.9 percent tested accurate to be functionally correct and so forth.

That is the huge accuracy you are getting, so how is it possible and why is it, so because this the question is this nets in the circuit do not really have such a neat stuck at 0 and stuck at 1 fault. Because, in the real world there are defects like the net may be torn the net may have become thinner and so forth, but still why is then stuck at fault model if really it is not happening at the level then why is stuck at fault model, so relevant. So, these are the two questions you are putting into picture, so you have you can go through the lectures and then think over and in the next lecture before we starting with we will go for the answers.

Thank you.