Design Verification and Test of Digital VLSI Designs
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Module - 7
Lecture - 1
Introduction to Digital VLSI Testing

Hello students, welcome to the NPTEL video course on Digital Verification and Test of Digital VLSI circuits. As you know the course has three modules, so design verification and test, as of now we have already discussed in details the design phase and the verification phase of the VLSI circuits. So now, we are going to the third module that is on the test of VLSI circuits.

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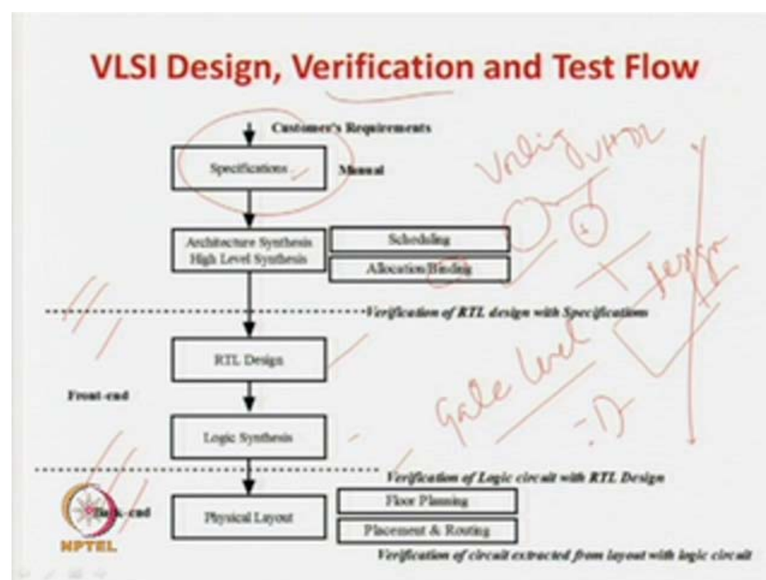

So, as we have already discussed in the first module that we start with, when which go for digital VLSI design, we start with what do you call is the specification of a circuit or specification of a design. Like for example, we have seen very detailed or descripted specifications like, how to design a control flow, how to design a adder or as simplest how to design an adder, have all as complex as how to design a control flow of a complex a mechanical system etcetera and then we write, we have seen that we have we write this stuff in some kind of a very simple user language or all which is not a technical language.

Then we have seen that it can be coded in form of something call verilog or VHDL very log or VHDL some language, we write down the specifications. And then what we have to do is that we have to go for a architectural synthesis, that is schedule, scheduling allocation and binding. That in case, we say that for a given specification to be realized, how we can optimally schedule, schedule the operators required in the given times steps. And then we have seen that how individual operators or that is the hardware operators are binded and allocated to this operation.

So, this was the high level synthesis part, which we have already discussed in details. In module in phase 1, of the course, which is on design. Following that we have seen that given a RTL design that is a Registered Transfer Level design, we go for a RTL synthesis and r t RTL and logic synthesis, that is a RTL design and logic synthesis. In this case we go finally, we get here is a gate level, Boolean gate level design of the circuit.

So, this first part as we have already told is called the design part or the fountain part of very VLSI design. Following that we go for for then placement and routing that is the back end part of the design, which we have not discussed in this course. This first phase of the design, this is the this call the VLSI design part, which is actually which is the module 1 of the course has already been discussed and after that in module 2, which was the verification part of the scours.

We have seen that, from one phase to another phase, like from specification to architecture design, from architecture design to RTL and then from RTL when we go for logic synthesis, there is we get the gate level design. So, for this same specification, we get different form of representation, like in this case we can get a control and data flow graph kind of a stuff, for where we get the after the logic synthesis step what do we get, we get is the Boolean gate level circuit. In this case what we get, we get some kind of what do you see, is that operators in some logical what do you call the time steps we have seen.

So, same specification like addition, control or something we have different representation. So, every step has to be verified that it is equivalent to the previous specification that is finally, when we have all circuit realize, it should be equivalent to the specification we have been given. So, every steps should be equivalent to the

previous step. So, this part was call the verification step of VLSI design. So, this part has also been discuss in detail in module 2 of our course.

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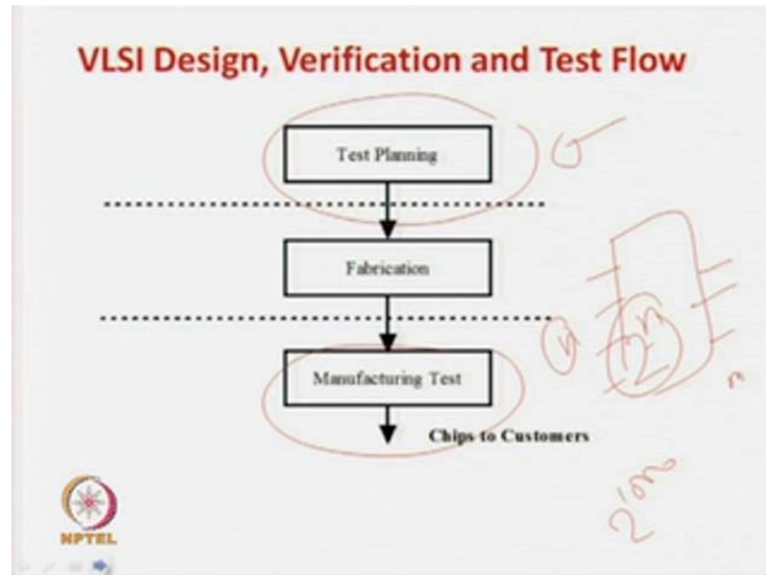

After that we have seen, also discussed in brief in very few initial lectures that, after the circuit has been designed. So, it has to be tested that is, it should the hardware's after the fabrication we get the hardware of the circuit that is the, chip or what you call the package chip or the vapor. Now, we have to verify that whatever you are shipping to the customer, is electrically correct that is whatever input signals you given the outputs you obtained, should be as per what do you called is the specification that we have required.

So, that is actually call the manufacturing test, there is one of the circuit has been design or un fabricated it should, electrically meat these specifications. So, and what is the test, that is actually the manufacturing test, but as you know that VLSI circuits are very complex. And a circuit with having say input of n input, if a circuit has around n inputs, n around say, m outputs then to find out that weather the circuit is matching electrically all the parameters of the specification or all the specification, we have mentioned in our requirement, then we required order of 2 to the power of n input vectors or 2 the power n input combinations has to be checked.

But, as you know if n is 1000 then 2 to the power 1000 is an prohibitive number to be tested. So, we have to go for an optimal test or what do you call, a test should be such that we apply much less number of vectors than 2 to the power n or a very less number of

input cases you can apply. And then you have to say, confidently that the circuit is working perfectly up to a extent and the extent should be around say 99.9 percent accurate, you have to tell that this circuit is operating 5 and with the much less number of test vectors then 2 to the power n.

So, that, for that we require a very detail test planning that how you can achieve this. So, this part is actually call the test planning. So, in this course, in the third phase of the course that is on VLSI testing, would be mainly discussing how test plans are made and how you can get a very good coverage that is you can get about 99.9 percent plus accuracy, with a minimal number of test cases you can apply. So, this is basically what you are going to study in this module.

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Introduction to Philosophy of Testing

- "If anything can go wrong, it will"--A very well known statement known as Murphy's Law.
- **Testing** a system comprises subjecting it to inputs and checking its outputs to verify whether it behaves as per the specifications targeted during design.

So, let us go ahead so, what is the philosophy of testing. So, is a very well known Murphy's law, it says that if anything can go wrong it will; that means, if there is a probability that a system can fail, defiantly it will fail there is a very high chance of fail. And our life, as test engineers we should be able to find out that, which is the cheap or which is the system that is not working properly that has to be discarded and whichever is working properly that can be shift to the customer.

So, testing if you take a very simple dictionary meaning, then is says that testing a system comprises subjecting the system, to inputs and checking that the outputs and check the outputs and verify that, the outputs are as per the specification targeted during

the design. So, in other words, what do you mean by testing so, you have the system, then you apply some inputs and you get some outputs, these are the inputs and you get some outputs.

Now, this output should be as per the design design specification which you have told and, so the this is actually the output response which has to be matched. Now, the question comes what inputs I will give. So, if you are given an enough time and you have infinite amount of time available for testing. So, you can apply, as in as large number of inputs as possible and your confidents on your testing will rise, but in a practical say practical scenario, the number of inputs to be apply during testing will be much less because, of the time constraints and there are several of other constraints which will study in this course.

So, our main goal is that you have to apply as no number of inputs as possible, to meet the constraint and your output should be matching this specification. So, what do call the your output, should match specification as largest say around more than 99 percent plus, as slow as possibly it may be 100 percent you have to reach that. So, you should show that your outputs are matching the specifications to that extent.

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Example: Electrical Iron

- Plug it in 220V AC and see if is heating.
  - "functional" specification, *that also partially*.
- Safety:
  - All exposed metal parts of the iron are grounded
  - Auto-off on overheating
- Detailed Functionality
  - Heating when powered ON.
  - Glowing of LED to indicate power ON.
  - Temperature matching with specification for different ranges that can be set using the regulator (e.g., woolen, silk, cotton etc.)

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So, our output, our goal is to take the outputs to a level that you can say confidently with a very high confidence that, outputs are matching all the specification and at the same

time you have to apply as less number of inputs as possible. So, this is the resting philosophy.

So, coming to the next thing. So, before we go for VLSI, VLSI or a or circuit kind of testing, let us start with an very simple example, of an electrical iron or a classical system. So, what do you mean by testical, electrical iron, if I asked to a lei man. So, here she can say that, you just plug in your iron to a 220 volts AC and seeing that heating is there. So, for in this is this is a testing and in fact, when you technical terms, this is also a proper kind of test because, our input specification for a heater is for a electrical iron is that, you plug in it will be heating and then you go on for ironing.

So, this is also a proper kind of testing. So, and the technical name of this test is call, this is actually the functional specification and, so we are actually testing it functionally. Now, let us see what more or how indicated testing is you can also understand from this example. So, this is a functional test and this is also partial, but now as you know that electrical appliances, like electrical iron, there is a lot of safety features that should be presented, that is all the exposed parts of the heat iron, should be grounded.

So, that there is no shout circuit. Secondly, there are many others and just listing 2 or 3. So, for example, if I just put the iron all and then I forget it for some reason, then after a certain amount of temperature you should go on for auto off mode. So, there are some other specifications that are coming into picture that are not that much related to functionality, that are related to safety part of the specifications of the electrical iron. So, you can see that, slowly the number of testing or number of test as requires, required to verify that your system is operating properly is increasing.

So, this is another part is the safety. So, you have to find out that weather everything is grounded and you have to subject your heat a iron to sum over temp overheating and then find out whether that it is a getting automatically switched off or not, following that if I go to a bits sophisticated electrical iron, which we can always see, which we are now a day’s which are available, then you can see that it as a laid.

So, when you put the electrical iron on, so the when the heating is going on. So, a laid gloss and whenever it the some some threshold temperature is reached, this thermo step which as the detected threshold as been reached. So, it switched off the heat, I mean a heating of the electrical and for some time and then, there is the LED glow glow LED

becomes off, hence it it goes on in this round. So, along with that also you have to test, if I am going for detail functionality test. So, I have to also see that, the laid is properly working or not that whenever the heater is on, it is heating then the led should be power down.

Whenever this specification it is reaching that from for example, around say some degree of degree centigrade reach the heating is off, then the LED should be powering LED should be off and, so for. So, this is another path of the testing for example, electrical iron has (( )) have a thermostat, as you might have see and there is something call, silk I think you might have see, ,then there is a call cotton. So, for all this thinks you can have different temperatures and if have different temperatures, then the thermostat what is accordingly.

That is, so if the if you are have set for the say cotton kind of a cloth, than if the temperature is a say around 80 degrees centigrade or something like that, then it goes about then it is switches off and when this for silk, the threshold will be different. So, you have to now you have to if you have to go for that elaborate kind of testing. So, you have to you have to said the regulated to woolen, silk, cotton, etcetera and then again I have to see, whether all the all these functionality, like auto cutoff, then LED glowing etcetera has to be again tested.

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Example: Electrical Iron

- Performance
  - Power consumption as per the specifications
  - Time required to reach the desired temperature when range is changed using the regulator

Tests for ONLY *electrical parameters*.

- Tests for *mechanical parameters*, like maximum height from which there is resistance to breaking of plastic parts if dropped on a tiled floor etc.
- Number of tests performed depends on the time, equipments etc. which in turn is decided by the target price of the product.

So, in other words, what I am saying is that, amino for a very system, very simple system like electrical iron, in a it seems that testing can be as simple as plugging it on and see whether it is working, whether it is heating on not, but in fact, this is not the case because, whenever you go for a detail kind functional test. So, you can see, how elaborate testing becomes.

So, now, let us see. So, the previous slide, we discussed only about the functional it is of the circuit, like different thermo sets setting, like cotton and whether ladies glowing, whether heating etcetera, but they are some other performance which is done, which is not that much really went directly to an user, that is actually the performance. We say that, we say that the heater, we you say that now a days the electrical iron is 5 starts complain.

So, it says that the power consumption of the heater or the electrical iron is a, is such sense such. So, you have to also see the power consumption. So, that has also be reach then also some for some branded companies we say that, the temperature we that will be reached by the iron will to from, cotton setting or for some silks setting, it will be reached within that with x seconds or 10 seconds or something like that, that is the performance that my electrical iron is, so good that it consumes, so much power, so less power and it reaches are it desired temperature in such low, low amount of time.

So, this performance tastings are also very important. So, I mean in the more a testing you require the more time it will require and the test procedure will be become more and more complex, even for a very system classical, very simple system affect like a classical iron, but these are or some of the test, which were related to the electrical properties of a iron. So, you can see that the whole Pandora’s box is slowly opening up.

So, now, you can see that, there can be some mechanical parameters, like you can say that the plastic parts of the electrical iron are un makeable that is or it, it is resistant’s to breaking so, but on how much, from how much distance if I throw it or from how much distance is forced falls on a wooden flour or it falls on a tiles flour, what will be the braking whether there will be scratches and all. So, there are some kind of other test which we may also require to test mechanical parameters or something like that.

So, test becomes, so complex that, you have to have more time for this now now. So, now, the question is more I do a testing, better is my product and better I can advertise it.

So, why should I do a less amount of testing, philosophically testing all for a common person, we can say that we should test as much as possible that is true, if you go for a exhausted kind of testing like for electrical iron that I have discussed So, that do you can get, you can get a very good test. So, that you can say exactly about your arrows specification, when you are selling, but now what happens.

Now, say for example, you are manufacturing 10,000 electrical iron per day. So, testing all the parameters, as I have discussed may take even more than an hour or even more than that to say fine say that, my each electrical irons satisfy all these properties. So, now, for each heater you are spending around 1 hour for testing. So, you have to devote man hour, you have to devote electricity in your test plan and you have to also devote, so many other things. So, you are adding into cost.

So, now, actually decided by that, so everything is decided by the, target price of the product and some efficiency which will come later. So, you can say that, if I want to sale my electrical iron at 5000 rupees something like that, then you can go for the huge amount of this, but as you know in a practical market, these things should not survive because, a video a very good electrical iron now a day's come below 1000.

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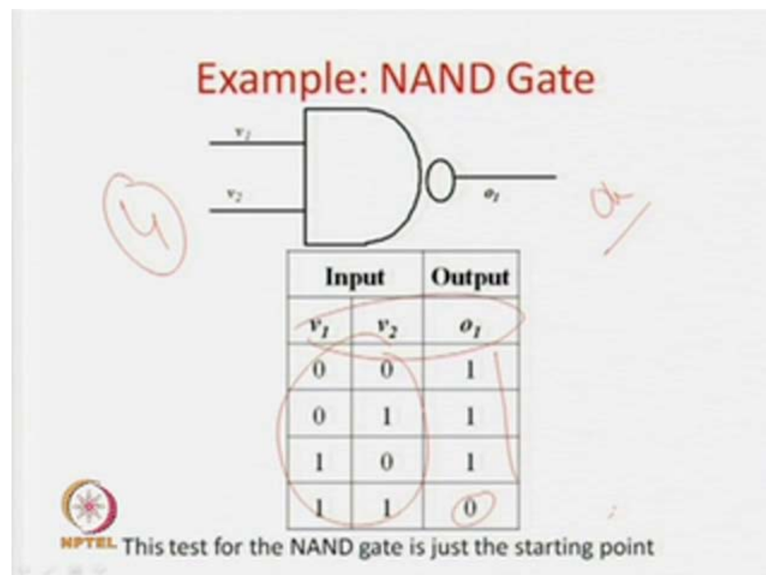

v_1	v_2	o_1
0	0	1
0	1	1
1	0	1
1	1	0

So, now, we have to decide that, I have to make profit in that 1000 or some x amount of money and at the same time I have to give a reasonably good amount of testing I have to do, so that I can also satisfy the customer. So, there is always a trade of between the

number of test perform, if you do a large number of tests then you can always go to a very ideal result, say that my heater or my whatever performs this, this, this, but at the same time it will increase the price of your design of your product. So, this always a trade of in between this. So, with is we started with a very simple classical example of electrical and because, of very well known to us.

Now, slowly we will go to our original course, which is our circuit. So, will star up with a very simple and NAND gate. So, this is your very simple NAND gate. So, now, again I need to test the and NAND gate. So, what with the very first, if I give to a person that you have to test a NAND gate. So, what he as to do, similarly like an electrical iron. So, you have just test the functionality. So, what were the test in electrical iron just plug it and test it.

So, in this case also I when go for a functionality test. So, you can see that I have 2 inputs and 1 output in this case. So, there can be 4 inputs in this case, there is 000110 and 11. So, these are the input cases. So, all the inputs I will give and then I will see whether the output in the first three cases should be 1 and if the input is 11 the answer is should be 0. So, if I find it, I know that the gate is I can say that the functionally.

So, but now you must be surprise to see that, this is just the very starting point of testing an NAND gate. So, now, just like heater a sorry just like our electrical iron, we will start opening what kind of tests are possible in the NAND gate.

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Detailed tests for the NAND gate

- Digital Functionality
  - Verify input/output of Table 1
- Delay Test
  - 0 to 1: time taken by the gate to rise from 0 to 1.
    - *v1=1, v2=1* changed to *v1=1, v2=0*; After this change in input, time taken by o_1 to change from 0 to 1.
    - *v1=1, v2=1* changed to *v1=0, v2=1*; After this change in input, time taken by o_1 to change from 0 to 1.
    - *v1=1, v2=1* changed to *v1=0, v2=0*; After this change in input, time taken by o_1 to change from 0 to 1.

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So, see. So, first is the digital functionality. So, it can be done, according to the table hour that we have already discussed, that is all all the 4 patterns 0001011 you given tested. Now, you see now this is a see a NAND gate. So, now, you have connected it to some kind of a circuit now, another very important part is the time. So, that is the delay. So, you might always have already discussed in the first two modules that, the circuit is working at exit guard, of this time or the time required by an operator. So, obeying operator like an, adder or a multiplier or some hardware is x and x nanoseconds or it is frequency is, so and so.

So, all these p will depend on the delay that is if some input I have save and if some outputs are I have save. So, what is the time delay of this gate. So, if this gate is having a very high time delay so; obviously, the whole circuit which will be which will be compose of. So, many smalls, smalls gates, will be also large and if you want to, go for a minimum delay or you have to increase the frequency or the performance in terms of the speed of your circuit. So, this gate should have a low or delay. So, that is delay is a very important parameter in case of circuits.

So, you know that functionality is fine now, if I what to shift my gate or if I am to say that I have manufacture this NAND gate and you want to sell it, another very important parameter is the testing that is actually called the delay test, like in the he liking electrical iron you can say that I am a very cheap iron kind of a thing. So, I can see that you just plug it into the electrical phase and it will, start heating that is the minimum there minimum test.

But, in case of a VLSI circuit like a NAND gate, digital functionality is 1 and then very important functionality which we have to do is that delay test because, unless you say that what is the time required by this gate, movement is going to accept the design because, when he is plugging in your gate into your circuit, we should also know that what is the amount of time, required by that gate to give the output, accordingly you can go for this design because, when is shipping is product it is digital functionality as well as, your performance in terms of speed is very important.

Like you might have heard that in case of when you all selling your Pentium processers or AMD processers or whatever you see that there are two things it is says that it is Pentium 3 or Pentium 4 or dual, course of that test that what is the basic functionality in

also it, it test that, what say 2 gigahertz it also a 1 gigahertz. So, what is that specify, that specify that the frequency of the circuit is, so much. So, they are very do important parameters which as to be tested.

So, now, how do you would go for a delay test. So, the delay test will be, like from 0 to 1. So, initially in the NAND gate, your this was the gate say. So, initially they output was as 0. Now, you have to make the output 1 for some because, of some inputs, like may be the input was in that case, say in this case it was input was 11 and now say input is 00 kind of a thing. So, the NAND gate output will rise.

Now, the question is how much time it will take to rise. So, this a actually, this is a very ideal scenarios. So, this gates are very ideal scenarios. So, now, you can say that that if you have given any input the stuff and then we tries in this, way this 0 delay kind of a thing is a very ideal ideal stuff, but generally, we will have a some delay liabilities. Now, I want to find out what will be this delay, with will be 1 nanosecond with will be 0.2 nanosecond and, so for.

So, I have to do now we can see how the complexity it will become. So, from 0 to 1 I have to test that is the rising of the output of the NAND gate. So, initially if you have I want to get a 0 over this I have to apply a 11. So, v equal to 1 v 1 equal to 1 v 2 equal to 1 now, you have to find out what is the time required to change the output from 1 to 0 sorry from 0 to 1. So, what is in NAND gate, output can be 0 only if v 1 equal to 1 and v 2 equal to 1, but output can be 1 in case of NAND gate in three cases v 1 1 v 2 0 v 2 1 v 1 0 v 2 1 and both are 0.

So, know what you have to do, in this NAND gate it is exhaustive we have to keep 11 here and then, the it will be 0 know we have apply the 0 1 over here and see how much time is requires for this 1 to go high, next you take a v 1 11 and then you apply v 1 v 1 equal to 0 and v 2 equal to 0 and see how much time is require for the change. As similarly v 11 and from 11 you change to 00 and then you see how much time is require to change.

And average you can till that, in the average case this is the time require for change from 0 to 1 in the NAND gate and also you can see, in the case of worst case may be from example from this one to this one the change required is, so much nanosecond.

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Detailed tests for the NAND gate

– 1 to 0: time taken by the gate to fall from 1 to 0.
  - v1=0, v2=0 changed to v1=1, v2=1; After this change in input, time taken by o_1 to change from 1 to 0.
  - v1=1, v2=0 changed to v1=1, v2=1; After this change in input, time taken by o_1 to change from 1 to 0.
  - v1=0, v2=1 changed to v1=1, v2=1; After this change in input, time taken by o_1 to change from 1 to 0.

- Fan-out capability:
  – Number of gates connected at o_1 which can be driven by the NAND gate.

4+6

So, this is the delay test on 0 to 1 know again you can also have to have a delay test from 1 to 0. So, you know that in a NAND gate, already discussed. So, we can have a out this is this this curve we are requiring, we require how much time is requires for this for this delay because, initially it was 1, know it was falling to 0 this delay, this psi equal to find out. So, initially how to I get a 0 in the NAND gate, you know that the answer has to be 11.

So, the all force should be 11 that how from where I can reach a 0, the answer is if the inputs are both 00 the answer is 1, this 1 and this also from this three input cases, if I go to this output cases I can get from 1 to 0 this fall is there, again you have to apply the 3 cases and you have to find out that, what is the a time delay that has been take in for this fall and then you can again represent that the delay from 1 to 0 fall is, so much in the worst case or in the average cases, so much.

So, this. So, know we have how many test till, now we have done, we have done 4 for this (( )) functionality and then, what you can say that now we are doing this delay test. So, we applying there are the 6 kind of a parameters, which you have or 6 kind of inputs 10 inputs till know we have given. So, this was about the functionality of the NAND gate in terms of logic as well as the delay.

Now, the another important thing, which you are some lets taking into picture this is your NAND gate I think you might also, have seen the fan-out case in our previous modules

that know this NAND gate can, drive or we should write similar other gates. Know the question can be ask that, how much gate or what is the drive capability of this fan-out or what is the fan-out capability or the right capability of this NAND gate.

So, I am not going into details of how the test can be done because, that is requires some complexity to perform this test, but again you have to till that. So, this gates can pretty will dies. So, many other gates with, so much load in, so much time. So, these about the fan-out capability test.

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Detailed tests for the NAND gate

- Power consumption of the gate
  - Static power: measurement of power when the output of the gate is not switching.
  - Dynamic power: measurement of power when the output of the gate switches from 0 to 1 and from 1 to 0.
- Threshold Level
  - Minimum voltage at input considered at logic 1
  - Maximum voltage at input considered at logic 0
  - Voltage at output for logic 1
  - Voltage at output for logic 0
- Test at extreme conditions
  - Performing the tests at temperatures (Low and High Extremes) as claimed in the specification document.

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Tests are for the "logic level" of the NAND gate.

Now, again if you look at the digital designs as I many times as I have told that we merely go for 3 stuffs in design. So, one is speed that is frequency, speed, power and delay. So, know. So, till know we have seen that this, what would you have to call the you have seen the delay and that is the delay that is the rise to 1 fall to 0. So, this delay parameter, we have tested and we have we can report it.

Another very important constraint, which is say is the power constraint that is actually coming in to prominent, know a days because, of the fact that we are using lot of hand held devices, like your mobile phones, laptop etcetera. So, many times we say that, our laptop on your processor is working at, so much frequency it is speed is, so much that is it is frequency and in at the same time, we also say that it is power and what is the power, of your said sorry the delay and speed at the same thing actually I made area.

So, will slow after afterward see come to area, there is what is the area taken by your stuff. So, the three parameters of designer area, delay that is same speed and power this is not this is not speed and delay at the same thing sorry for that. So, this area delay and power. So, delay we have already measured, then and we can perform the delay latest. Now, also you might have heard that we sometimes say that our processer, like an atom processer is a very low power processer or it consumes low power.

So, also we have to find out, what is the power required by your NAND gate that also you have to tell this is. So, if your and gate is very fast it is functionally verified, but it is a lot of amount of power. So, that may not be also good for your design. So, along with this delay test, also you have to go for a power consumption test. So, I am not go into details how the power consumption test are done as the many be pretty complex.

So, we generally measure two types of power, one is static power that is when the gate is not functioning still, there can be some power loss because, of leakage and there something called dynamic power that when is your circuit is switching from 0 to 1 and 1 to 0. So, there will be also some kind of a power as it is the dynamic power. So, we have to measure those power. Then you can say that, the power of my circuit is this much, delay of my circuit is, so much functionally it is correct, in area we can measure from the a design path.

So, that is when we have do done designed your circuit, then you have done back in that is you have done layout and fabrication has been there then you can also report your area. So, area we generate do not cover under testing, but you can (( )) report this is the area. So, minimum these 3 parameters, we give and this thing we generally can verify from your test results and say that your NAND gate is such and such. So, these are your around, you can say that logic Boolean functionality of kind of a thing.

Know, that is depending on your functionality and all those thing. Now, another important thing, we always say that. So, slowly you can I am telling you that two test are basic NAND gate, how much satisfaction it is. So, that is how, we also started with a very simple example of an iron and then we saw that, how how what what are required to be tested in that iron, to get very good amount of what you call test results or very good amount of confidence, same thing we are doing for a electric for a for a VLSI circuit like a NAND gate and then will do the comparison to give you the philosophy.

So, now, what another testing that is required, we say that logic 0 and logic 1, this is the nothing call logic 0 or logic 1, there is some voltage that corresponds logic 0 and there is some voltage that corresponds to logic 1. Generally, we can say that, if it is a say some some kind of circuit may 5 volts is considered as a upper tactual and say 0 we considered as 0 we considered as the 0 volt we considered as lower tactual and we can say that, if anything is around above 4.8 volts and to say 5.2 volts or something. So, we call it a logic 1.

And logic 0 we can say that, if the voltage is a up to say 0.3 volts or something we said that a logic 0. So, this specification I say that, if I get something less than 0.3 volts or bellow I call it logic 0 and from 4.8 volts to 5.2 volts I concentrate logic 1. Now, again all the tests I have done for 0 and 1's I have to apply these all the inputs in case of NAND gate in the table 1 as you already see that we apply 000110 and 11 and then we get the answer say 111 and then we sorry we get 111 and after this some pattern we get the answer 0.

Now, for each we have to measure what is the voltage, like for all the once your voltage level should be within 4.8 volts to 5.8 volts and for 0 volt it should be within say 0.3. So, now, you have to measure all these things using analog techniques because, digitally we cannot measure volts kind of a stars and then you have to find out that this, all the voltages at the logic 0 and logic 1 and everything is making, meeting.

So, your logic 0 and logic 1 that comfortable with the input voltage ranges. Now, again now, you know that circuit can be subjected to and the set of test. So, it can be subjected to very extreme conditions, like it can be subjected your we say that your VLSI circuit or your devices or whatever, will what properly say for examples from say take 5 degree centigrade to around say 6 degree centigrade kind of thing, usually write that.

So, your device will work properly within, so and so simple it, is the military grade equipment, we say that it operates from minus 60 degree centigrade kind of a staff, say just an example, may not be correct, but say from some x, minus x degree centigrade to some plus x degree centigrade. So, all the test which I have done, know I have to be done for extremes low and high extremes, which is actually came in the specification document, say if it is temperature you have to do all the operations such an high

temperature and also, if you have the some specification it can work at, so much pressure of the mercury and, so for.

So, all the test we have done have to be also verified at this high extreme extreme test conditions will be apply and then only we can said that your NAND gate is actually, operating and this or it is satisfying it is satisfying all the conditions which is required in the specification document, as well as it is, it all the things all your and NAND gate will operate, functionally correct and with all the parameter make test parameters like power consumption, threshold, delay, etcetera within, so and, so degree of temperature and, so and, so degree of pressure.

So, now, you can understand the complexity that is for a simply NAND gate with two inputs, how what is the amount of test I have to do, to assure that it works at, so and, so frequency it operates at, so much and, so delay it takes, what you call this amount of power and this is the voltage levels and it operates at this and this. So, all the things I have to do pass into the NAND gate. So, you can understand the complexity of testing a circuit.

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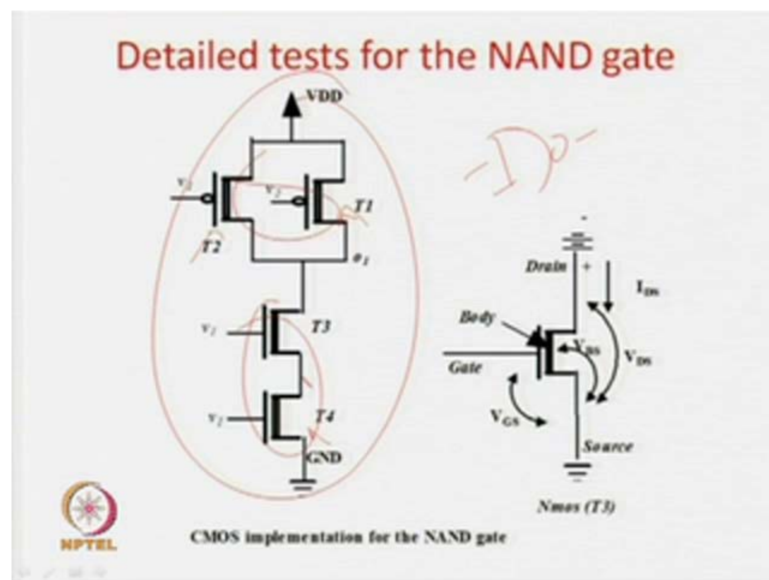

To assure that so assure that it is operating properly. So, this till now we were talking about the NAND gate, only from the logic level point of view that it is a digital NAND gate, but actually if you look at the NAND gate from internal. So, it is not a simple NAND gate, is not a just like a digital stuff you understand, inside it will look like this, it

has to p mass transistor, it has to n mass transistor it is connected in this way. Know, if you want to say that your NAND gate operates properly, sometimes we have to go for a detailed test of this transistors and then only we can say this four transistors operating properly.

So, we can guarantee much better tests or much better a specification coverage for the NAND gate. So, I will not go into very details of how the tests of this (( )) are done because, they are they are part of analog testing and just to give you an idea.

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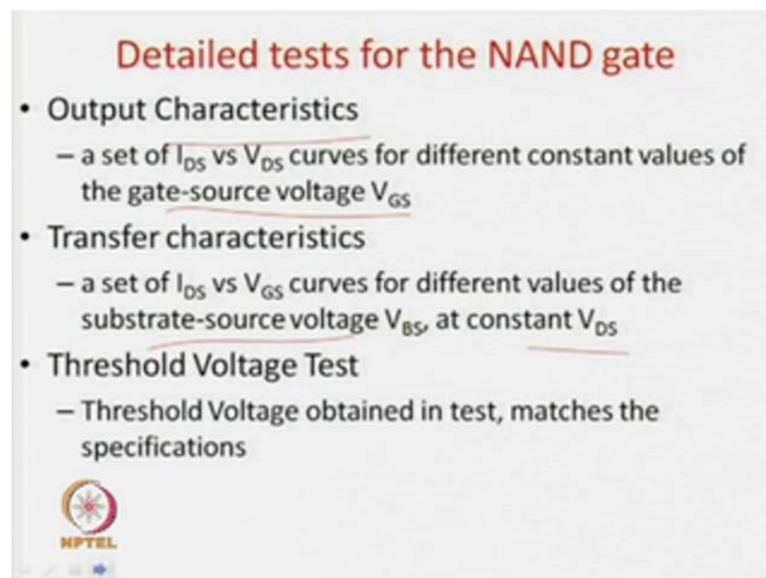

So, you can see you have to find out the output characteristics of all the transistors, like a set of input current, but the input voltage current, for different values of volt to drain sources and also there can be trance again, some threshold volt test for this transistors, also there is some substrate source voltages for constants VDS. So, they did not going to details, but for each of the transistors, like this we are testing, what is the voltage and what is the this current, what is this voltage at constant this one and, so for.

So, some of the parameters will giving constants and you are starting the voltage, versus the current for this table, thing and all the transistors we are doing that and then we are reporting the results. So, more depth we go, more amount of test are coming into picture for NAND gate.

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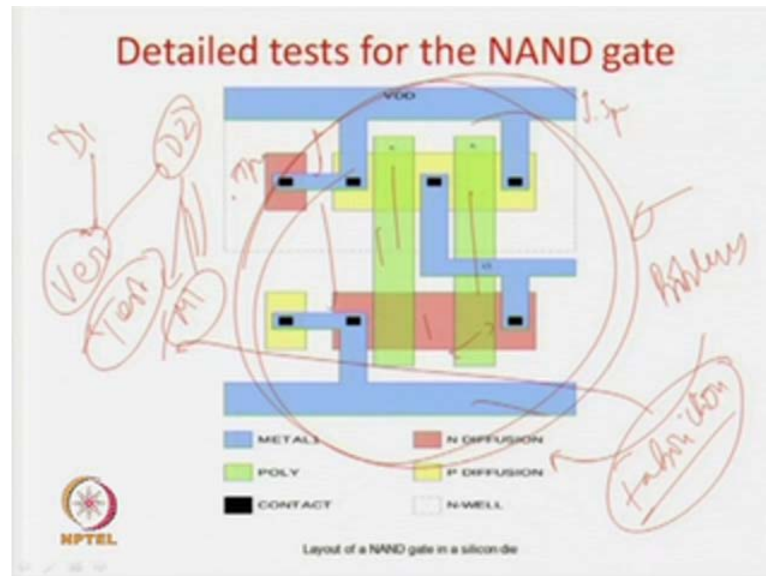

So, that was about the transistor level design, but know our transistor is design the transistor is very well laying on the transistor in a physical backing or in a VLSI circuit. So, your one single gate, NAND gate generally looks like this. So, this is your metal. So, this is your and diffusion, this is your poly. So, these are physical layout of your circuit. Now, if I want to test this, things will become much more complex and the device equator now, you have to have a electron micro scope kind of a thing.

Because, now I say that, what the NAND gate I said this this specification is a find 0.5 micron. So, if this much more than that, then I can said that it as form as specification, we can also say that, the distance between, say these two metals should be say 0.7 micron some specification. Now, after this has been laid out now, you can go for a very complex micro scope or there several other very complex state, next to find out whether, whatever was your minimum requirement for this kind of a NAND gate, it has been properly laid out.

Because, laying out a circuit or fabricate fabricating is circuit also observe very complex procedural. So, we do not know that after the fabrication because, all the faults in your circuits as we told is, so is looking in this series of lectures on testing, mainly happens because, there are some from what you can call, that is problems, some problems in this fabrication that is the main thing. So, if I tell you, what is difference between verification and test. So, verification and test.

So, in verification what do you verify, you verify that I wanted to design a adder. So, whether if I have really written a code that actually I have the adder. So, that is what I verify is that it is functionally, what I intended to design, what I have designed or not. So, if there is any failure in the verification case, then you can be sure that it has happened because, it was the designer mistake, but when we say that testing.

So, what does testing verify, the testing verify that I have I have made design say D 1, I have verified it see if I verified it; that means, all my mistakes are been taken care of and now I am getting a design D 2 say, which is functionally correct; that means, whatever code I have written that actually implement this specification. Now, this D 2 will be manufactured and say a manufacture you say a chip I get is manufacture say is M 1. So, what is the manufactured chip look like, for the NAND gate it will be basically looking like this in a die.

So, know this fabrication process of the manufacture process have lot of imperfections. So, we slowly see why they are. So, because, of this imperfections, this M 1 may not be equivalent to your D 2. So, testing proceed your basically test, whether there has been any problem in the manufacturing step that we are M 1 is not becoming equivalent to D 2.

So, that is why to lay speaking we have to find out whether this has been properly laid out, this has been properly laid out, whether this thickness is proper and not and the test equipments and the test timer a numerously a numerously an it should be exceptionally high, if you are going for a test at this level. So, what we have seen is that, basically we this layout of a NAND gate, then we have see the transistor level of a NAND gate, then you have seen that electrical parameters of NAND gate, like delay power and then simply the functionality of a NAND gate, like 0001011 kind of test.

So, more in depth you go, the more number of test you have to do for VLSI circuit as indicates our critical system and you can understand that a modern typical processer, has a millions of two input NAND gate.

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Optimal Quality of Test

- Given a digital logic gate, what tests are to be performed to assure an acceptable quality of product at reasonable price".
- Test for the NAND gate should be such that results are accurate (say 99% above) yet time for testing is low (less than a millisecond).
  - Table 1 for the NAND gate and at proper time
- DIGITAL TESTING is not testing digital circuits (comprised of logic gates).

DIGITAL TESTING is defined as testing a digital circuit to verify that it performs the specified logic functions and in proper time.

So, you can understand that what is the complexity of testing. So, what is the basic idea, our idea of testing as I already repeated that in case of the NAND gate or for whatever circuits, that your accuracy should be very, very high more than the 99 percent and your testing should be very, very low, see even less than a mile second because, they told a circuit may have millions of gates.

And if you start test taking 1 to 1 or even 1 or 2 second for 1 chip. So, 1 circuit will take 1 million seconds to do it, which made an in to days and we know that for a single design we fabricate millions of circuits and we sell in the market. So, your test procedure will run into 100's of year. So, that is not possible. So, what we have to do, we have to have as high as 99 percent accuracy and we have to test to be less than a millisecond.

So, why digital testing procedure or digital test planning is how can we achieve this matching. So, will in this course will see that. So, know, if I say about digital testing is not say that. So, if you say me, ask me what is digital testing. So, from a lay man point of view or from a (( )) non experience in testing, we will see that digital testing is testing digital circuit, but it to be more precise, it is not testing the digital circuit because, digital circuit testing, we have seen such a complex case of NAND gate.

So, you have to go for functional testing, speed testing, delay testing, power testing threshold and then for the lay out. So, that is very complex. So, if in if I start doing this I will take even more than 1 hour to test a circuit and for 1 gate and a circuit will be in this

and for 1 million circuit will be used, it will be years. So, basically I do not have a time for a such a sophisticated thing.

So, basically digital testing is defined testing a digital circuit to verify that it performs the specified logical functions and in proper time that is I am not much bothered, whether it is taking, whether the layout is proper or not or whether it is the some issues in the poly or some stuff. So, basic this is actually we should solve the basic because, more on if you become which you call it sophisticated digital testing or advanced digital testing.

Then it will become more complex, the various digit the various digital testing is that I want to know, that in my digital NAND gate is performing proper in case of 00011011 and it has it has to give you the results in proper time. If this is done more or less where basic digital testing is over. So, digital stuff circuit is not about testing the digital circuit entirely, which you have seen in the last few slides, but this basically this much, these are basic testing, but if we want to go for advanced testing. So, all these things will come into picture.

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VLSI circuit testing Versus Classical System Testing

VLSI Testing	Classical Systems
Technology matures and faults tend to decrease, a new technology based on lower sub-micron devices evolves	Basic technology is matured and well tested
Diagnosed and repaired	Binned as defective and scrapped (i.e., not repaired)
Yield is Low	Yield is almost 100%
Expensive equipments and Specialized Manpower	Simple Test Setups and Technicians
All Samples to be tested	Random Sample Testing
Test arrangements in design	Rarely Required

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So, now so now we have seen about two, what you call two systems, one was the classical system of the iron and one was the gate. Now, let us just have a very quick look at, what is this, what is the basic difference or basic similarity in between this. So, in case of classical systems, we never go on for a very complex testing like a electrical iron which I had mentioned, we generally do a very preliminary test and then your satisfy.

Now, now why, but the some circuits we have to do do it, we have to exhaustively test all these circuits I already much more complex there are (( )) why is it, so. Because, in case of electrical system the technology very well matured that we all know how to design a electrical iron and the it is and the techniques is remaining similar, for last say 30 to 40 year prescribed modification. So, whatever you produce, are more or less guaranty to the or working file. So, have random testing kind of a thing with the few samples is fine, but in case of circuit now, we have a technology say 0.5 micro on technology.

So, we are having lot of problems with a technology manufacturing is not proper, then we quickly go for, we are having lot of issues or some tests are failing, but still we are going for 0.5 micron technology, but due to market pressure, some other companies say come up with 0.25 micron technology. So, even before 0.5 micron has matured and there is very little scope for errors and new technologies coming into the market because, you are going to get better performance in those, in the lower some micron then (( )) quickly moving to new technologies.

So, even the for a technology matured and faults tend to decrease that is, technology has matured it is stabilized we go on, for new and a new a technology. So, always test falls are a numerous in numbers and testing is a either prominent thing that has to be done, but in case of, in case of classical systems. So, this the other way of, see and then important I will go, this part I will come I will come to later, this is will slowly will move to this course and then we will come in the end. So, another thing is yield.

So, now in case of classical systems, we say that yield is almost 100 percent, then if I make 1000 electrical irons you can now that say around 99 will be operating file or may be all 100's will, can we sold with little repairing, but in case of circuit idea is not that because, the technology is always maturing, say yield is even low as well as 50 percent that I made 100 chips, 50 I have to have to through them of, only 50 will survive.

Then that is why if such a high amount of failures are there. So, you have to go on, for testing is an every part because, if I miss then is a very high probability that I can shift you or the customer a faulty chip, but still how the VLSI will make profit because, they can sell it in a slightly higher price, but that is not the issue, but I always have to be, as per the markets that is if I have a very nice NOKIA mobile phone or a very nice

Motorola phone I will go for that these are that a very old kind of a phone because, always the technologies maturing in case of the VLSI and we are getting newer or newer gadgets.

So, I can slightly go pay higher price is get a very good gadget that is what is the or a very good performance. So, that is why we are going towards newer a newer technology even if there are errors or if there are faults. So, that 50 percent of a circuit I am ready to throw out, but still I have to catch up with the markets of the latest trends. So, with the high number of faults. So, that is why testing is, so important.

Secondly, in case of classical system, tests are very simple, just you plug it on or even a simple technician can do your test, but if in case of, this electrical what is VLSI circuits as a seen for the NAND gate, it is a very tough process, you can see that you can require microscopes sometimes you required to major voltages something that have to add terms. So, very expensive equipments are required for this one and test arrangements, I will tell you. So, next is, so this arrange a examples.

So, as I told you that in case yield is almost 100 percent. So, almost all the circuits are operating fine. So, you require as less as say around, say one are two random samples you can test and fine, but in case of the circuits, all these gates has to be tested. So, because, the number of what do you call the, number of faults can be very high as high as 50 percent of the circuits may have fault. So, all samples has to be tested. So, that is why each and each every unit has to be tested in case of circuits, while in case of classical system like iron or heater or something.

So, as he number of false are very less. So, you can even take 3 or 4 random samples and you can do it. So, So, now, I will slowly see in this circuits basically about these two parts, this is not very I mean you cannot explain this initial lecture that is, in case of circuits we generally do not go for repair and in case of classical systems, if we find some repair, we can a if you find out some that some of the electrical arrow, some system have a fault.

So, we generally go for repairing then we sell it sell it in the picture, but in this kind of in the VLSI circuits, test arrangements I mean basically it is not required, we have something, we tested and then we find out that there is problems in case of the VLSI

testing circuits is not performing finally, we generally then through them out, that we do not believe in, what do you call repairing and all those things.

So, this is basic from difference in the VLSI testing, as compare to a classical testing, but some of the things like test arrangements in the design and test do not have such type of stuff, in case of classical systems, we slowly see this points, like billing and defective, non repairing. So, these parts will slowly see when will going to the other parts of your mean. So, will go progress through the course, you will see.

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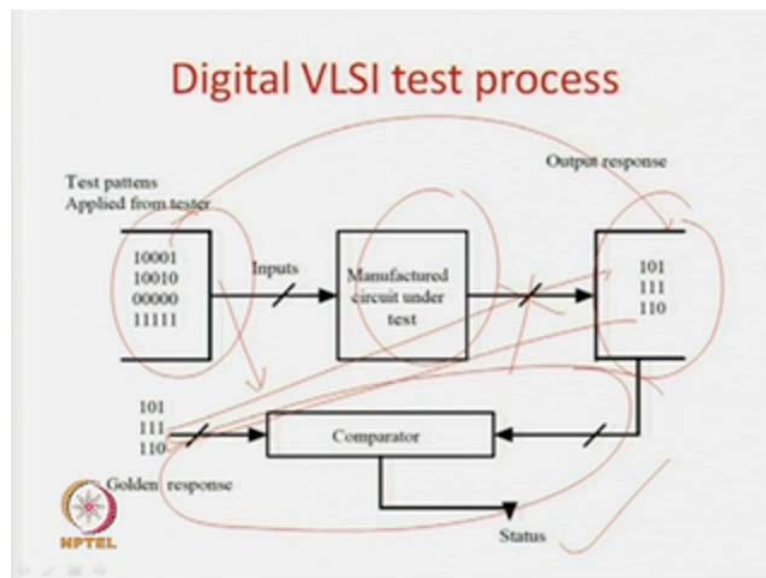

So, basic difference in case of a normal testing, many classical testing as well as the system VLSI testing is that, classical testing all most all the products are correct. So, random testing we do and very simple kind of test. So, even a technicians can do, but in case of VLSI around say 40 to 50 percent or even more than that circuit can have defect. So, you have to have, all the circuit tested and test procedure is quite expensive. So, you have to have really sophisticated instruments and engineers to do that.

So, that is the very basic difference between normal's classical testing, as well as system testing. So, compared to classical systems VLSI in VLSI testing in occupies a very, very important parameters. So, therefore, in our course, we have kept one third module only for testing. So, let us slowly going to the course, a basic introduction. So, in case of circuit; so what will have, we have a manufactured circuit we give the inputs.

Now, this inputs I have told you should as less in number as possible, then there is a golden response that is we know that for this input this should be output, then there is a comparator. So, it compares' this output with the golden response and if all the response are matched, we said that the circuit is operating fine and also we also major the delay in this case of requirements.

So, if this is the process, then we said the circuit is correct otherwise, if there is some mismatched between this and this, then we said that there is a fault and the circuit can be scraped or there is I mean it can be declared as a faulty circuit. So, there is the basic digital test process.

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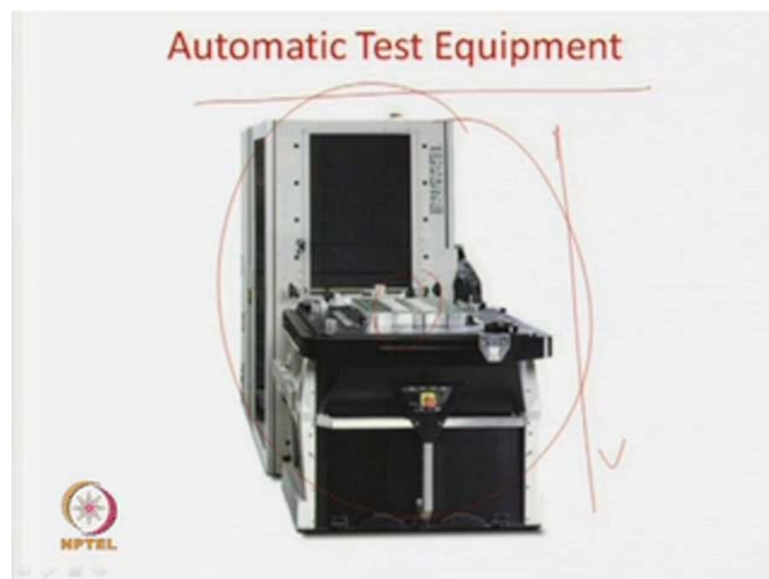

So, this is and equipment atom now, I have told to that I have to do the testing of power delay, so and, so. So, basically what are the test equipments do clay, this is a automatic test equipment, we call it in 80. So, this the test equipment here, we put this circuit in a die in this case and this big equipment as oscilloscope, CRO's, pattern generator, the logic analyzer and they do most of the distinct for it. So, this is the automatic test equipment and is a extremely, expensive equipment and very, very big companies can only offered this instrument that you have to be understand.

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Taxonomy of Digital Testing

Criterion	Attributes of testing method	Terminology
When tested?	1. Once after manufacture 2. Once before startup of circuit 3. Always during the system operation	1. Manufacturing Test 2. Built in self test (BIST) 3. On-line testing (OLT)
Where is the source of Test patterns?	1. An external tester 2. Within the chip 3. No patters applied, only monitoring	1. Automatic Test Equipment (ATE) based testing 2. BIST 3. OLT

So, now a, they have we before we go in more details, let us see what are the taxonomy of testing that, what are the different types of testing that is available in the market. So, first question is when tested that is the criteria, when you want to test the circuit. So, if you just do it before the manufacture, then is call the manufacturing test, also after the circuit as been manufacture and it as been sold in the market. Now, it is in your laptop or in your pomp top or your PDA that of at that time also you can have faults.

So, before the circuits starts it is operation, I can always have my circuit test that is like in your PC, whenever you start your PC it shows that the RAM is being tested and if you all the RAM is fine, if gives an and then a circuit course. So, therefore, many of the circuits are tested, every time before the circuit stat that is actually call built in self test, that is circuit test itself when the circuit is starting in operation and for very mission critical systems like, nuclear plant or airlines flights or rockets you can understand that the circuits should also be tested every time or concurringly when it is doing is operation.

That circuit is operating and the same time you have to say that, you have to test itself. So, that is actually fault or else that is every time the circuit is all the time circuit is operating, a person is monitoring it for it operation. So, these things are formation critical applications like, have your needs, nuclear plants etcetera. So, this is call online testing, the circuit is operating as well as the same time, you are testing the circuits. So, when the circuit is testing, these are the basic term on your logic.

Now, the question can be ask, who apply the test patterns, like we have seen for the NAND gate 000110 and 11 and the question can be ask, who is applying the test patterns. So, if it is the manufacturing test the 80 example I have shown you. So, that is an 80 is as equipment. So, if the equipment apply the test pattern, we call it the ate based testing, line now in a BIST. So, a what is he BIST, BIST is Built In Self Test.

So, in this case what happens, the circuit is a doing it is operation is, staring is operation before that we are applying some test patterns and we are getting a response. Now, if I manufacturer a circuit and I put it in your laptop; obviously, you cannot bring the ATE machine and test your circuits. So, in that case, the test pattern generator and the test pattern and response analyzer are within your circuit.

So, this a we will slowly seeing it was the end of the course we will see how it is done, for equipment is simple, you applying the pattern you observe the response, but now the holes BIST of 80 circuit a mini miniature version, if you put in the circuit then the test patterns can be applied from the circuit and also it can be analyze in the circuit itself. So, if the patterns are applied within the cheap, then it is in the case of BIST.

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Taxonomy of Digital Testing

Criterion	Attributes of testing method	Terminology
Circuit in which form is being tested?	Wafer IC Board System	1. Non packaged IC level testing 2. Packaged level testing 3. Board level testing 4. System level testing
How are the test patterns applied?	1. In a fixed predetermined order 2. Depending on results	Static Testing Adaptive testing

And now, you see the what is the case of online monitoring, in online monitoring what happens, the circuit is ruing is normal operation you are just monitoring. So; obviously, in this case you can not apply any pattern, the circuit is doing is operation no patterns are

applied you are only monitoring and then your gathering whether the circuit is behaving properly or not.

Now, third criteria is in which form it is tested. So, I think I see you have seen, we have all seen that this is black chip with some pins here and there this is called the IC, the circuit as been fabricated and I want to test it. So, this is actually call, package level testing, these circuit has been packaged and you have to do the testing I will (( )) now you have also seen in a board. So, you can have a PCB kind of a thing. So, I think all of you might have seen, this is the per Printed Circuit Board and we have chip which are inter connected.

So, this is called the board level testing circuit has already been in the board now, how can you test, it in case of IC you can apply pattern in in all the points, but in case of a board, you can only apply the pins, patterns which are the input, output of the bolt, it is very difficult to control a pin here, and this circuit because, this pin is already connected to another part of the circuits. So, directly getting an axis to this be difficult, but if it is in a IC level thing, you can easily axis all the pins.

So, if these chips are put or place on us board and you are doing the testing it is actually called the board level testing. Now, all the many number of PCB's are connected and you have made a system like a PC or a laptop, then now you have to do the testing. So, it is more difficult because, in IC you can get axis to the all the pins of the IC.

Now, if I put in the board you can axis only the pins, which are in the input, output of the PCB, all input outputs of the IC you cannot get it. Now, if I go for system which is called level testing, testing some articles more difficult because, now all the PCB's are correct in a system and you can have a axis to only the input, output of the whole system, this is the system there were many PCB's in the PCB's there were many IC's, but you can only axis the input, output of the PCB, internally you can axis.

Now, the something call wafer, wafer is nothing, but when the circuit is fabricated it is a die and you said the die, you will have a wafer this is the direct circuit, which this circuit is actually put in the IC and then this is packaged. So, directly with the wafer can also be tested because, it is very easy to mean get axis to all the pins, like for example, if you have a IC like this is. So, there is a log of many, many, many gives only few of then you

can the axis can access pin of the IC, but if you are accessing directly the die. So, you can access many more pins of it.

So, more system level you go, lessees the number of pins you can access and less more difficult to the testing. So, this is a very raw testing, which called non package IC level test you can have lot of pins. So, low lower you go the, more abstract level you go the less number of pins you are having and, so for. So, but these are the a different levels of testing, in terms of when the circuits are tested.

Now, the courses how will the test pattern apply. So, there can be two things, you can have static, you can plane I have that what you want to apply and also it can be addictive label, depending on the output performance of the test you can change your test patterns.

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Taxonomy of Digital Testing

Criterion	Attributes of testing method	Terminology
How fast are the test patterns applied?	1. Much slower than the normal speed of operation 2. At normal speed of operation	1. DC (static) testing 2. At-speed testing
Who verifies the test results by matching with golden response?	1. On chip circuit 2. ATE	1. BIST 2. Automatic Test Equipment (ATE) based testing

NPTEL

Then there is few others, like how fast is the test pattern apply. So, if you are doing at the normal speed of operation that you are testing at gigahertz. So, it is called at speed testing, but if test or you cannot supply, speed test that was that level you can do much slower that is called DC or slow testing. Now, again who verifies the response of the output that there is the some persons you should response, match the golden response.

So, if it is in case of automatic test equipment, the equipment have everything, but in case of BIST that it is in case of a circuit a online tester or in case of building safeties, on chip there should be a on chip circuit because, in case of BIST, BIST the chip is doing

the online testing. So, so sorry the BIST is doing this circuit is doing the testing in case of online testing, the circuit on chip is doing the monitoring. So, in this case the response analyzer, sits within the on the chip.

So, the in this case if the if the person matches the golden response on chip, you can call it BIST online testing and in case of 80 it is 80 BIST testing equipment will do everything for you.

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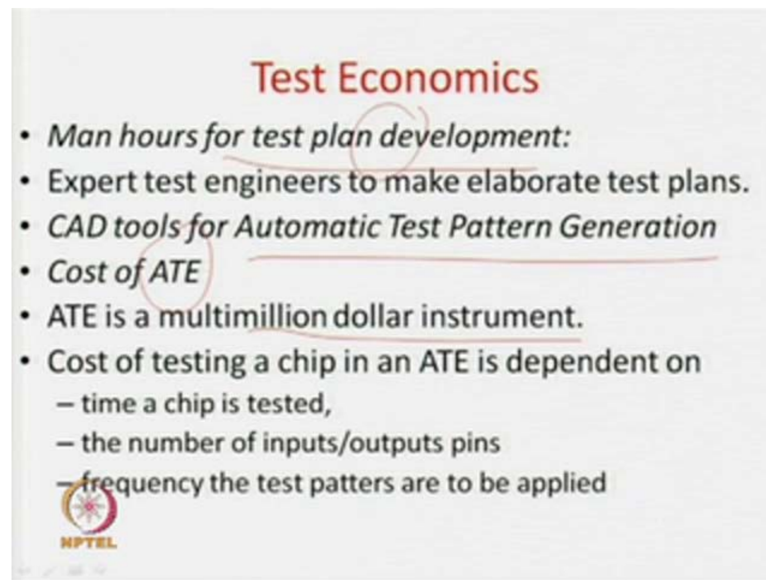

Now, what do you gave and what do you pay. So, pay what you have to do, you have to make test plan, you have required test engineers, you require automatic test equipment which I have shown you the, which extremely expense equipments. So, more is a multi dollar equipment. So, more time you spend on your test that many amount of money that I have to give that is more amount of test patterns or more test you want to do, at more amount of time you have to use the ATE more amount of test you have to pay.

And if you are laying a very intelligent test pattern, and then you have to pay the engineers right. So, that is test now, if you if you increase the test time then you have to use more amount of 80 and more amount of money you have to pay and if make a very intelligent kind of a test plan. So, that with a less amount of pattern test your circuit then you should have a very good test plan.

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Test Economics

- DFT/BIST circuitry
  - Additional circuitry kept on-chip to help in testing results in raise in chip area
  - Rise in area power and lower yield
- At-speed testing by ATE is extremely expensive.

Tradeoff

- Returns
  - Proper binning of Chips:

In case of VLSI testing, it is not of much concern as how many chips are binned as faulty, rather important is how many faulty chips are binned as normal.

But, again that then you have to which as to be very sophisticated or very highly skill man power is required which will again take money. So, whole testing process is basically about trade of economics like. Now, the some people say that, if your ATE equipment is very expensive, why not you put some extra circuitry all chip, which can do a part of the testing for you, in that case some of the patterns can be applied from the ATE and some of the patterns can be applied from on chip circuits. So, this things will be see in details.

So, that which we are again doing is the trade of between the ATE and your circuit, like ATE is the third party tool, third part equipments. So, I have to pay ATE event that. So, I have to if I apply some amount of testing I can do on chip circuited, like BIST or that is or online testing kind of a stuff or some circuit I put on chip to the testing, then I can say some time or some amount of patterns in ATE.

So, but again I have to increase my chip area, then again these are trade of weather I should pay the ATE vender or whether I put some extra circuitry on the chip for testing and I make the chip size higher. But, now what do I get, I get a proper binning of chips. Testing in case of VLSI will never I sure that, all the chips are correct or I will repair my circuits. So, that I can say all myself, that is are difference between VLSI testing and a classical system.

Classical system you test a circuit, then you say that all I repair, all my some irons I find faulty I repair them and then I sell after the market, but in case of VLSI circuit is is not that some 5'th around from 100 say some 60 percent circuits are fine, which is good and some 40 percent of circuits are bad, which I have to throw them out. Now, what I have my circuit VLSI testing is giving me, it is being a very proper partitioning of 60 and 40.

If I somehow sell a defective that circuit into a good group and I sell it to a person, then that will be a big problem. So, that is how, test economics will what did you will help me, test economics basically will give me a very proper kind of, it will give me, you said see that in case of it is VLSI testing not proper concern that how many chips are been faulty, it is another important that, how many faulty chips are being as not that, if you have a faulty chips, you been it and in a good a sell it to a person, the person will have a defective chip, in his that will be sold in that will be in bad reputation on the country; so ours and because there is no scope of repairing a circuit. So, what we have to do, our testing will give you, what do you call good circuits as good and bad circuits as bad.

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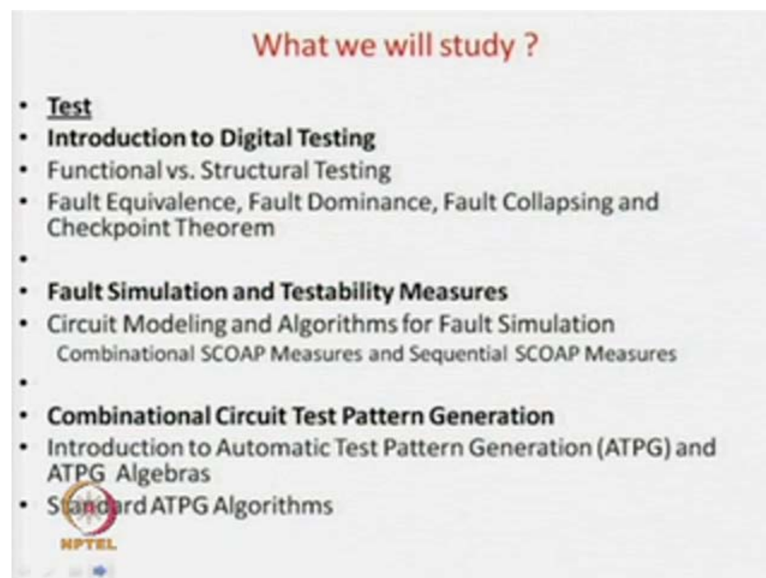

So, that you can, go for, what do you call a proper VLSI testing that is a good is being as good, fault is being as fault, and then you give the proper thing to the circuit. So, in this course, what we are now these are the very introduction to digital circuit testing, the basic philosophy I have told you and what is the different, different classical testing and VLSI testing I have told you because still now, in our mind we had a idea of classical

system. But now, I have explained you that VLSI testing philosophy is bit different from classical system.

So, in this third module, what we are going to read. So, today we have seen about introduction, next in the few lectures we will be looking at structural versus functional testing and, so for then will go for fault simulation, then we will see combinational circuit test pattern generation.

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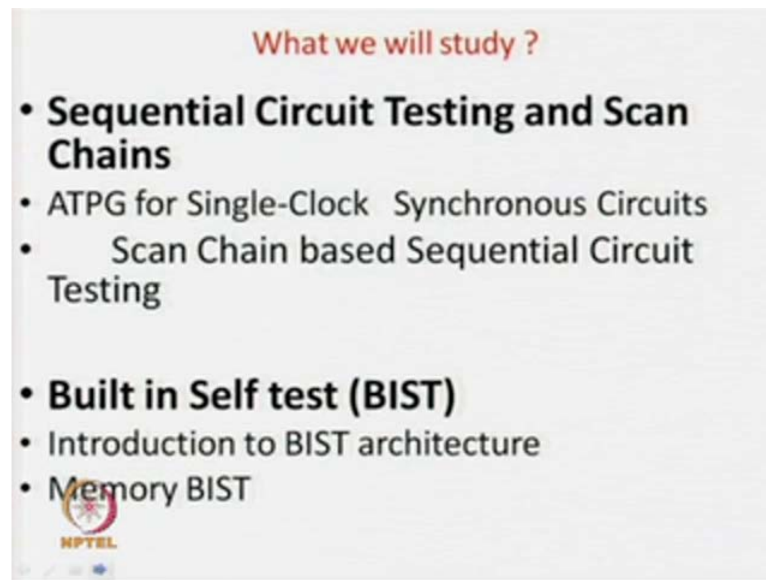

Then, we will go for sequential circuit test pattern generation and finally, we will see if I have to put all the tester on chip that is built in self test, how it will go, and then we will also seen something like, built in self test and may be some ideals online monitoring. So, with this, we come to the conclusion of the first lecture in case of VLSI testing that was the introduction.

In the next class, we will see that how we can intelligently developed test pattern or how we can intelligently plan test, so that I apply very less number of test patterns, we are get a very good confidence that my cover is the very good that whatever binning I am doing is proper.

Thank you.