Computer Architecture
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Lecture - 14
A Primer on Digital Logic Part-I

Hello everybody. Welcome to chapter 6, where we will be discussing about the basic hardware components, that is needed to build processor from scratch. So, what we have done up till now. In the last few chapters that you have looked at what bits can do, how do we use bits to represent integers, numbers, and pieces of text? Then we have looked at three kinds of assembly languages in chapter 3, 4 and 5; the basic simple RISC assembly language ARM assembly and x 86 assembly.

Now, given the fact that we have a decent idea of what assembly languages are, you want to build an actual processor. To build an actual processor what would be discussing in this chapter, is essentially the building blocks of actual processors. So, I want to repeat once again, that this is chapter 6 of the book Computer Organization and Architecture; this has been published in McGraw Hill 2015.

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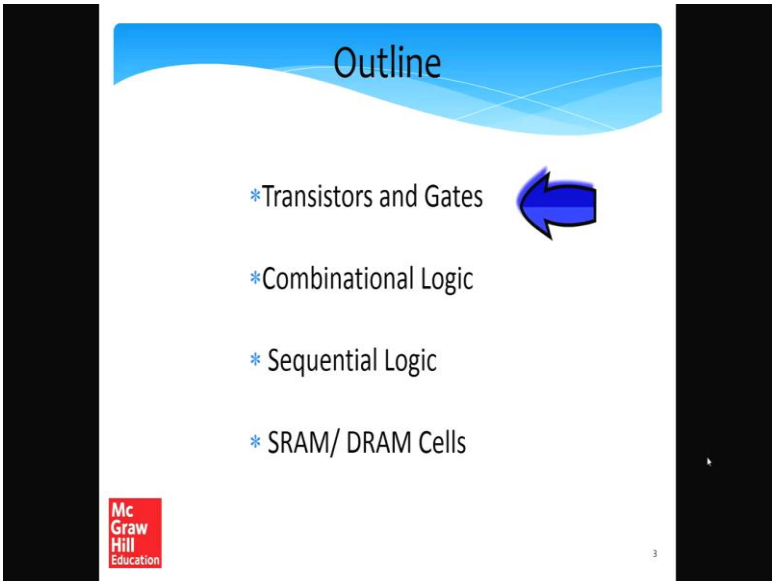

So, let me start with an outline of this chapter. So, this chapter is divided into four sections; the first section discusses the most basic building blocks of circuit, which are transistors and logic gates. Then we discuss combinational logic, which is basically

create larger circuits, by combining this basic elements which a logic gates. Subsequently, we shall discuss sequential logic. So, in sequential logic, we save, we store individual bits, and then we use these individual bits in circuits. Finally, we will discuss SRAM and DRAM cells. So, these are the memory elements inside a processor, we can store data here, we can store bits and bytes. So, SRAMs and DRAMs are two very different technologies.

So, we will discuss both of these in the last part of this chapter.

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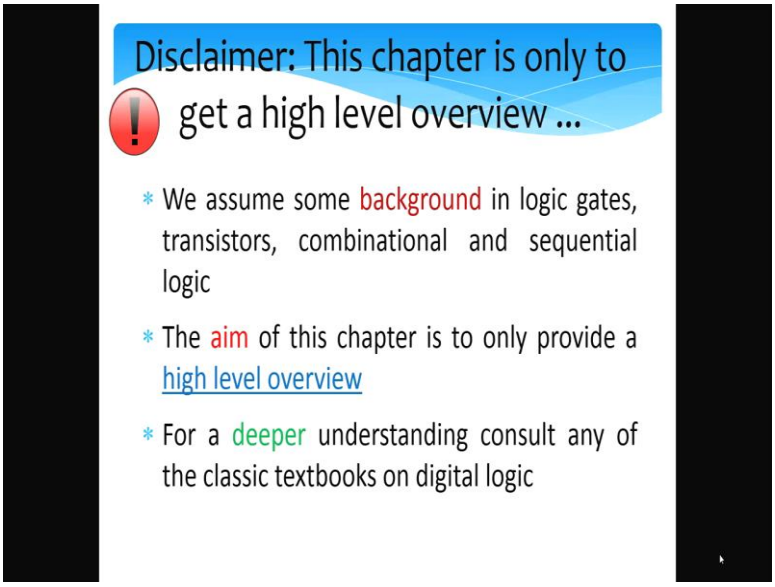

So, let me start with a disclaimer, this chapter we are providing a very high level overview. So, pretty much the entire digital logic course, is being covered in this one single chapter. So, it might be difficult for some readers, or a listener to follow exactly all of that is being said. So, the assumption is that at least students of some background in logic gates transistors combinational and sequential logic. So, then this chapter, you can re recapitulate all of those concepts, and also get a high level picture of all the elements, that we need from the point of view of designing a processor. So, for a deeper understanding if it is required, the students can consult any of the classic text books on digital logic.

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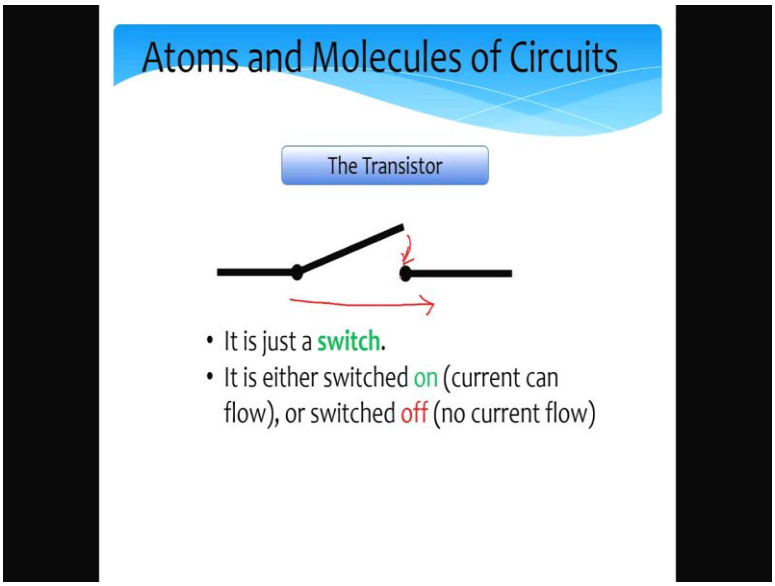

Let us take a look at the basic atom of a circuit, the most simplest, it is like an atom and molecule of a circuit. So, the most basic element is a transistor. So, the transistor in common man's words, is basically a switch, it is the same as a light switch, and is any kind of switch, when the switch is open current is not flowing, and when the switch closes there is a flow of current.

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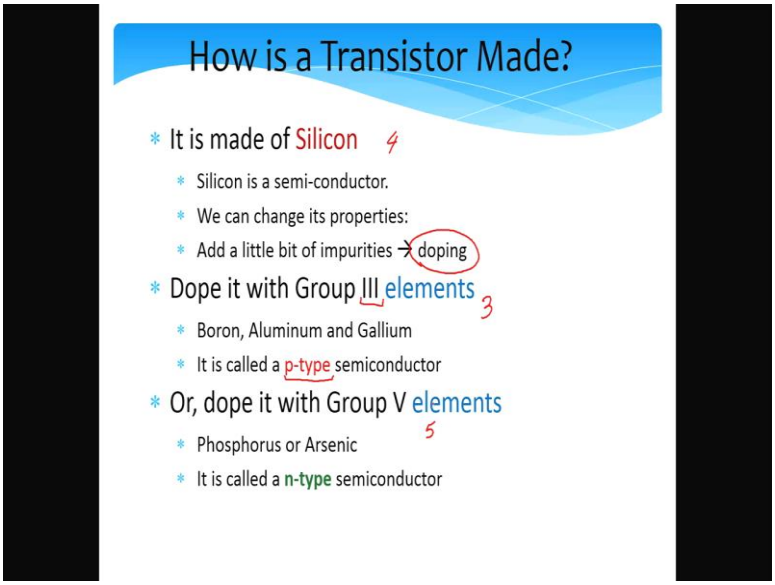

So, this is as simple as that when the switch is on, the current can flow from this terminal to this terminal, and if the switch is off there is no current flow. So, the transistor works

like and open circuit. So, this is the most basic element of a circuit, is just a simple switch. And how is a transistor made. So, transistor previously was being made with different technologies, but for the last 40 50 years, it is being made of silicon. So, silicon is a basic element of sand, it is brownish, grayish material. It is a semiconductor, which means that it is not a conductor and it is not an insulator it lies in the middle. It is.

So, the fantastic thing about silicon is, that it is possible to change it is properties. We can add a little bit of impurities to silicon, and this process is called doping. So, what is doping again. It is the process of adding a little bit of impurities to silicon. Once this is done, we can change it is properties. For example, if you dope it with group three elements of the periodic table; such that boron, aluminum or gallium. So, then it will become a p-type semiconductor; p for positive in that sense. Then in this case the conductivity of the semiconductor will actually increase.

So, we will discuss how, but the basic idea here is, that if you dope silicon with another element, in this case a group three elements or the periodic table, it is conductivity will increase. And so there are ways to control that. Similarly, if you dope it with group five elements of the periodic table which are like phosphorus and arsenic, it is called a n-type semiconductors. So, recall that in the periodic table, in the outermost ban band, in the silicon has four electrons, group three elements will have three electrons, and group five elements will have five electrons.

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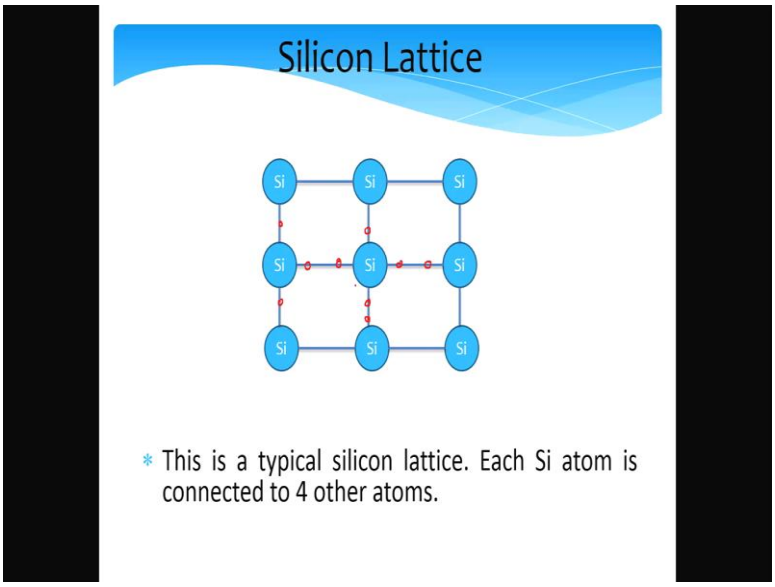

So, how is silicon? So, how is a typical silicon, you know a piece of silicon organized in terms of it is basic atoms. So, well say silicon is a group four elements. So, it has four electrons, in it is outermost layer. Similarly, other silicon atoms also for electrons, so essentially 4 plus 4 become 8, and so they form these covalent kinds of bonds here, and so they arrange themselves in a lattice. So, this a 2 d view of what is otherwise a 3 d lattices, but you can sort of think that each silicon, conceptually you can think that each silicon atom, is connected to four other silicon atoms. So, they form covalent bonds of the way that is shown, to ensure that they have a stable structure.

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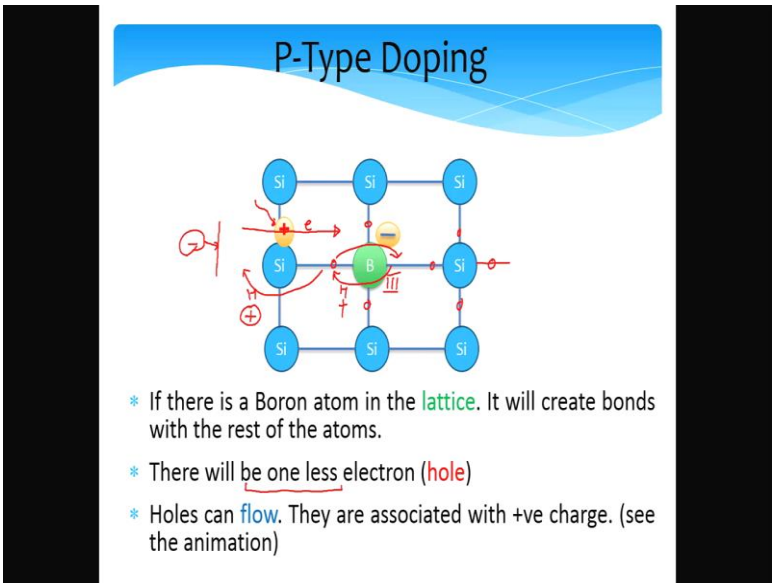

Now, what we can do is, that let us assume that we replace a silicon atom with the boron atom. So, boron atom is a group three atom. So, it has three electrons in it is outermost layer or bit, and basically there is one electron missing, whereas silicon has four electrons. So, what happens is that inside the lattice, there is a hole over here. So, what is the hole mean. A hole essentially means a lack of an electron right. So, basically an electron is not present. So, this is called a hole. So, this is essentially lack of an electron or one less electron being is a hole, and the reason the hole is there, because we have a small boron atom.

So, the interesting thing is, that in this case, the hole scan actually flow in the sense, that this electron can get transferred over here, and the hole can get transferred over here. Similarly, holes can also flow like this, to the hole get transferred over here and electron

from there are comes here. So, the reason that this happens, is that inside the atomic world, things are fairly complicated. So, atoms are connected to each other. So, actually you know one reason that metals are very heavy conductors, is basically because the electrons form what is called an electronic (Refer Time: 09:20) with, electrons form, what is called an electron gas or an electron cloud.

In the sense that all of the electrons are available to sort of carry charger carry current. So, in this case electrons it is true that they are associated with atoms, but they are also somewhat mobile in the sense that they can flow. So, if an electron flows in one direction to cover up a hole. Conceptually we can think that the hole is flowing in the other direction. So, the hole per se is not a physical quantity it is a lack of an electron, but we can conceptually think of a hole as a charge carrier, where it is associated with positive charge, and the fact of the hole moves let us say in this case, from the right to the left, essentially means an electron moves to fill up the hole from the left to the right.

So, the holes are considered as charge carriers. If you take course and device physics you will study a lot about electrons and holes, and compute effective masses of holes and so on, but for the sake of an overview, these advanced concepts are not required. The only thing that needs to be understood, is that a hole indicates the lack of an electron, and hole it is elf can flow. For example, if I apply, let us say a strong negative charge, that will essentially repel electrons away from it. So, basically the hole can then flow towards the negative terminal, which essentially means electrons are flowing in other direction, and the hole is flowing towards the negative terminal.

So, the hole we can think is that it is conceptually associated with positive charge. Similarly we can have another kind of doping. There is a animation over here, so let me show this once again. Let us consider the hole that was created by adding the boron atom, and let us consider an electron. So, if we apply a strong negative potential over here, then electrons will get repelled from the negative potential, and thus the, an electron will take over a hole, and the holes can migrate towards the negative terminal. So, we are thinking of a hole as a net career of positive charge, and it essentially can move. So, it is associated with current.

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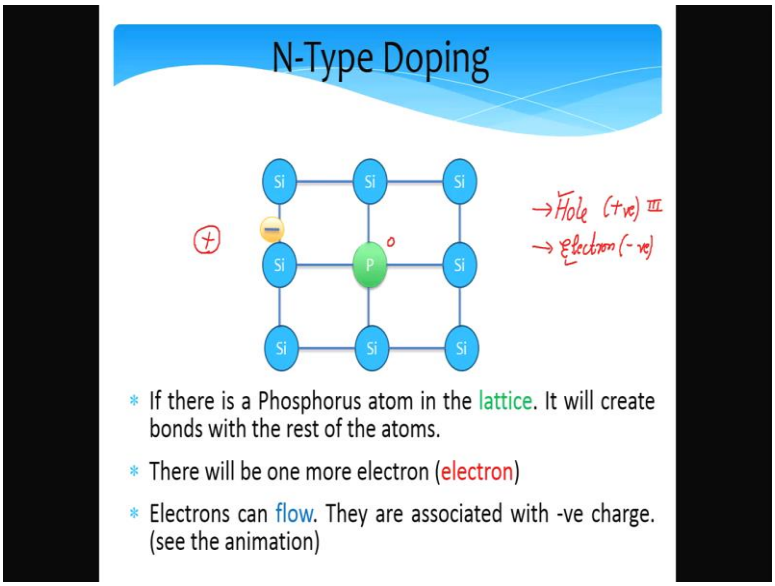

So, let us now look at a similar kind of doping called n-type doping, which is actually the reverse of doping with group three elements in this case where the doping with group 5 elements. So, let us assume that there is a prosperous atom in the lattice. So, it will create bonds with the rest of the atoms, which is fine, but will have an extra electron. So, this extra electron; that is there, can essentially migrate and carry current. So, this electrons will flow it is associated with a net a negative charge.

So, let us show a similar example, that electrons on the application of the electric field which is essentially a potential difference, electrons can flow right from the negative end to the positive terminal. So, at this point what are the two important concepts that we have read. We have read the concept of a hole, which is a lack of an electron, but conceptually it can be thought to carry positive charge, and then we have studied about an electron, electron carries negative charge. So, how is a hole introduced? A hole is introduced when a doped silicon with a group three elements, in that case one electron is missing, as you can see from the previous slide; one electron is missing from the lattice, so that creates a hole, and the hole can migrate and electrons can come and fill it up.

So, basically the hole in this case is thus associated with positive charge. Similarly, in this case, will have an extra electron, which can migrate within the lattice, and it will migrate towards the positive terminal as a shown in the animation over here, and thus it can carry current. This is precisely the reason why, if you doped silicon with positive

with, either you know a group three elements or group five element where extra charge carriers, and what are the extra charge carriers, they are either holes or they are electrons, and thus the net connectivity increases.

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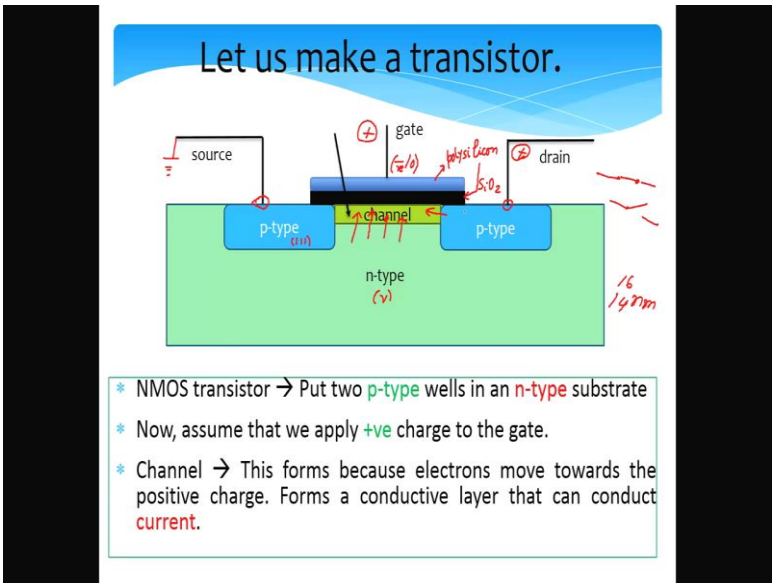

So, with this basic understanding of p-type and n-type semiconductors; what are n-type and n-type semiconductors are? Semiconductors doped with group five elements like phosphorus, and p-type semiconductors is silicon essentially doped group three elements which is boron. So, let us make a simple transistor. So, let us considered an n-type well, and in that put two smaller wells of p-type material as this shown, then let us have a metallic contact, and let us call this terminal the source. This is called the source. Let us call this the drain, and then let us put a layer of silicon dioxide which is an insulator, which is a very strong insulator in fact. Silicon dioxide is regular sand. See put a layer of silicon dioxide and then conductor on top of it, which is typically poly silicon, but it is not necessary as poly silicon, it can be a metal as well, but does not matter. Once second.

So, it is typically poly silicon layer which is a conductor, and on top of that we attach metallic wire, at this terminal, is called a gate. So, basic transistor has two terminals sorry three terminals; one of them is the gate, one is the source, one is drain. So, this is called in NMOS transistor. So, in NMOS as n transfer the negative the fact that is an n-type substrate, so basically the MOS transistor over here. How do we do we put to p-type wells, in an n-type substrate.

So, now let us assume that we apply positive charge to the gate. If we apply positive charge to the gate what will happen right. So, say let us assume that there is positive charge to the gate. So, what will happen is that, all the electrons will start migrating towards gate. So, in this case, a channel will form a channel of electrons. So, this will form, because all the electrons and migrate to it is positive charge, and the channel over here which is rich with electrons, is a conducting channel, because it has a lot of charge carriers.

So, it will be conducting channels, it will be possible to actually pass current from the drain to the source via the channel. So, that is a possibility, answer thus the transistor in this case the switch will in a sense close. So, basically current can flow. Then if we apply a negative or 0 voltage to the gate the channel will go away, and since even a doped semiconductor is not a very good conductor of electricity, we can think of this as the switch being open.

So, what is the controller of the switch? The controller of the switch is the potential at the gate. If we apply a positive voltage at the gate, all the electrons will get attracted towards the gate, and they will get accumulated over here, because they cannot move further, this is because of the s i o 2 insulator that is over here, the black box, but they will accumulate here and they will form the channel, and then if let us say we apply a positive charge at the drain, and let us connect the source to the ground. It is possible for current to flow across the channel, and the reason it is possible is, that because the channel has a lot of has an excess of charge carriers, and if it can conduct current. So, in this case the switch is closed, but now I see apply and negative or a 0 voltage right, let me write negative, or 0 voltage to the gate the channel will vanish, it will break down, and the transistor will not remain a good conductor.

So, this is very high level 20,000 feet kind of view of what transistor does right. Essentially a transistor as a switch; and say if a mechanical switch how does it work? We essentially press it with our finger. So, in this case we do not press it with our finger, because a transistors typically a very small structures. So, now, it is a transistor typically 16 nanometers or 24 nanometers right very small structures. So, instead we apply a voltage at the gate; if it is a positive voltage in the case of an NMOS transistor, the transistor will conduct otherwise a transistor will not conduct current.

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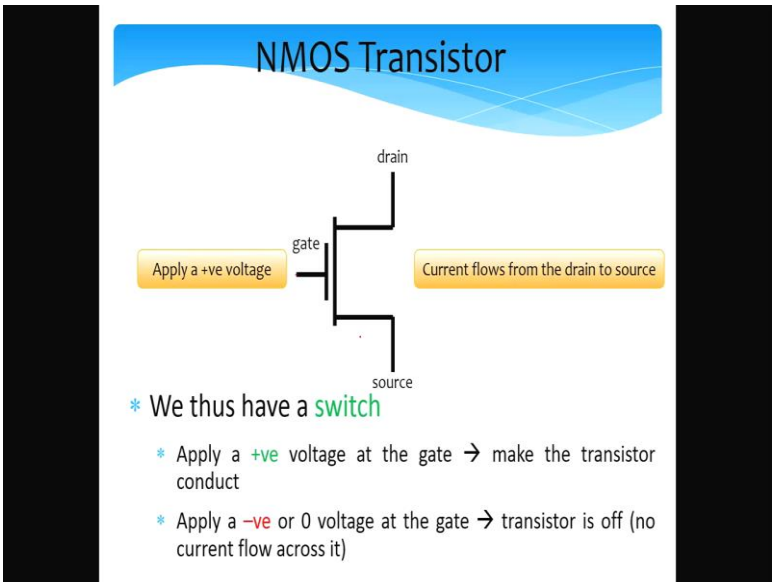

So, the symbol for an NMOS transistor is like this, that this is a symbol, this is a gate over here, and then we have two terminals the source and the drain, which are interchangeable. The most important point to note is, that if we apply a positive voltage at the gate, the transistor will conduct it will become like a single wire, with a resistance of course, and if I apply and negative or 0 voltage of at the gate, the transistor is off. So, it will no current will flow across it. So, apply positive voltage current flows to the drain to source.

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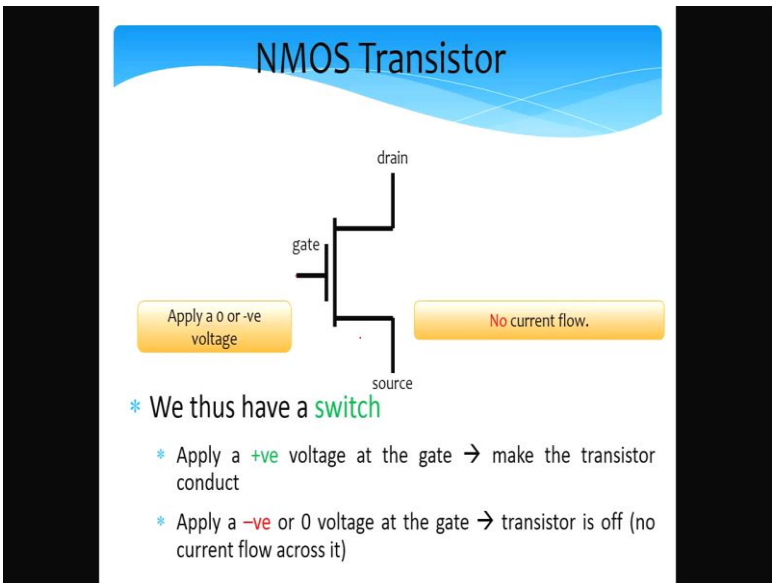

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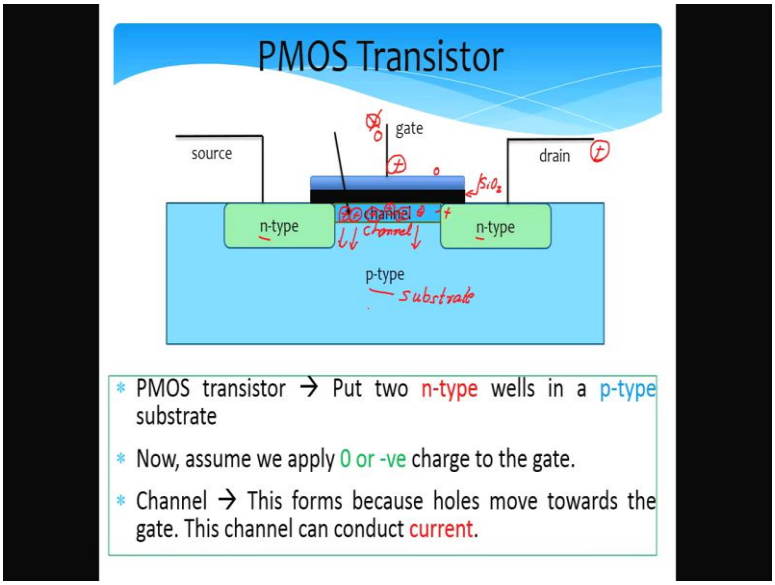

Apply 0 or a negative voltage, there is no current flow. Now let us take a look at the reverse; a PMOS transistor. In this case inside a p-type well we have two n-type smaller wells right, or actually this is not called well is called as substrate. So, inside a p-type substrate, we have to n-type wells.

So, in this case, the control is actually reverse. See we apply a 0 or a negative charge to the gate what will happen is that, all the holes will. Let us say apply a negative voltage to the gate or even if there is no voltage. So, what will still happen, is that I can design the transistor in such a way, that if there is a small negative voltage or even if the voltage is 0, all the holes will get deposited here, just below the s i o 2 layers. So, the structure is the same. So, here is what I can do. So, let us assume that I apply a positive charge to that drain right, and in this case let me assume that the gate in this case is connected to the ground. So, what will happen is that if you consider let us say this region, this region of the transistor. So, in this case there is a net positive charge, and here let us see the charges 0.

So, what will happen, is that because of the positive charge, all the holes will get repelled and they will essentially move, try to move towards the top which is the gate. They will not be able to go because the s i o 2 layer, layer is there, they will essentially get stuck over here at the boundary. So, will have an excess of holes over here right. So, we will have less holes here, but will have more holes towards the n-type, nevertheless will be

some holes over here. So, will have a lot of charge carriers in this region, mainly because there is a potential difference right, and holes will be will sort of get repelled from the positive regions and move towards wherever they see a lesser voltage, and lesser voltages at the gates, all the holes will try to move towards the gate, and this they will accumulate in this region, and they will form a channel.

So, this is this part is the channel. After that we can have a stable current flow across the channel. So, this is the switching of a PMOS transistor is exact opposite of an NMOS transistor. In a PMOS transistor, the channel gets formed, when the voltage at the gate is either in a 0 volts or the voltage is negative, and this is when the transistor conducts. If you then apply a positive voltage at the gate, what will happen is that all the holes will get repelled away from it, and a channel will pretty much time. Once there is no channel there are no charges carriers in this region, hence current will not flow.

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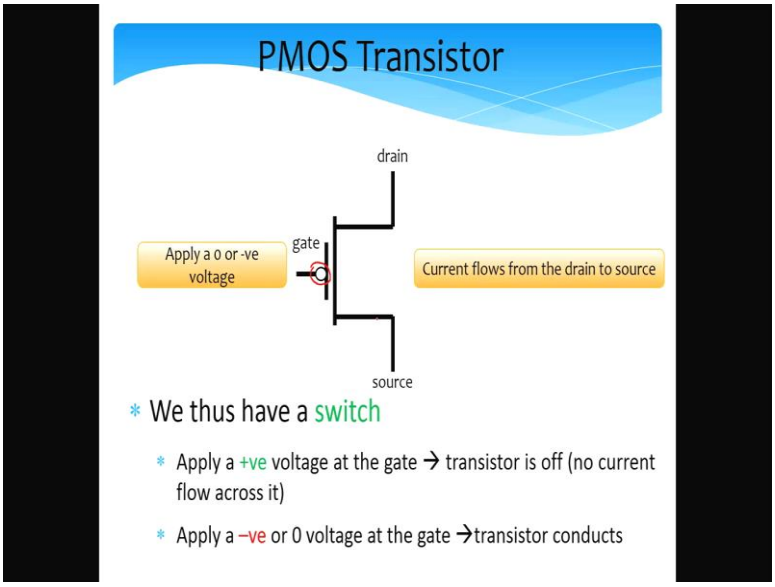

Now, let us take a look at the symbol of the PMOS transistors. So, it is the more or less the same as that of an NMOS transistor with one simple difference. So, the difference is the circle over here at the gate terminal. So, that is mainly the only difference; otherwise the rest of the diagram is the same, and we have two terminals the drain and source which are interchangeable terminals, and in this ways if you apply is 0 or negative voltage, the transistor conducts the current flows from the drain to source.

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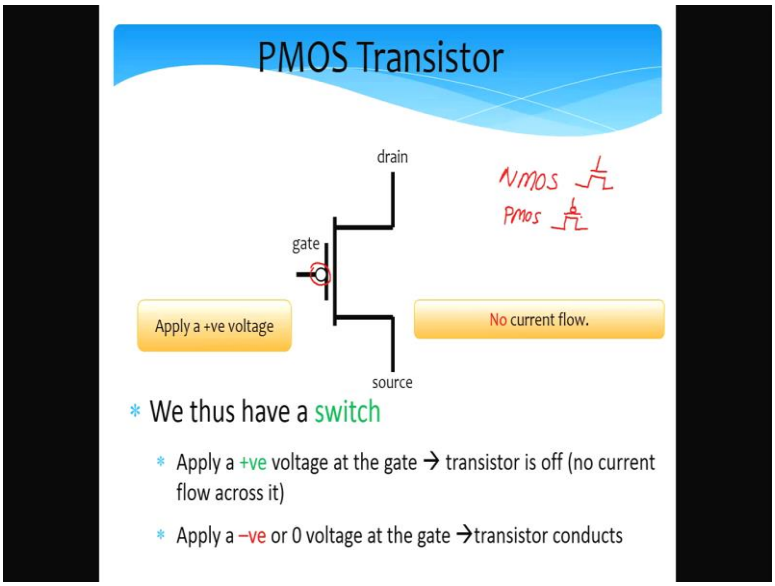

And if you apply a positive voltage of the gate, the transistor is off there is no current flow. So, let me at the end summarize our discussion. So, we have two kinds of transistors; the NMOS transistor and the PMOS. So, n basically stands for an n-type substrate whether to p-type wells. So, in NMOS transistor, what is MOS? It is metal oxide semiconductor the reason being that we have all three here. We have a semiconductor substrate, we have an oxide layer silicon dioxide layer, which is the insulator on the gate, and we have metallic contacts to the transistor. So, we have a metal oxide and semiconductor.

So, the NMOS transistor whose symbol is like this is basically controlled by the voltage at the gate. If it is positive current flows otherwise it does not flow right. And the PMOS transistor the symbol is more or less the same, is just a give a circle over here. So, it has a reverse operation. So, if the voltage of the gate is either 0 volts, either the gate is grounded or it has a negative voltage. In this case current does not flow across the transistor, I am sorry current flows across the transistors, and the gate has a positive voltage, then current does not flow across the transistor.

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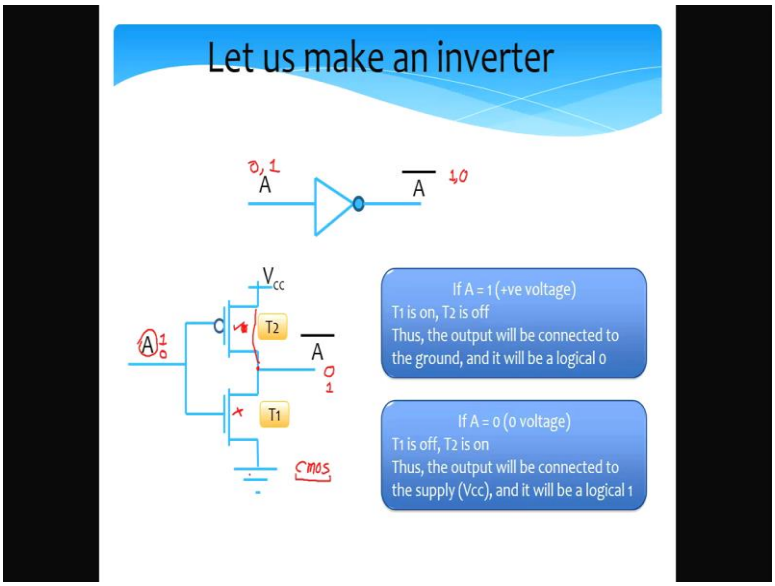

So you have two switch; two different kinds of switches, with different modes of operation. So, let us use this transistors, you know what good is knowledge without actually using it. So, let us use to make an inverter. So, this is the sign of an inverter. So, what it does is, that if I apply a logical 0, then the output is a logical 1. So, if logical 0 might physically correspond to 0 voltage, and a logical 1 might correspond to 1 volts or 2 volts or 3 volts that is a material.

Then if I apply a logical 1, then at the end I get a logical 0. So, it pretty much compresses the complement of a bit. So, how do we do it. So, let us assume that I send in a logical variable at which can be 0 or 1, and I have an NMOS transistor T 1, and a PMOS transistor T 2. The PMOS transistor is connected to the supply voltage v c c at the top, and the NMOS transistor at the bottom is connected to ground, and the output is from, is basically at this terminal in the middle of the diagram.

So, let us first see if I apply, if A is equal to 1, if it is a positive voltage what happens. In this case if it is positive T 1 will conduct right, T 1 will conduct and T 2 will not conduct. So, effectively this terminal will get connected to ground. So, if the value here is one, the value here, since is connected to ground will become 0. So, it effectively works on inverter. Similarly let us take a look at the other case, where A is equal to 0, or 0 voltage. So, the other case what will happen is that the transistor at the bottom T 1 will not

conduct right, but the transistor T 2 will conduct, and this output will be connected to V c c. So, then in it will become a logical 1.

If I have a logical 1 here the output is a logical 0, and if a logical 0 as the input, the output is a logical 1. So, this acts an inverter. So, this kind of a circuit is a combined NMOS PMOS circuit. So, it is called a CMOS circuit. So, it is combined circuit right, has both NMOS elements PMOS elements, but the important thing is that we put NMOS in PMOS in series, and one end of NMOS is at the ground, and one is at V c c. And all that you need to do to understand operation of such circuits, is basically considered pairs of inputs, so, the input is a logical 1. Then you need to find out which transistors are on and which are off. So, in the case of logical 1, this T 1 is on and T 2 is off. So, the output gets connected to ground, hence it is 0.

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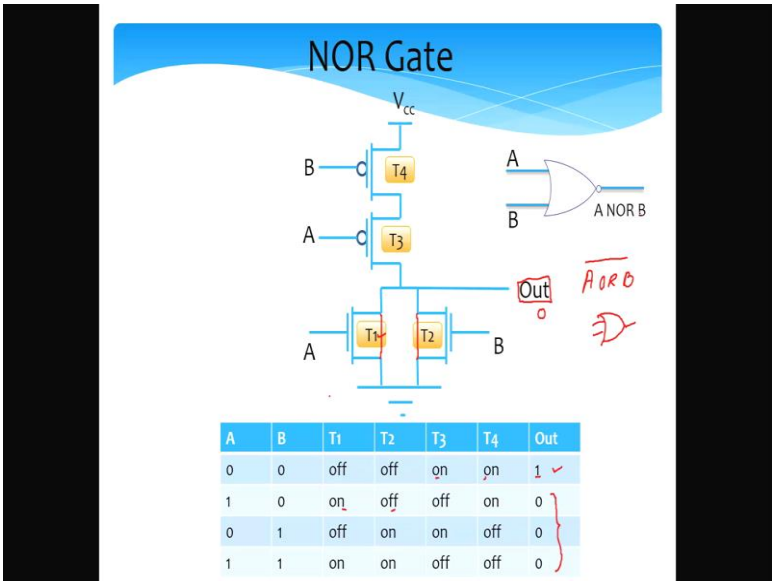

A	B	T1	T2	T3	T4	Out
0	0	off	off	on	on	1
1	0	on	off	off	on	0
0	1	off	on	on	off	0
1	1	on	on	off	off	0

So, let us see more examples of a similar logic. So, let us consider a NOR gate, which is of the same type at least. So, it is looks similar, but we have twice a number of transistors. So, let us find out what it does. So, NOR gate is actually. So, let us first take a look at the NOR function. So, we know a NOR function, which is A or B. So, NOR function is essentially the logical complement of A or B. So, let us consider the combinations of values of a 0 1 0 0 0 0 0. So, the NOR of 0 and 0 is the knot of 0, which is the logical 1.

For all the other combinations of A and B which are 1 0 0 1, and 1 1 A or B is equal to 1 and it is compliment is 0. So, that is a reason all three of these values, are 0. So, this is exactly what you want to compute, via these four transistors. So, let us see the organization. So, we have four transistor name T 1 T 2 T 3 and T 4. The input A is connected to T 1 and T 3, the input B is connected to T 2 and T 4. So, T 1 and T 2 are connected in parallel, and T 3 and T 4 are connected in series. So, T 1 T 2 are NMOS transistors, and T 3 and T 4 are PMOS transistors.

So, let us first considered the simple case, where A is 0 1 B is 0. So, in this case both the NMOS transistors are off. So, T 1 and T 2 are off, and both the PMOS transistors T 3 and T 4 are on. So, the transistors are on this basically means that T 3 and T 4 form a conducting path. So, the voltage at the output terminal out, will be the same as V c c or the supply voltage right. So, the voltage at the out terminal will be the same as V c c the supply voltage, because T 3 and T 4 are conducting. So, hence that will be a logical 1.

Now, let us consider the next situation, where A is 1 and B is 0. So, A is 1 the transistor T 1 will conducts as a result it is on. Since B is 0 T 2 will be off as a result it is off. Similarly let us take a look at T 3 and T 4. So, since A is 1 logical 1 at the high voltage T 3 is turned off and T 4 will be turn on, it does not matters. So, the reason it does not matter is, because when transistors are connected in series. If one of them is off, the entire line is off, but what we have over here for this, for the second input. These are the transistor T 1 is conducting. So, the output terminal is directly connected to ground, because this transistor T 1 is conducting. Essentially we can sort of add a straight line over here, that it is directly connected to ground. As a result the voltage at the output terminal is equal to the ground voltage, which is 0, and thus output is a logical 0.

Similarly, we can consider the other pair it is an absolutely symmetric argument here for 0 1. So, in this case when A is 0 and B is 1, you can see that the. So, this is basically T 1 is off, T 2 is on, T 3 is on, and T 4 is off; the important point to note that in this T 3, T 4 pair, in this case T 4 is off. So, as a result you know supply is not connected with the output line, but out of T 1 and T 2, T 2 is on. So, in this case this is become a closed circuits. So, as a result the output terminal is connected to the ground via T 2, and it is voltage is 0.

Similarly, both A and B are one and one, then both T 1 and T 2 are conducting. So, both of these lines, you know the outputs are connected to the inputs. So, the output terminal is connected to the ground, and since the ground represents 0 volts, the voltage at the output terminal is 0. So, what we get to see over here is that using a CMOS logic, we can have, we can create with NMOS and PMOS transistor the structure via which we can compute A NOR B, essentially A or B complement, and this is the symbol of the NOR gate. So, which is a regular NOR gate and the circles. So, the circle denotes inversion. So, a regular or gate would be a gate like this right, A and B two terminals. So, we add a circle at becomes A NOR B, which is the complement of A or B.

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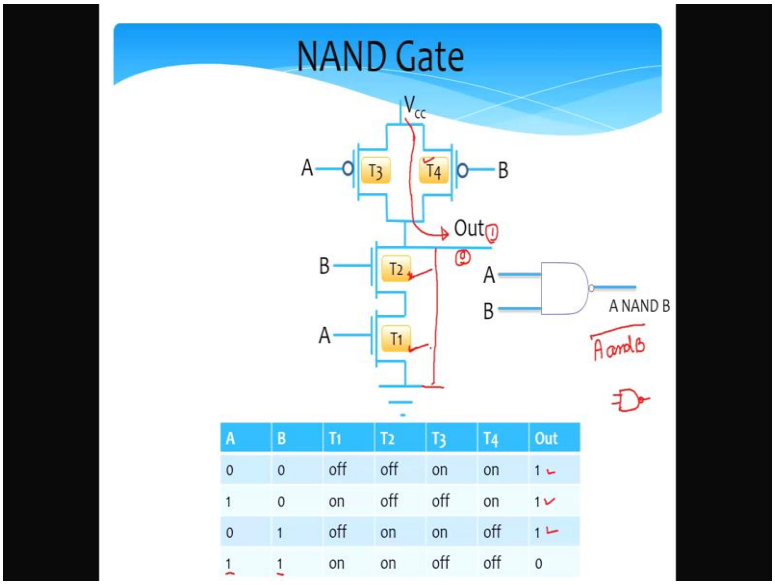

A	B	T1	T2	T3	T4	Out
0	0	off	off	on	on	1
1	0	on	off	off	on	1
0	1	off	on	on	off	1
1	1	on	on	off	off	0

So, let us now take a look at the NAND gate. The NAND gate is the same thing as NOR, essentially conceptually the same thing, where we compute A and B, and we take a logical complement of this. So, this is becomes A NAND B. So, here what we have is, that we have a similar looking design, very different though, if you taking a look at the details.

So, we have the NMOS transistors in series, T 1 and T 2, and we have the PMOS transistors in parallel. So, the input A is connected to the T 1, as well as to T 3, and the input B is connected to T 2 as well as to T 4. And this is the symbol of an NAND gates, so which is basically a NAND gate plus a circuit. So, had I drawn the gate symbol as this, this would have indicated A and B, but if I draw a circle over here, it indicates A

NAND B. NAND basically means a compute the logical and between A and B and then I take the compliment. So, that is A and B compliment.

So, what I can do now, is that let us take a look at all combinations of A and B are how the circuit works. So, if A is 0 B is 0 both T 1 and T 2 are off, but T 3 and T 4 both of them are connected are on. So, basically the voltage at the output terminal will be the same as that in v c c. So, as you see the output voltages one. So, let us consider the case where A is 1 and B is 0. So, if A is 1 then transistor T 1 is conducting, but transistor T 2 is off.

So, as we had mentioned in the last slide, when two transistors are connected in series, when one of them is turned off, essentially current is not going to flow via that line. So, so basically we can sort of assumed that the output terminal is disconnected from the ground, but let us take a T 3 and T 4; that is more interesting. Since A is 1 T 3 is turned off, but then B is 0 T 4 is turned on; hence we have a conducting path between the supply voltage via T 4 to the output terminal right. So, basically current can flow like this.

As a result what can happen is, that the voltage here will get set to the same voltage, similar, roughly similar voltage at the supply voltage, and we can assume that it is a logical 1. So, I will not be describing other symmetric case here where A is 0 and B is 0 1, but the logic is very similar. So, in this case also the output is a logical 1. Let us now consider the case where A is 1 and B is 1; that is important, because that is when A and B is 1. So, A NAND B has to be 0. So, A is 1 and B is 1 the transistor T 1 conducts, and transistor T 2 also co conducts. So, essentially we have a straight path between the output to the ground. What about T 3 and T 4. Both of them are turned off, because the voltages at A and B are one each. So, what we sees that in this case, the output will be driven to a logical 0, because it is directly connected to ground which is assumed to be at 0 volts.

So, this is the operation of NAND gate, which is very different from that of the OR gate, I am sorry the NOR gate, but the important take home point is that we are connecting. In the previous case we connected the p NMOS transistors in parallel the PMOS in series, and for this case we are conducting the NMOS transistors in series and PMOS in parallel, and if it analyze. So, how do we analyze such circuit is, basically analyze for all pairs of inputs. So, in this case there are four pairs of input, four possible pairs of inputs.

We just need to make a table of the form that I have shown of which transistor is on and which transistor is off, and then you will quickly see that the, according to the design it will the output will either get directly connected to the supply voltage, which will give it a logical 1, or get directly connected to the ground, which will assign at a logical 0.

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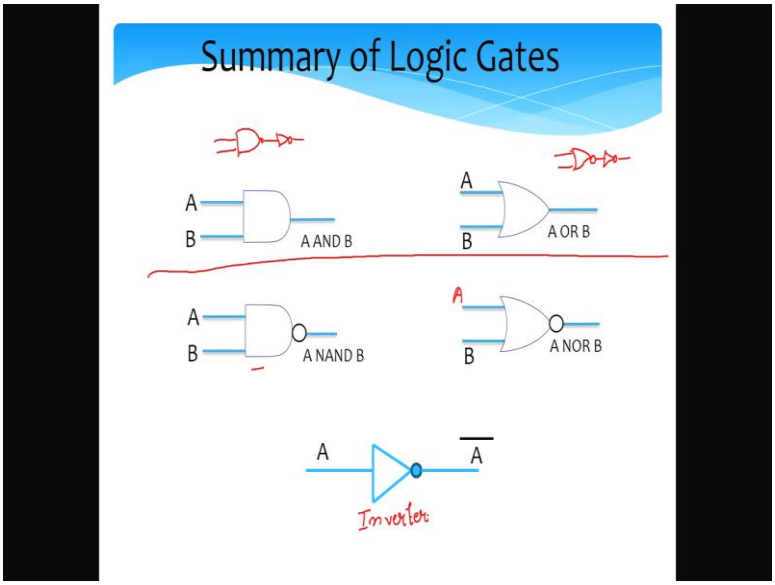

So, here is a summary of logic gates, all are learning up till now that we have done. So, we built all of these with basic transistor with NMOS and PMOS transistors. So, we can build a. So, first built an inverter; some starting from bottom up, so the first built an inverter that complements a single bit. Then we built an NAND gate. So, how did we build an NAND gate what we basically did is, that we had and MOS and PMOS transistors some in series and some in parallel with the symbol for a NAND gate. We also built an NOR gate, sorry I should add this. So, we also built an NOR gate, where we take A and B and we compute A NOR B. So, basically NAND and NOR are actually called universal gates, in the sense that we can realize any logic function, with only NAND gates and NOR gates. So, that the description of you know why this is the case is somewhat difficult. So, I will not you know discuss it now, but should be kept in mind.

So, now we can easily construct a NAND gate with at least all the basic gates that we have created. So, what we can do is, that we can take a regular NAND gate, add an inverter to it, and then we will become a NAND gate. Similarly we can create a NOR gate. So, what is the idea we can take a NOR gate that we have made with our

transistors, then connect the output to an inverter. So, we have A or B. So, symbol for an OR gate is like this is. So, only difference and gate symbol, and OR gate symbol is that in this case this line is straight, and this line is curved, and also in an OR gate you can see an additional curvature, like this looks, like an arrow right pretty much.

So, this is where. So, these are called basic logic gates and and or NAND NOR and inverter of course, right. So, let me maybe try turn inverter over here. So, these are called the basic set of logic gates that we have, in our arsenal, and these basic logic gates we can use to build far more complex and complicated circuits. So, I will discuss that in the next few lectures, but let us just keep this basic figure in mind, that these are the basic logic gates that we have created from pretty much bare and simple transistors.

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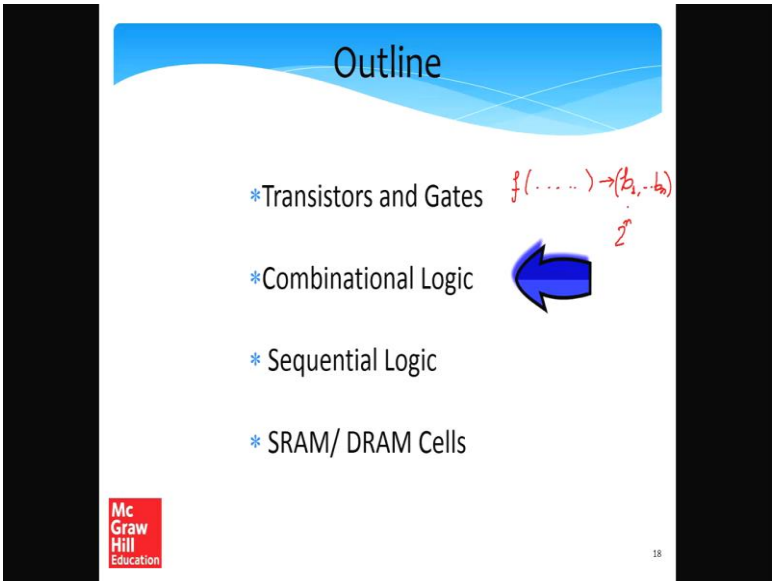

Let us now discuss combinational logic. So, so what is combinational logic, it is essentially creating a complex logic function. So, let me see what is the logic function? So, logic function takes multiple Boolean variables as arguments, and returns an output, which is the Boolean variable, or it can return the series and outputs as well. So, it can also return a set of Boolean variables B 1 to B n.

So, this is made of logic gates. So, the final output is essentially one of the possible. So, if let us say, that there are n outputs. So, there are 2 to the power n possible values, some of these values are allowed in some are not allowed for a given set of inputs. So, the typically for a given set of inputs only one value out of this set is allowed. So, so that is

the reason we call it of combinational logic, where essentially we take a combination of Boolean bits, and we determine the output.

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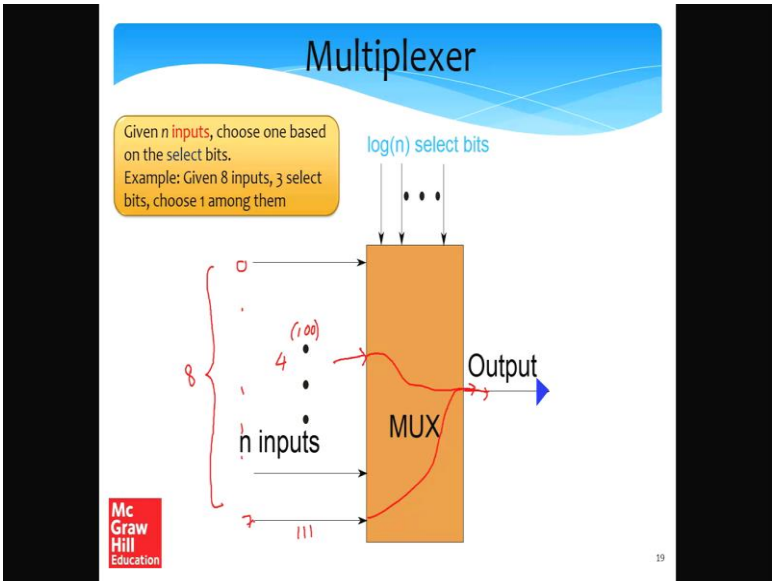

So, let us first discuss. So, what we want to do in this part is essentially discuss some of the most important combinational logic blocks, that are used typically in modern processors, and a multiplexer is probably the most important logic blocks. So, let us discuss that first. So, so remind you in combinational logic, we just take combination of variables, and then we decide the output. So, there is no storage per say. So, say let us consider a multiplexer.

So, in multiplexer given n inputs, we choose one of the inputs as the output based on the select bits. For example, if there are eight inputs over here, then we will choose one of the inputs; for example, let us say this input, to get reflected in the output, based on the values of the select bits. So, let us say this is input number four, and there values are the select bits are 1 0 0, and we will choose this input to get reflected at the output.

Similarly, if this is the last, if let us say the last one, the last line we want, the value of this to get reflected at the output, then the value of the select bit should be 1 1 1 right, where we are assuming that the number from 0 till 7. So, this is this is a very important element in the design of processors. So, we will see why this is the case when we go to chapter eight. Mainly chapter eight and chapter nine, but nevertheless let us try to understand how to actually build one such circuit to implement a multiplexer.

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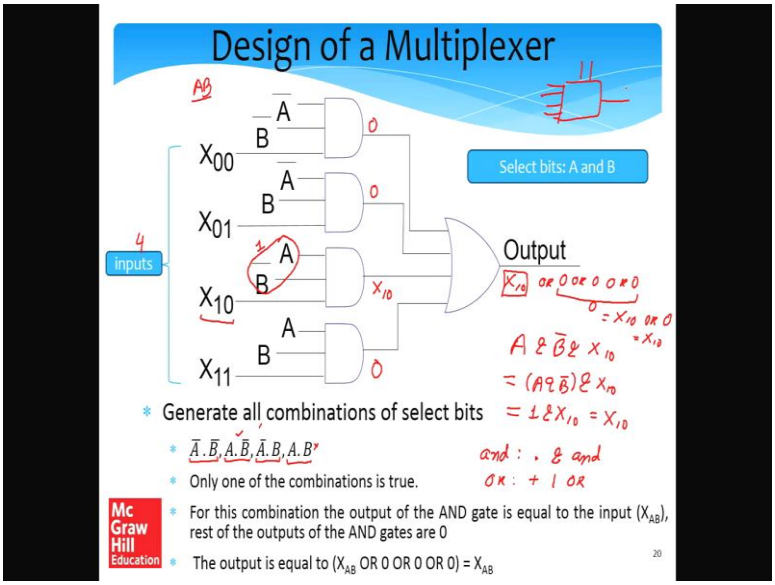

So, let us consider two bit multiplexer, where there are four inputs, and there are two select bits A and B. So, if A and B are 0 0 we want to choose the first input, 0 1 the second input, 1 0 the third input, and 1 1 the forth input. So, what we do is, that we generate all the combinations of the select bits. So, the four combinations are a bar and B bar, A and B bar. So, B bar means the compliment of b, and a compliment and it with B a bar dot B and a b.

So, they are generating all the combinations of select bits. So, only one of the combinations will actually be true, for any value of A and B; for example, if A is 1 and B is 1 only this combination will be true. If A is 1 and B is 0, then only a dot B complement will be true; so only one of these combinations is true. So, for this combination, what we do is. So, with the way we design the circuit, is that we take each combination of the select bits, either original bit or it is complemented form, and we and it with the input in an and gate.

Since only one of the combinations is true, the output of the rest of the and gate, will actually be 0. So, let us assume output of this and gate is 0, this is 0 and this is 0. And in this case let us assume that this combination is equal to 1. So, x 1 0, if the input is one then output is one, if the input is 0 the output is 0. So, in the sense the output is reflecting the input, is the select bits. So, so if let us a this particular combination over here, is equal to 1.

So, since in this case the output is reflecting the input, this is x 1 0. So, let me explain this once again. Since A and B bar is equal to 1, pretty much their value does not matter, the output of the and gate will be equal to whatever is the value of x 1 0 right, because what is the outputs it's a. Let me use a and symbol and, sorry is A and B bar and x 1 0, which is equal to A and B bar x 1 0. Since A and B bar in this case is one, it is one and x 1 0, which is equal to x of 1 0. So, the output here will get, the output here will get reflected on the basis of the input. So, now, let us consider the OR gate that we have over here; since a all the rest of the values are 0, the output will also reflect the input, because anything odd with any Boolean variable odd with 0 is a Boolean variable it is elf. So, what we are effectively computing is x 1 0 or 0 or 0 or 0. So, 0 or 0 or 0 this entire thing is 0. So, essentially this is x 1 0 or 0 which is x 1 0.

So, what we can see is, that in this particular case, where we are setting a dot. So, in this case A is 1 and B is 0, only this combination is true that the rest of the combinations are false. as a result at this point the output is the same as the input, the chosen input x 1 0, and similarly at output of the or gate the output is equal to the chosen input. So, for the entire circuit; the output is equal to the input that we choose which is x 1 0. So, one more note regarding this equations I could I could have used a different terminology as well. So, typically for and, typically for and operation, will typically used a dot operator. We might use the, and operator sometimes to make the explanation easy. We might write and also to make the explanation easy.

Similarly, for or we would use the plus operators, we can use the or operator which is like a single or vertical bar, or we can just write or, so we will use these symbols interchangeably, depending upon the contexts, but the meaning is the same. So now, coming back to a multiplexer, with the help of these equations, what we essentially showed, is that depending upon the values of the select bits, only one combination is true, and for the input corresponding to that combination, it gets reflected with the output or the multiplexer. So, on a whole what do we have, what we have is that we have four inputs coming in and we have two select bits, based on the value of the select bit, only one of the inputs gets reflected at the output.

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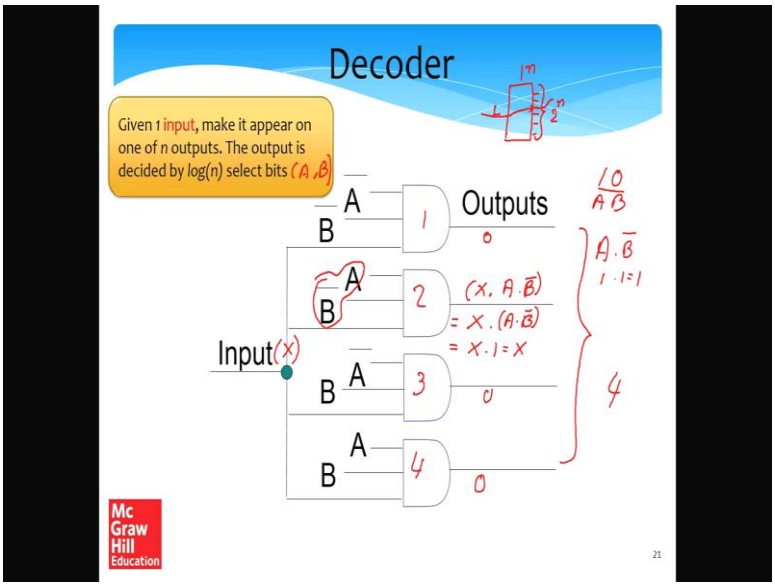

So, now let us look at another structure called a decoder. So, decoder is very important, it is typically used in the design of on chip memories. So, in that sense, it is extremely crucial and vital to the design of processors. So, what is a decoder? So, decoder, the decoder is also sometimes called demultiplexer, but we will use the word decoder in all our discussion. So, what it means is like this, that given one input, let us make that input appear on one of the n outputs. So, let us say we have one input, and in this case we have four outputs. So, we want to make this input, appear in any of the four outputs, based on the values of the select bits A and B. In this case the select bits are A and B.

So, let us assume that, let us say the select bits are one 0. So, if the select bits are one and 0. So, which means that A is 1, and B is 0. So, we wanted to appear on one of the outputs, that corresponds to 1 0. So, let us see how does this work? So, the way this works is, very very similar to the way that the multiplexer used to work. So, in this case we will generate the four combinations for A and B right, A bar dot B bar A B bar A bar B and A B bar means compliment; so then only one of the combinations is true. So, in this case which combination is true A is 1. So, a this combination is true, where A is 1 and B is 0. So, 0 complement is one. So, 1 dot 1 is equal to 1, 1 and 1 is equal to 1.

So, this particular combination is true. The rest of the combinations are false. Since the rest of the combinations are false, the output that you get 0 0 and 0. For this case if the input, let us consider the input to be x. So, what are we getting? We getting x ended with

a B bar, using the distributive rule. I am sorry using the associative rule, what we can do, if we can replace this is this right, which is equal to x ended with one, which is x.

So, what we can see is, that if this combination is true which is A and B complement, then the output at this point, which is essentially the second and gate; the output of the second and gate, which is chosen by the select bits is equal to the input which is x. So, to summarize what we have essentially the decoder is a block, where we have one input and we have 2 raise to the power n outputs right, and we have n select bits. Based on the value of select bits only one of the outputs shows the value of the input, the rest of the outputs are set to 0. So, we say that that particular output is enabled, and the rest of the outputs are disabled.

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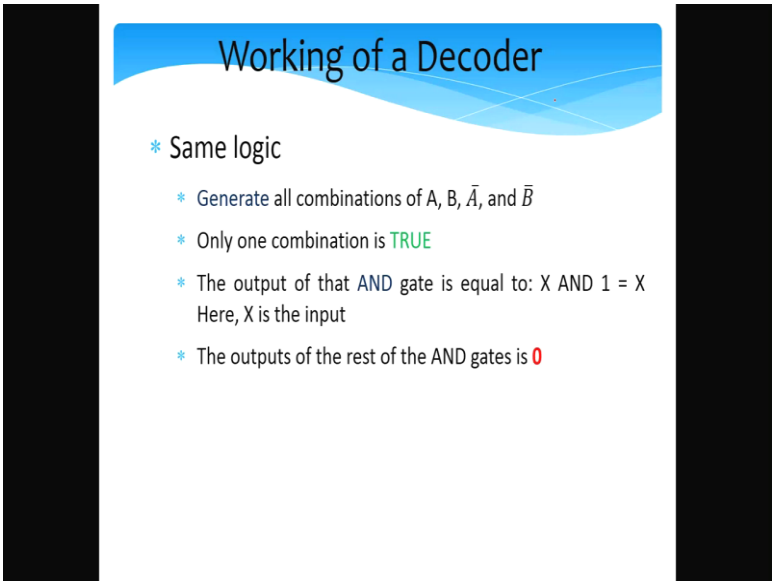

So, this slide again summarizes the working of decoder, which I will just repeat. So, the logic is the same, as the multiplexer which is generate all combinations of a B a compliment and B complement. Only one of the combinations should be true. The output of that and gate, corresponding to that combination will be equal to x ended with one, with excess input. And x and 1 is equal to x, and output of the rest of the and gates will be 0.

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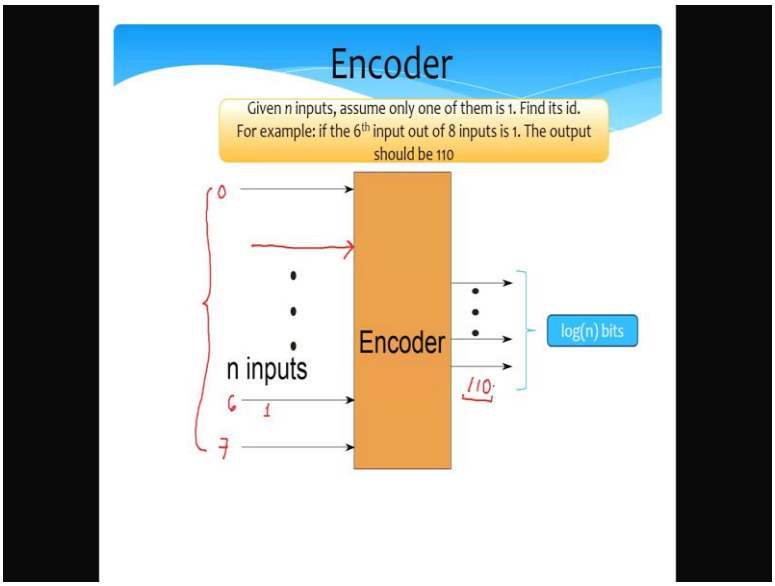

Now, let us consider one more circuit called an encoder. So, the encoder is also very important, it is also very useful in memories. Particularly a certain kind of memories called content associative memories or cam memories. So, the encoder works like this that given n inputs, assume that only one of them is one right. So, this is normal encoder, is something of priority encoder which I tell you what it is, but will not discuss it is design.

So, let us assume that the n inputs, and one of the input is equal to 1 and the rest are 0. So, then the output is will find the id of the input, that which input is one right. So, for example, let us say that inputs are number from 0 till 7, and the sixth inputs is equal to 1, that rest are 0. So, output should indicate which particular input is one. So, the output should be 1 1 0, which is the binary for 6 (Refer time: 55:00).

So, what happens when multiple inputs are 1? When multiple inputs are 1 we need to choose one of them, based on the priority. So, this is called a priority encoder. So, priority encoders can be a many different types, depending upon the priority. So, we will not discuss that, but readers were interested in priority encoders, can consult any other classic text on digital logic. So, we will find many different kinds of priority encoders.

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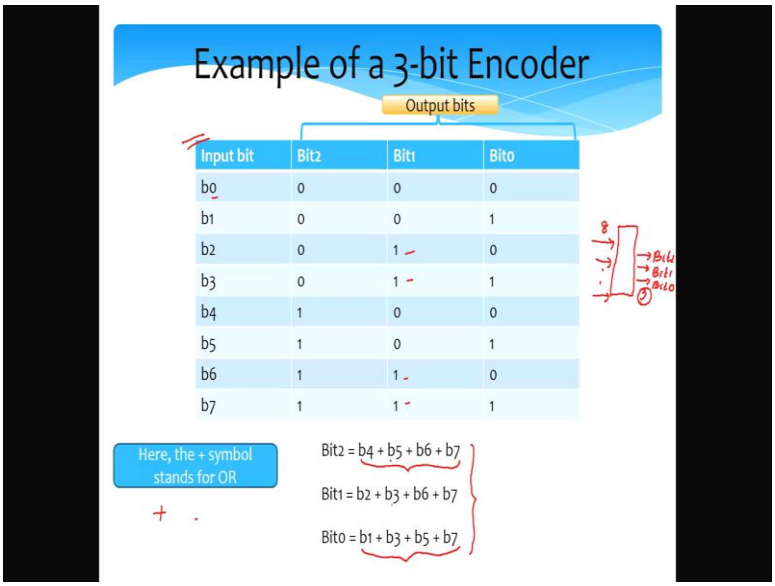

Let us look at designing a three bit encoder. So, if I want to draw the circuit of encoder this is what it would look like. I am sorry not a circuit a high level diagram. So, I have in the case of a three bit encoder, I have eight inputs, and I have three outputs. So, one of the inputs is equal to 1, and I need to find out which input it is. And then encode the number of that input in binary. So, if you think about it, let the input bits B number B 0 to B 7, and let us consider three output bits. So, let us call them bit two, bit one and bit 0.

So, as we can see, if bit 0 is equal to 1, output needs to be 0 0 0. Similarly for B b 1 the output needs to be 0 0 1. So, essentially the binary encoding are 1. Similarly for B 5 it will be 1 0 1, and B 7, it will be 1 1 1. So, what we can do is that for bit two we can write a Boolean equation, to denote that when the bit is true, depending upon the values of the input bits. So, let us use the plus symbol to stand for or. So, recall that we will use plus for or, and dot for. So, in this particular case the second bit, is equal to, because the second bit when is it true, when either B 4 or B 5 or B 6 or B 7 is true. So, this is the logical expression, for when bit 2 is true.

Similarly, we take a look at bit one when is it true, it is true when B 2 and B 3 sorry B 2 or B 3 are 1 or B 6 or B 7 are 1. So, we can say it is B 2 or B 3 or B 6 or B 7; that is when bit 1 is 1, in the rest of the cases the default we will switches 0 similarly for bit 0. So, bit 0 denotes the unit, the least significant position of the binary number. So, bit 0 is true if either B 1 is true, or B 3 is true or B 5 or B 7. So, this is a Boolean equation of bit

0. So, all that we need to do is, that the Boolean equations that we have over here, we need to implement them at logic gates, and we are all done and for a 4 bit or a 5 bit encoder, the logic will change in a similar manner. So, we need to make a table as shown over here. So, we me need to make this table once again, and for each output bit we need to find out for which inputs it said to one, right appropriate Boolean equations and implement them.

So, let us consider the circuit of a three bit encoder, it just has three or gates, and the see if you see the equations here. The equations here show that we are taking an or of four quantities of 4 bits.

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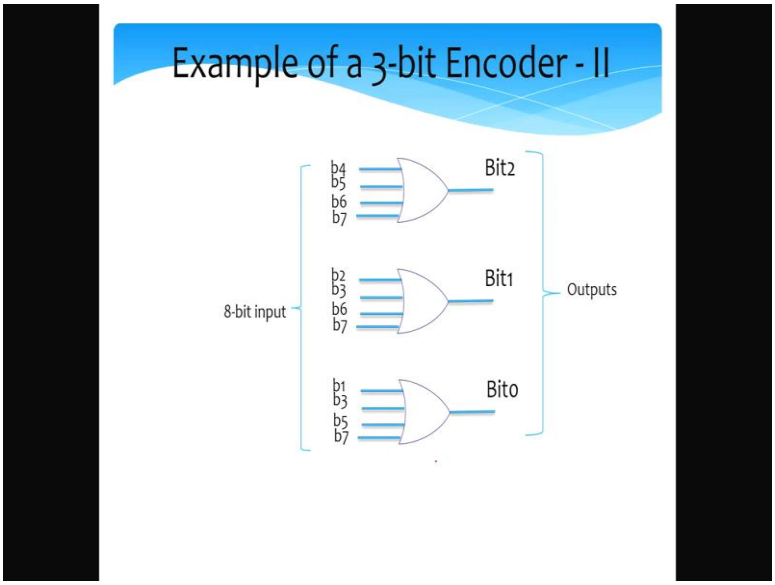

So, each or gate has four inputs and the inputs vary depending upon which output bit is corresponds to. So, bit 2 is B 4 or B 5 or B 6 or B 7. Similarly bit one and bit 0 the circuits are determine the equations on the previous slide. So, this is fairly simple circuit all that we need is three four input or gates. So, 4 bit and 5 bit encoder are slightly more complicated in the sense within or gates, even more inputs, this is the basic idea. Subsequently, we will take a look at sequential logic.

So, that will be there in the next lecture. In the next lecture the idea is to cover sequential logic and memory cells.