Fundamentals of Micro and Nanofabrication
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Lecture – 61
CMOS process for photonics application

In this lecture, we will look at a case study of how to use the unit processes that were discussed throughout the lecture and use them for some applications. In this case, we are going to exploit CMOS compatible fabrication processes for silicon photonics. We will look at CMOS process flows and key technology steps required realizing a silicon photonics application.

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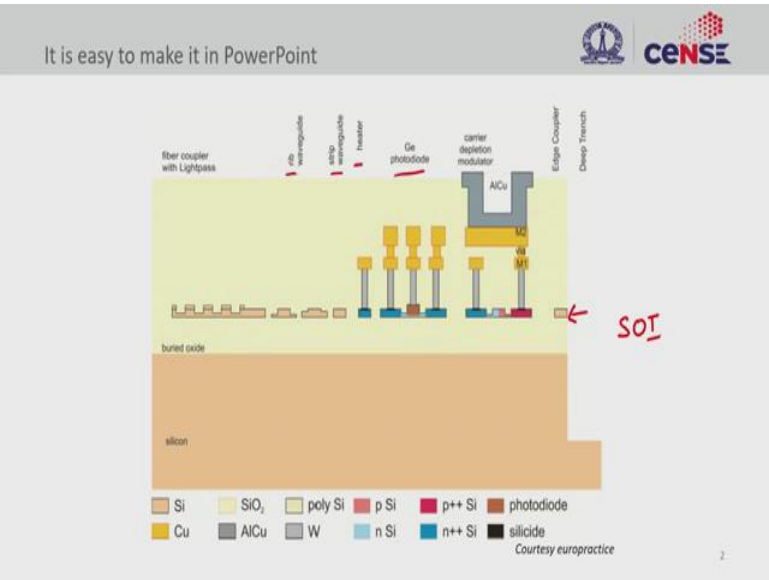

The above image shows a cross-section cartoon of a photonic integrated circuit on a silicon on insulator (SOI) platform. In an SOI, we have an active device in one layer. The device silicon layer is etched or doped, or integrated with new material and metallization for contacts to realize various functionality. In this lecture, we will look at various processes to realize this on a wafer.

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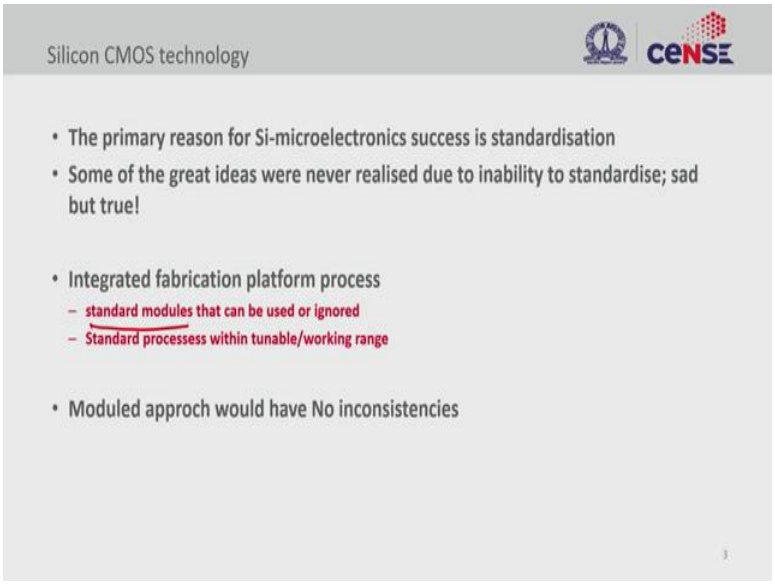

The primary reason for the success of the silicon microelectronic process is its standardization. So, it is important to standardize and modulize by adding various Lego blocks or various process modules to realize desired functionalities. Without standardizing the process, we cannot realize a great idea that involves large volume fabrication.

In a standard integrated fabrication platform, we use a standard platform and modules. So, the standard processes should be within the tuning range, for example, if a standard process module gives a line width variation of about 5 percentage. Still, if the requirement is 0.5 percentage, then it is impossible to realize the required design, it should be in the workable range of the standard process.

We should make sure that the module is with no inconsistencies in realizing the required process.

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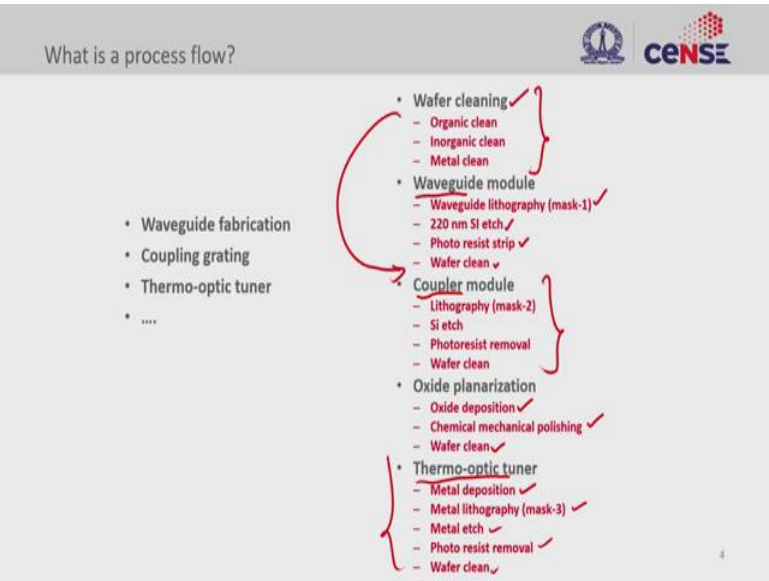

A simple process flow involves various modules. For example, a wafer cleaning module would include organic clean, inorganic clean, metal clean. All this is encompassed in one cleaning module. So, we call this a cleaning module. A waveguide module includes a lithography step, etch step, removal of a photoresist, and then a cleaning step. So, after the waveguide module, there is a coupler module, a device module that includes lithography, etching, photoresist removal, and cleaning step.

Next, we have a planarization module consisting of deposition step, polishing to make the wafer flat, and then wafer cleaning. A thermo-optic tuner or some metal heater module starts with metal deposition, followed by lithography, metal etching, photoresist removal, and cleaning. This module can be used in any device fabrication, which includes a thermo-optic tuner or a metal heater.

We can take a particular module and then place it wherever we want based on the requirement from the designer side. For example, a wafer cleaning module can be included in between processes to make sure the transition between one module to the other module is all contamination or cross-contamination free.

A discrete module is a collection of complete unit steps in itself. Modules created should be reusable so that it can be adapted for the desired application. We will look at each of these processes and all the requirements within each module.

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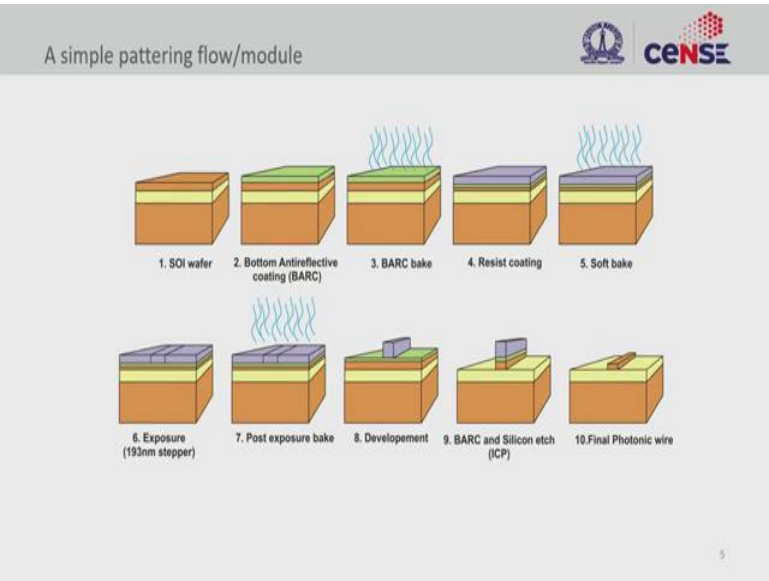

An engineer would make a flow cartoon to visualize a process, as shown in the above slide. We start with clean silicon on the insulator wafer; we coat it with a bottom anti-reflective coating and bake it. Then we do a photoresist coating followed by a soft bake; this is a pre-exposure bake. The baked photoresist is then exposed by illuminating the required design onto the photoresist, and after that, we do a post-exposure bake. The wafer is then developed to remove unexposed or exposed regions depending on the resist's tone (negative resist or positive resist). After the development, we do ICP etching. During inductively coupled plasma reactive ion etching, we remove the silicon layer exposed and then remove the photoresist to end up with a simple silicon wire.

The process flow gives a very natural way of visualizing the process. If we encounter any issues while making this process flow, we can go back and look at the developed process flow and address those issues.

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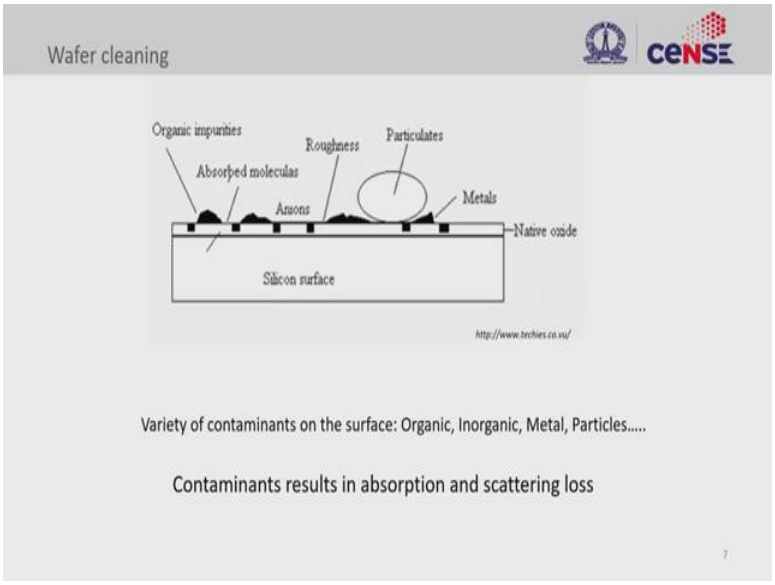

Once the process flow is ready, then we start doing individual process modules.

In the photonic application, wafer cleaning is important to remove the contaminants, resulting in absorption and scattering of light. Cleaning is done to make sure the wafer is clean from any particle contamination, metal contamination, or ion contamination, including organic contaminants.

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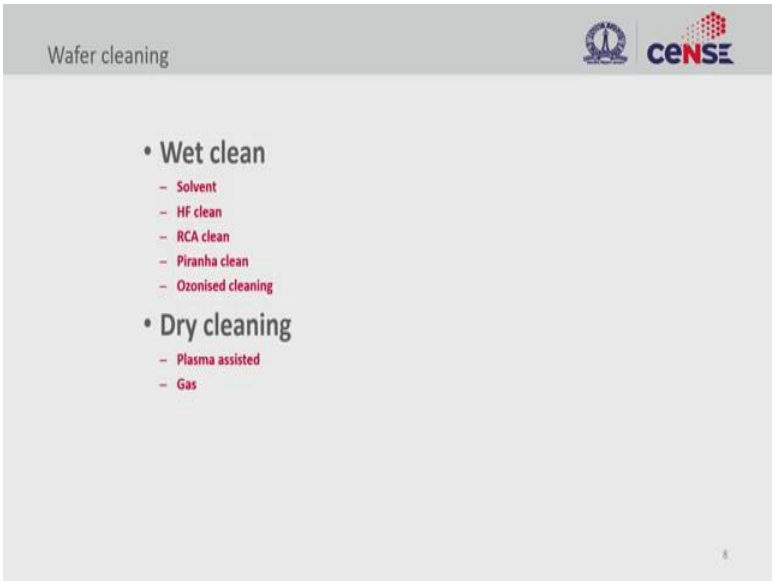

We can either do wet cleaning or dry cleaning. Wet cleaning involves solvent, HF or RCA clean, piranha clean, or ozonized clean as well. In dry clean, we can use plasma directly or any gasses that can etch away the substrate.

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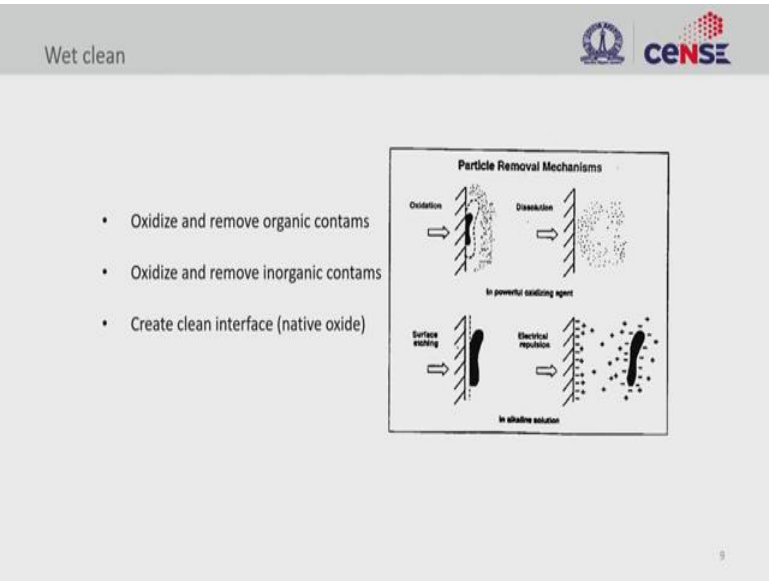

The mechanism involved in cleaning is primarily to oxidize the contaminants or the underlying substrate and then remove the contamination similar to lift-off. A thin layer of native oxide is formed during the process to protect the substrate from further attack from any contaminants.

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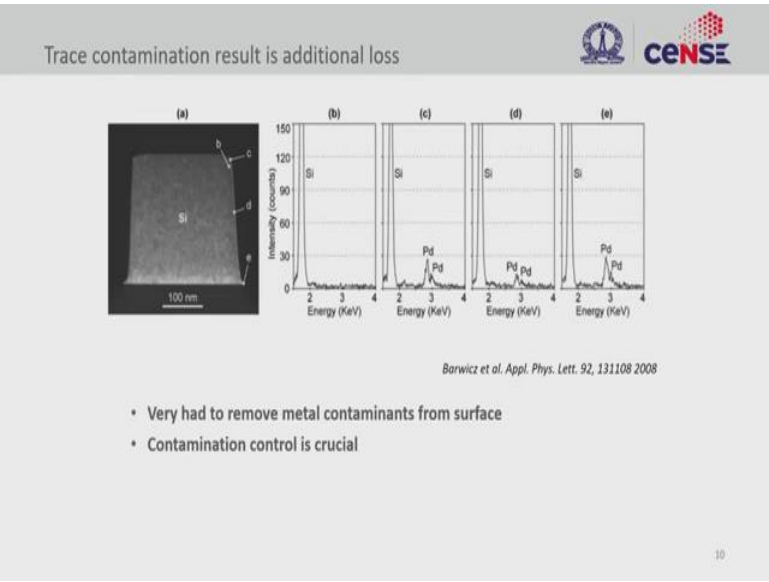

Even a clean substrate can still have trace amounts of metal. If the substrate is exposed to any beaker during cleaning, then the contamination on that particular glassware will transfer to the substrate, and it is difficult to remove it. And this can be very specific to the position on the wafer or on the structure itself if the cleaning step is after dry etching. The above image shows a cross-section of the waveguide; there are no contaminants at position b, but at position e, there is increased metal contamination. So, one needs to be sure about the distribution of contamination on the wafer and the structure that one prepares. So, once it is clean, the next step is lithography.

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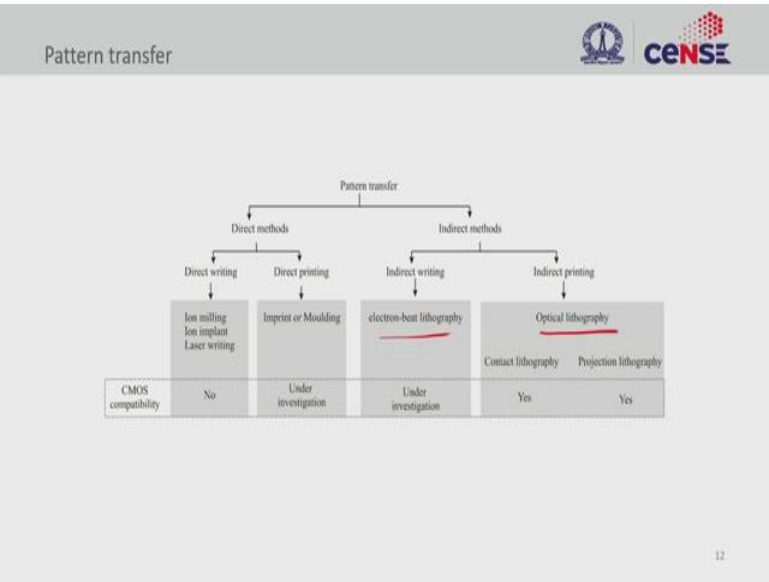

There are various lithography that was discussed in the earlier lectures. Primarily optical lithography or electron beam lithography is used in academic research, and optical lithography is used in industrial-scale processes. In this case, we are going to use optical projection litho for patterning the structures.

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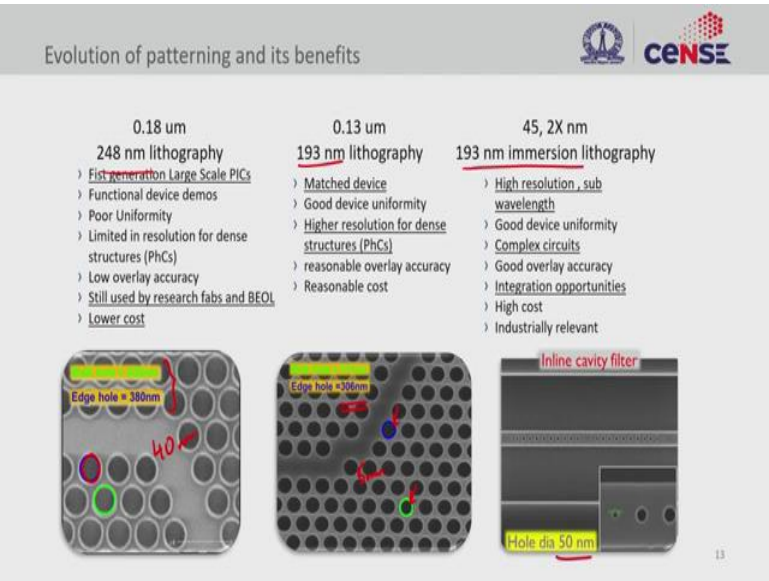

The above slide shows the evolution starting from 0.18 micron to 0.13 micron, and in the present day, we have 45 nanometers or 22-nanometer node technology. The lithography technology uses the wavelength of 248, 193, and 193 immersion. The 0.18-micron technology gives a pretty good patterning, but the effect of proximity comes in to picture.

If we compare holes at different positions, there is a 40-nanometer difference between the holes on the edges and holes at the bulk. And, in the next-generation technology that is used for the 130-nanometer node, we can see the reduction in the variation (reduced to about 5 nanometers). So, we see an order of magnitude improvement when we go from one technology node to another technology node. So, this brings us to the technology selection itself. So, what is the requirement? What is the final structure should look like? What is the specification on the overall device and within the device as well? In the above case, there is a within device variation, which is addressed by going to advanced technology.

If you look at 45 nanometer and 20 and below nanometer technology node, we can pattern really small features. This opens up new avenues for integration and advanced devices. So, it is not just about resolution; it is all about uniformity and adaptability of this technology to come up with new innovative ideas. The patterning is evolving, at the

same time, what is our requirement and how do we choose a technology also plays an important role.

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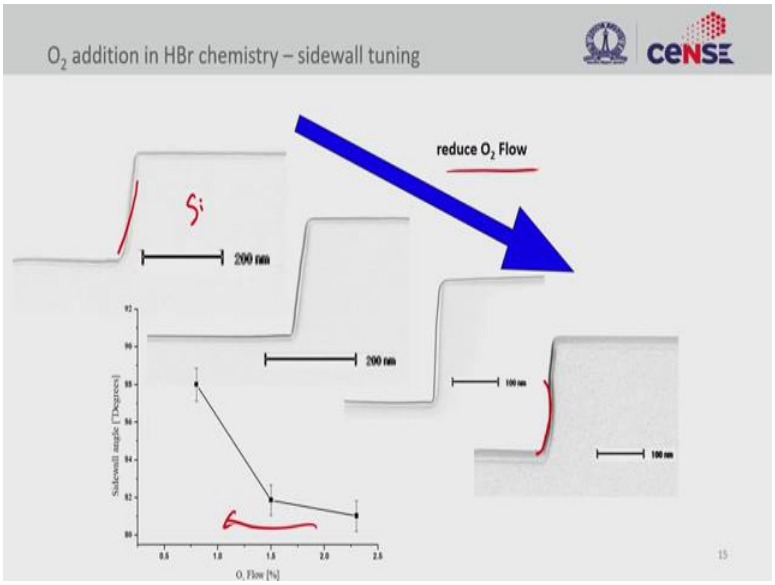

After device patterning, next is to etch the device using dry etch. In dry etch etch chemistry is important , for example to etch silicon in the HBr and O_2 is used. Cross-sectional image of above slie shows that with change in etch chemistry, i.e., reduction in oxygen flow, a positive slope will change to a negative slope. This is how one can optimize the etch chemistry.

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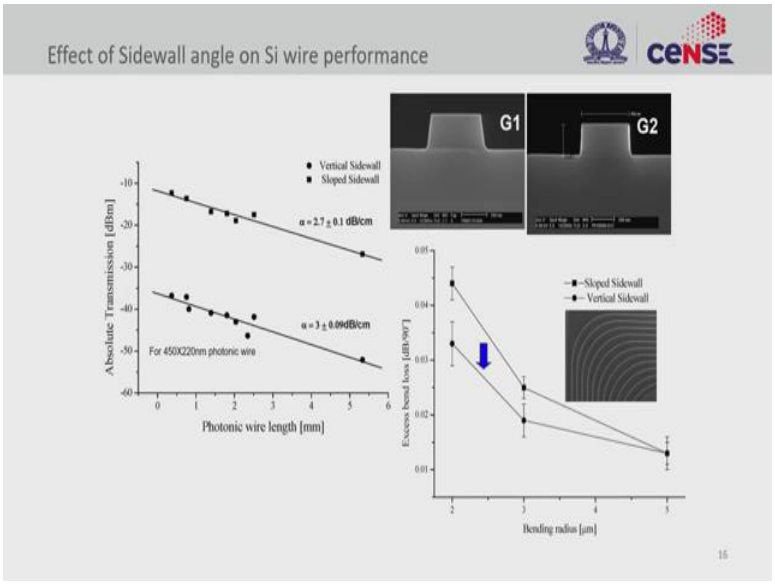

The chemistry change not only affects the profile but also affects the performance of the device. In the above slide, we see two different kinds of etch– one is with vertical sidewall and the other is with slope sidewall. The propagation loss alpha in a vertical sidewall gives 3 dB per centimeter (about 50 percentage loss), but with the sloped sidewall, the loss is less.

The reason for that is when we have a sloped sidewall; a polymer layer will be coated; that protects the sidewall, but it is less protected in the case of the vertical sidewall. So, we will see a plasma attack leading to scattering loss in the case of the vertical sidewall. But bending loss is higher in the case of sloped sidewall geometry compared to a vertical sidewall geometry.

Hence shows that the profile also affects the performance. It can be a device that is of electrical nature or optical nature, or electromechanical in nature, but the profiles will have a certain influence on the performance as well.

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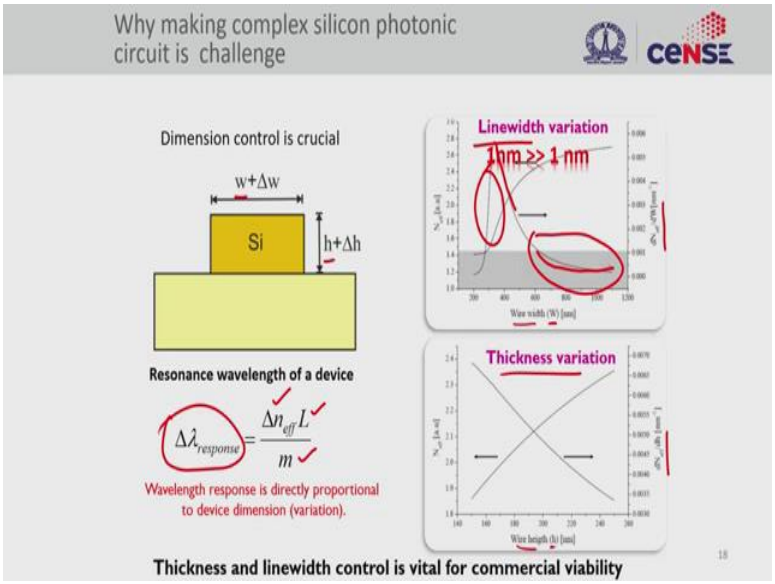

The next thing is about variability. So, once we have etched all these centers, let us look at how the variability is going to affect them. So, this is something that we would like to elaborate on where the variability, either width or height variability, will directly affect the performance. In this case, we are looking at the resonance of a certain device which depends on the density of the material and the optical path length L.

So, the length of the device and the density of the device will affect the device response. The above slide shows the line width variation (Δw) and thickness variation (Δh)as a function of waveguide width or waveguide height. The variations dN/dW and dN/dh are high close to the operating point; hence the slope is high.

So, we want to make sure that the operating point is chosen so that the variation is taken care of. So, for instance, in this case, you want the slope to be rather flat; when the slope is very sharp, nanometer variation could result in a nanometer variation in the performance, which we want to avoid. So, all the processes should be controlled to get uniform distribution.

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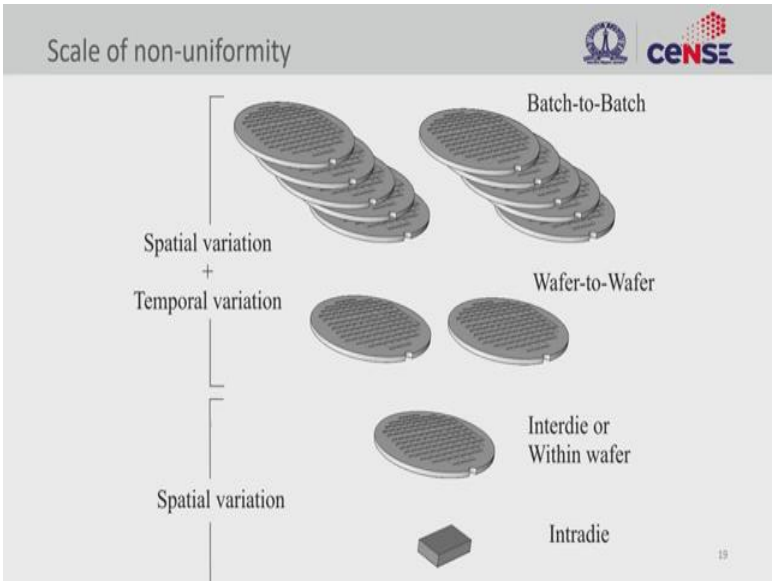

So, the variation can be of multiple nature. So, we could have a spatial variation or could have spatial and temporal variation. So, this depends on whether we are processing a single die or multiple wafers. So, depending on the scale of manufacturing or fabrication, the variation will also scale.

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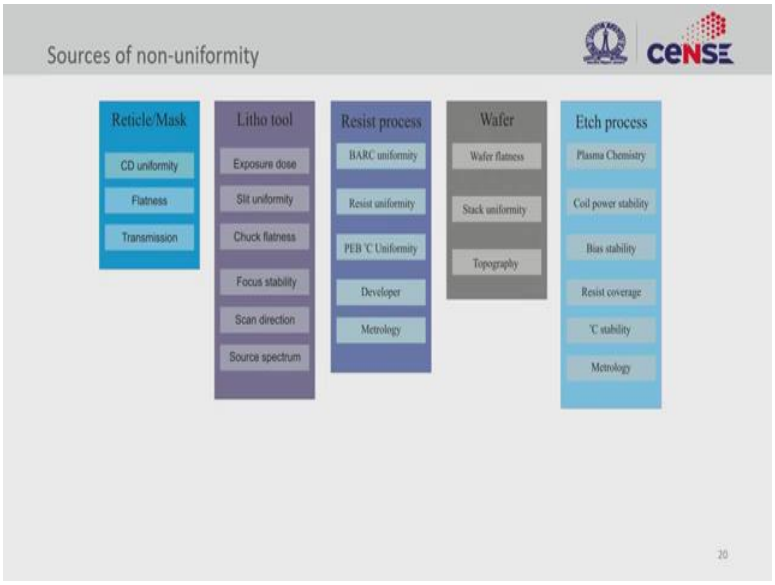

So, the variation can come from any process that we are using. So, one should be aware of each step that will add non-uniformity and variability. We should try to reduce the number of process steps and collate the process steps to make an efficient process flow that will reduce the non-uniformity.

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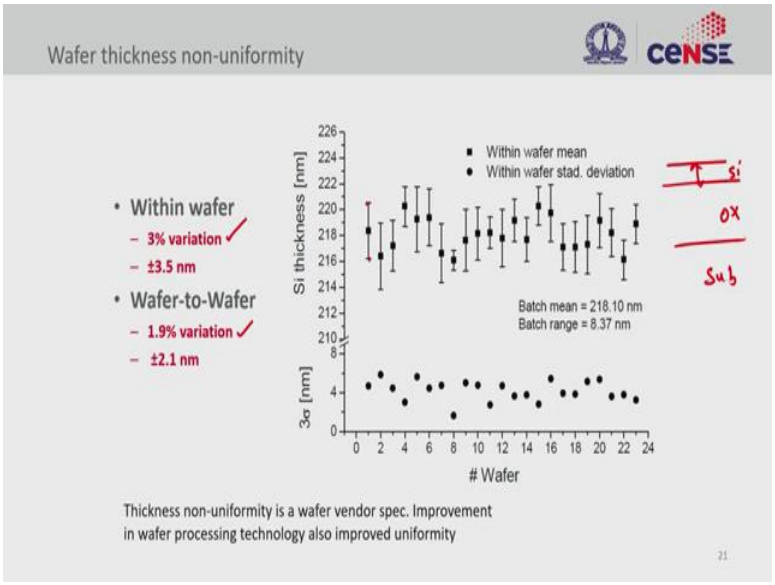

The non-uniformity may or may not come from the processing that we are doing. It may come from the substrate itself. Here we see the thickness variation of silicon in a silicon-on-insulator substrate. We see the thickness variation of the top silicon layer with

different wafers and within a wafer. In the slide, we can see that we have about a 4-nanometer variation within a wafer, but the variation could be much smaller between wafer and wafer.

There is a within wafer variation of 3 percentage; however, wafer to wafer variation is about 2 percentage. So, it is less than within wafer variation. So, when we process multiple wafers and multiple batches, the variation can be not just come from the process, it can be from your starting wafer itself. So, this is something one should be aware of.

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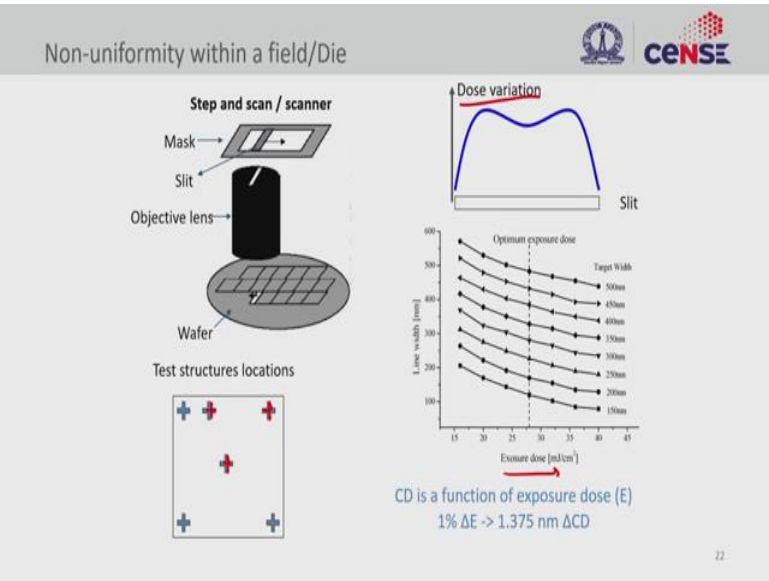

The lithography step can also bring in non-uniformity. This we had already discussed. The position of the device within the chip can also play a role because of non-uniformity in the dosage during illumination across the die. The device can have various line widths; this can have variations in line width as well.

The placement of the device is also crucial. So, we should be aware of the placement-related non-uniformity while considering the circuitry's global uniformity.

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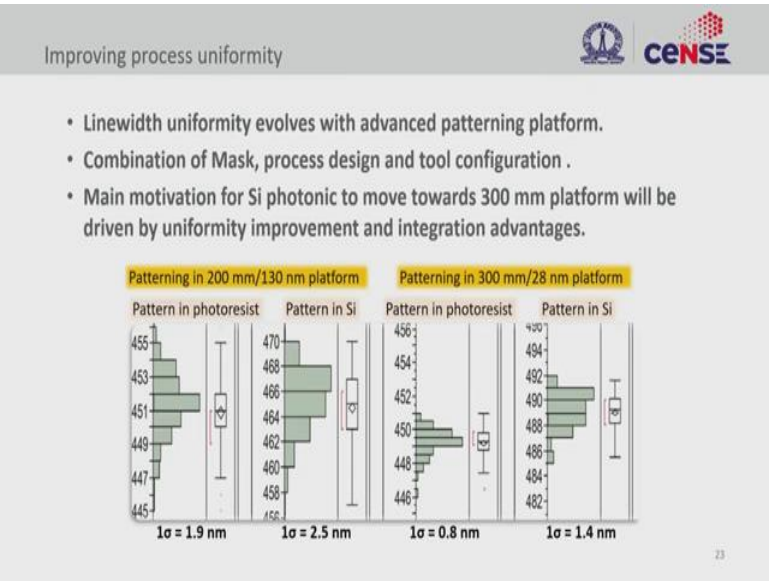

And, this also helps when you go from you know different types of patterning platforms. The above slide shows the comparison between the 130-nanometer node and 28-nanometer node platform. When we look at patterning accuracy, the spread right i.e., 1 sigma (standard deviation), is 2.5 nanometer in silicon for 130 nm platform. In contrast, for a high-end technology (28 nm), it becomes 1.4 nanometer which is almost half. This reduction comes from superiority in the patterning technology itself.

So, when we go from one process technology to another processing technology, non-uniformity will reduce. So, it is important to modularize all the processes to get the maximum out of each module.

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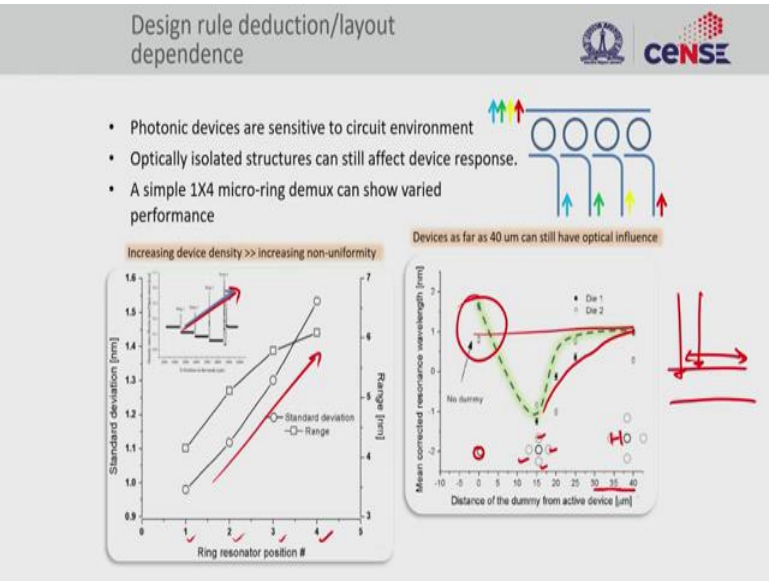

Another important thing is variability as a function of space. The above slide shows the spatial variation in a single device and device surrounded by dummy features. And there is a distance variation that we are giving here between the active and dummy devices. The presence or absence of dummy structures will affect the device response. The distance of dummy structures from the device will also affect the device's performance, as shown in the graph above. The graphs show that even when the dummy and the active device 30 – 40 microns apart, they can influence each other. So, this influence is coming from the wafer scale, plasma processes that we are doing. When the radicals come onto the wafer surface in the plasma process, the radicals can migrate based on the energy and substrate temperature. So, based on this, it can diffuse on the surface and this diffusion length can also affect the neighboring device uniformity. For example, there are four different types of devices, and based on the density, when density increases and performance is affected. The device response is correlated with the density of the device around. So, it is not just the device we are interested in, but also the environment.

We should make sure we control the environment so that there is a uniformity across the wafer or across the designed chip that these variations are taken care of.

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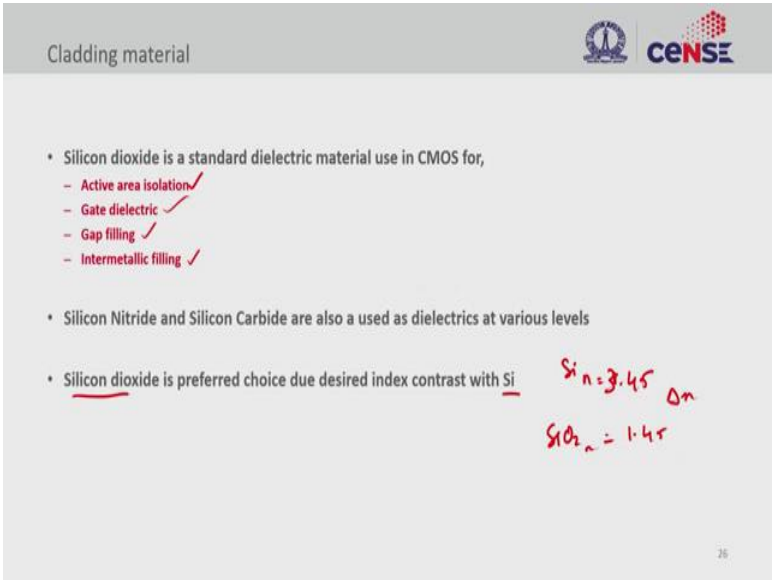

The next important thing is cladding, a coating on top of the device to protect the device. Normally silicon dioxide is used as a typical cladding or coating material, which is used in multiple places. Silicon dioxide is used as active area isolation in gate dielectric, gap filling, and intermetallic filling. So, we can also use nitride, carbides for example, and we can also use silicon dioxide for various other applications.

We use silicon dioxide because it goes very well with silicon as the optical contrast (Δn) between these two materials is high (the refractive index of silicon is 3.45, and silicon dioxide is 1.45). Silicon dioxide is chosen because of its non-absorbing property and low refractive index.

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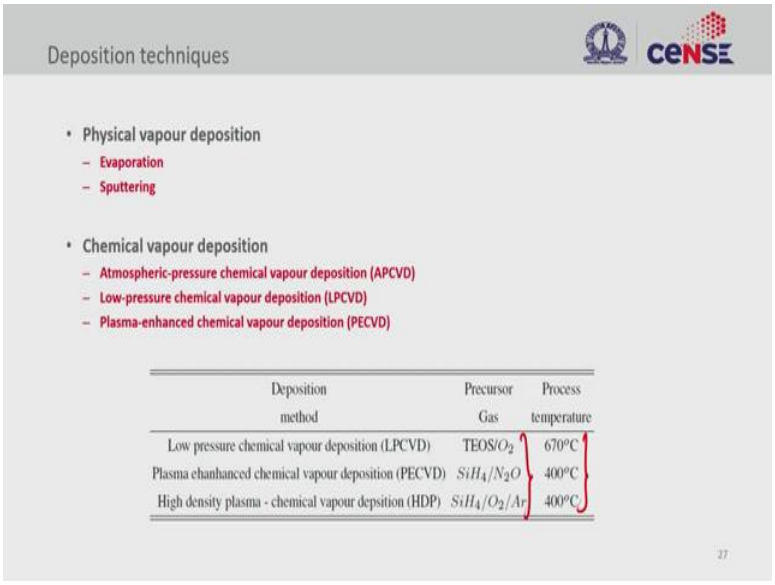

There are multiple ways to deposit silicon dioxide. We can use evaporation or sputtering or a CVD technique, either atmospheric pressure CVD, low-pressure CVD, or plasma-enhanced CVD, to deposit silicon dioxide. The slide shows the list of CVD processes with varying precursor gases and processing temperatures. If we already have metal underneath, we cannot use LPCVD; we rely on the PECVD or HDP process.

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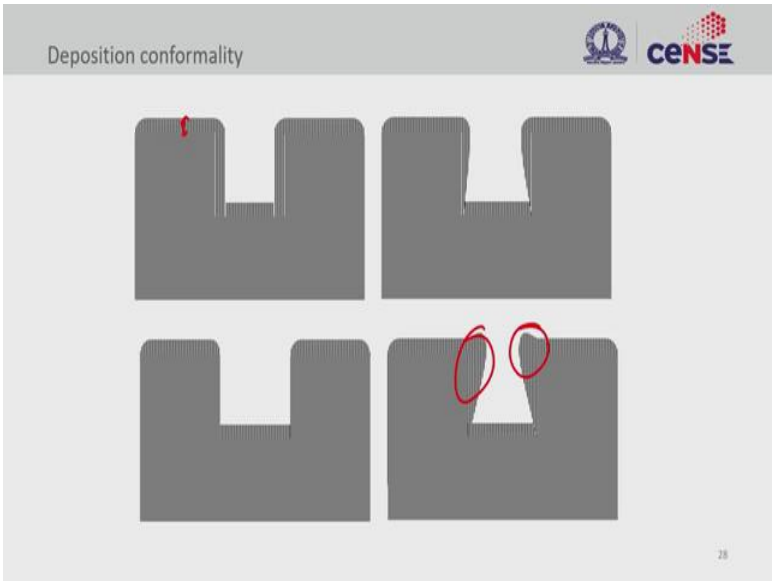

The deposition process can be either conformal or non-conformal. So, if it is conformal, the thickness will be uniform, but during non-conformal, there will be an overgrowth of the edges as shown in the figure above.

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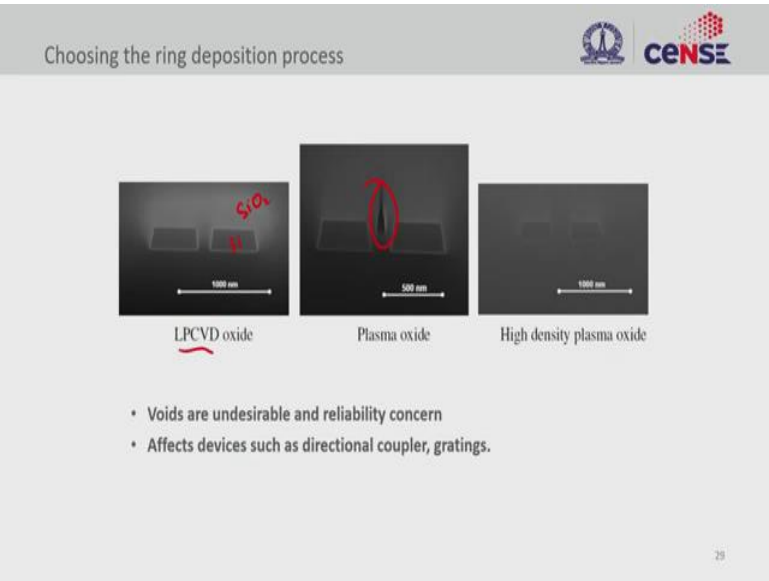

LPCVD process is a conformal process, and we don't see any gap between the two silicon regions after silicon dioxide deposition, as shown in the figure above. However, in a plasma process, we see a gap formed because growth at the two ends is closing, and then it creates a gap here. However, the high-density plasma oxide process will not create a gap.

So, the choice of the deposition process is important, not just the choice of material, but also the kind of process that one needs to choose to realize certain kind of device geometry that we have.

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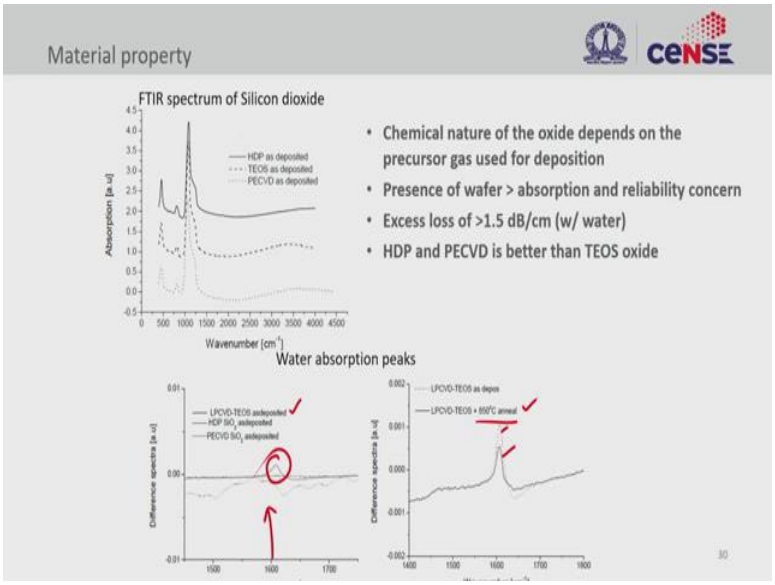

The above slide shows the FTIR spectrum of silicon dioxide material deposited with three different techniques: high-density plasma CVD, plasma-enhanced CVD, and the TEOS-based or LPCVD process. Since the LPCVD process happens at higher temperatures, deposited material shows low absorption at 1600 compared to PECVD and HDP processes; it corresponds to water absorption. However, see as-deposited film shows a small coming from the water that is present in TEOS material unlike the other materials, we do not have any water absorption at all. Even after annealing at high temperature, there is still some water vapor peak present. Post anneal on cooling, water can diffuses in, and then it will occupy the space that is available inside this oxide material deposited with LPCVD. This shows that it is not just any technique we should also be careful about, but also the precursors we are using. Though LPCVD happens at high temperatures and we are also annealing at high temperatures, but then at the end, the TEOS as a material is not suitable for some of the applications because of water absorption.

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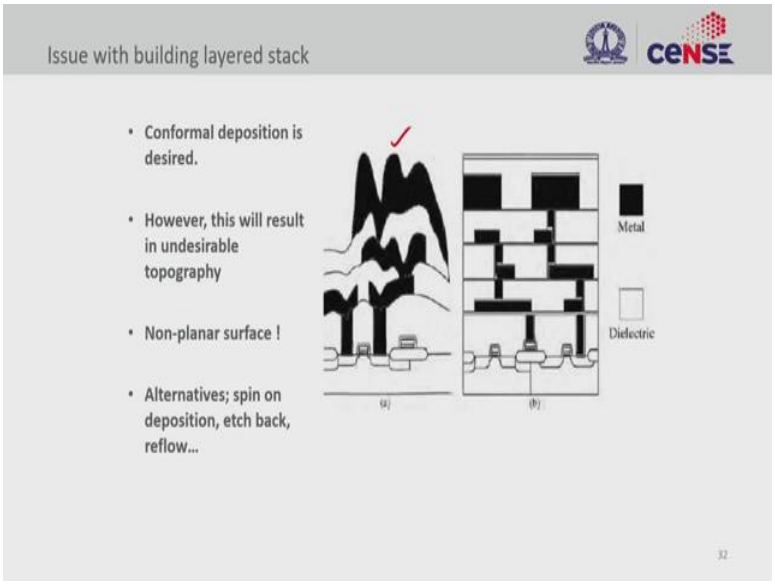

The next process is planarization. After film deposition, we do CMP or chemical mechanical polishing to planarize the layer to remove unwanted thickness variation and reliability issues.

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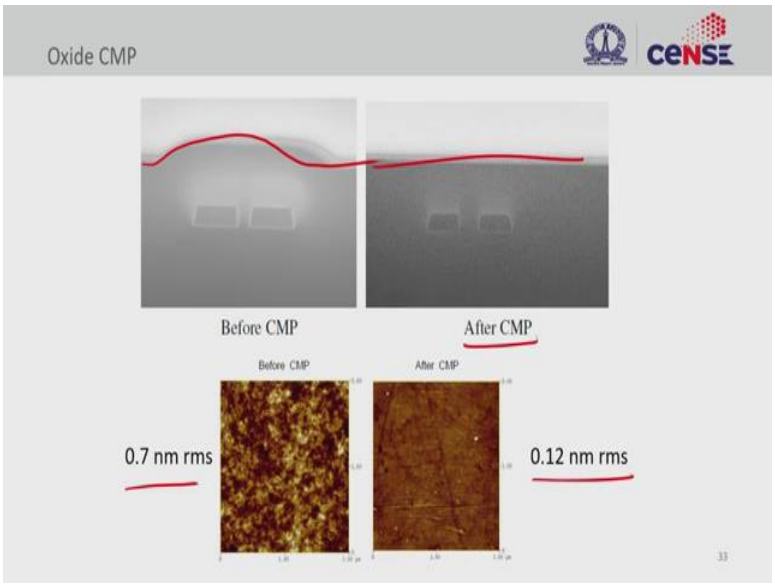

AFM is carried out before and after CMP to confirm the planarization. Before CMP shows topography indicating a conformal deposition, and post-CMP shows a flat line as required. On comparing the roughness, deposited films show the roughness of 0.7-

nanometer rms, but after polishing, it is 0.12-nanometer rms. So, it is not just getting a flat wafer; it is also about creating smooth surfaces.

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The final step is metallization. After obtaining flat oxide, we follow lithography and etching steps to make the trenches. These trenches are filled with metal deposition followed by CMP to remove the metal in the non-trench regions.

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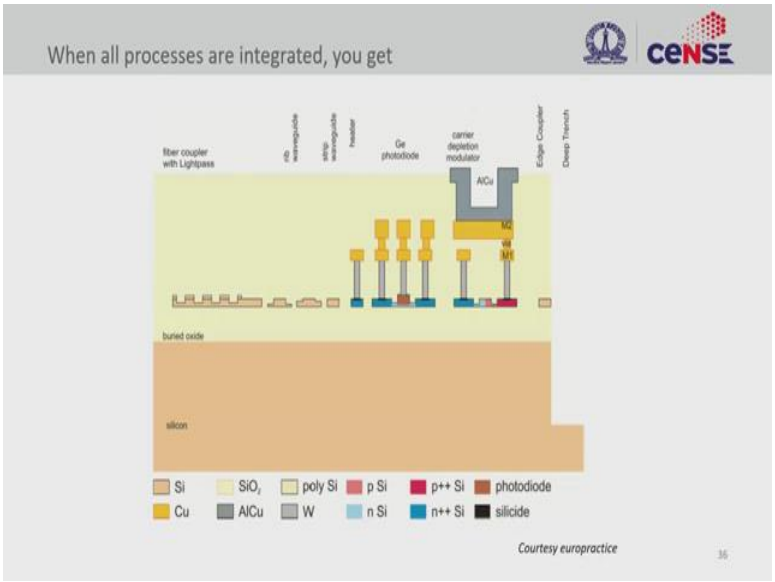

On repeating this process, we can build complex structures, which should result in the desired structure as shown in the above cross-section image.

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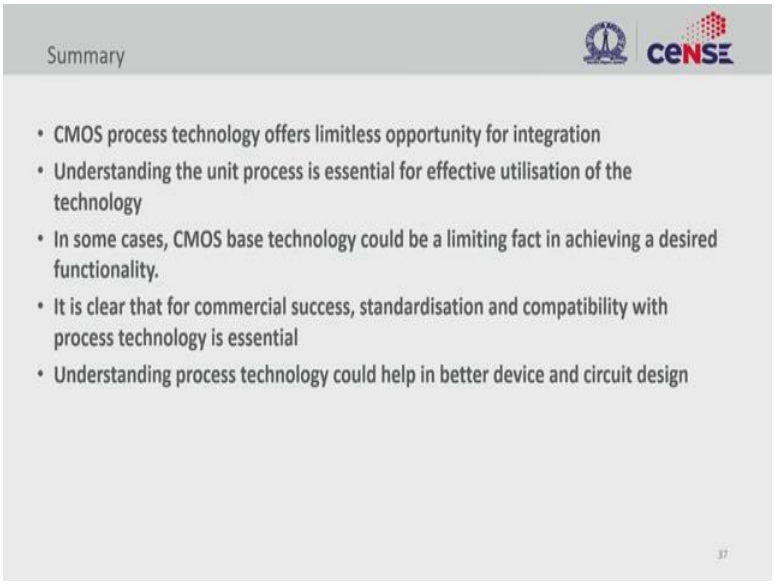

With this, we come to the end of this lecture, where we have seen the CMOS technology offers a lot of integration opportunities. The main reason for this is we create modules out of each unit process, and we make sure these modules can be used wherever we want right and arrange it the way that we want in order to realize the cross-section that we want. And, to get these modules right, one should understand the unit process so that one can utilize the technology effectively.

Some of the processes may be limited; that could be the limit of what we can get out of this CMOS technology. We may add additional modules to achieve the desired device, but we should always try to standardize any modules you would like to pursue.

And, as we mentioned earlier, if we want to make any commercial success, the process should be standardized and compatible with the process technology. So, we should be able to stack all these standardized modules to realize the end goal. So, as I mentioned, understanding is crucial here. We should understand the unit process, and we should understand what each module will deliver. So, once we understand, we can realize better device and circuit designs.