Fundamentals of Micro and Nanofabrication
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Lecture – 57
PV integration

In this lecture, we will discuss an example of a successfully integrated product, silicon solar cells. It is unique and is very different from the typical semiconductor fabrication systems like CMOS or BiCMOS. I wanted to give you a flavor of process integration and highlight the importance of the low-cost and throughput in integration that traditionally has been costly. Silicon solar cells have made remarkable progress or have helped make noteworthy progress in making microfabrication cheap.

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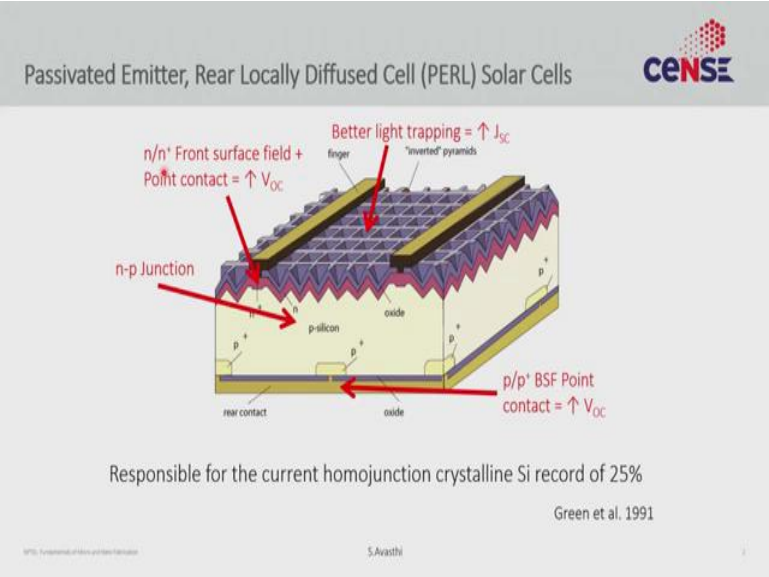

We will not discuss solar cell physics; for this lecture, they fundamentally diode or p-n junctions optimized to harvest energy from light. Typically, one contact is semi-transparent, completely transparent, or has a metal grid that allows light to enter the cell so silicon can absorb it. A photon generates an electron and hole. The efficiency depends on how many of these carriers you can extract before recombination within the cell. They can recombine in bulk or at the surface. An efficient solar cell reduces recombination losses. We start with what you get at the end of a solar cell physics course; the most

efficient silicon solar cell structure we can make with silicon homo-junction (without using any other semiconducting material).

It looks slightly different. Notice these inverted pyramids. The surface is not flat. These metal fingers collect the charges, but they are reflective. So, you don't put a blanket metal layer. You require some metal to extract the current, but it typically covers < 5 % of the surface. We start with a p-type substrate. The red film represents an n-type material. This p-n junction is responsible for separating carriers and creating energy from light. There is another junction: p^+-p, highly doped p-type, and moderately doped p-type junction. It helps reduce interface carrier recombination. The physics behind it is not relevant here.

You can restrict the area where recombination can happen to reduce recombination losses. This blue film is SiO_2, an insulator, but more importantly, a great passivator. At the interface between the oxide and the silicon, there is negligible recombination. The only place the recombination can occur is the rear silicon-metal contact. You want that area to be small but can't make it arbitrarily small because you need it to extract the current. So, you have optimally located points where you can collect the carriers.

Suppose you are in the PI-team in charge of making it and have all the dimensions and details. How would you go about fabricating the cell? We know how to select a substrate and make a p-n junction. We start with a p-type substrate and diffuse in n-type dopants. There are two diffusion layers, n^+ and n layer. You create a moderately doped layer through diffusion and do a second diffusion for a highly doped layer using a different pattern. We probably need to do lithography in the middle. You make the inverted pyramids using anisotropic silicon etching. In basic etchant like KOH, as you etch silicon (100), you get (111) facets at an angle around 54-56^o with the surface. So, you have these pyramids at 56^o on the top. For the back p^+, you have another lithography step to open holes in this oxide and diffuse a p-type dopant. Then you deposit the metal on the back and the front. That is one more litho step to define the metal pattern on the top. It is very close to how the people who made this cell did it.

However, the problem is there are too many steps. When you make millions of solar cells, each step counts in terms of time and resources allocated - chemicals, workforce, equipment, consumables, etcetera. You want to reduce the number of steps and be very

efficient in how to do them. This process is similar to what you would use in micro and nanofabrication of logic, such as Intel and AMD processors. But it is expensive. Intel reduces cost by scaling down, but solar cells can't. If anything, you want to make a larger solar cell that can capture more light. The solar cell industry went in a different direction than Intel, AMD, and other CMOS technology to reduce cost. They don't have to do things at the nanoscale; they work at millimeter-scale or hundreds of micron-scale. So, they can gain a lot in cost and processing efficiency by ignoring finer aspects. Today, silicon solar cells are at par in terms of price with traditional sources of energy. It is cheaper to install a new silicon solar cell plant than a new coal power plant, which is a remarkable change. This lecture explores those innovations.

To summarize the device structure, we have a p-n junction and an n-n^+ contact. The pyramid structures help in trapping the light that would reflect from smooth surfaces. Similarly, a back p-p^+ contact reduces the surface recombination. This cell has a record efficiency of ~ 25.4 %. Since then, the silicon solar cell efficiencies have increased to > 26 %, but they use heterojunction, which we shall not cover in this course.

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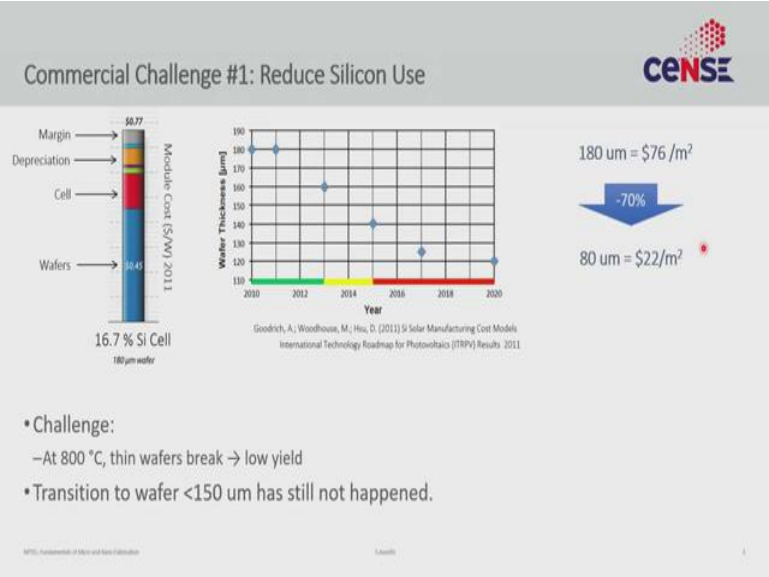

If you want to make it cost-effective, look at the cost structure. Understand where the bulk of the money goes, and zero in on reducing that expense. This bar represents the cost of a module in 2011. The solar cell prices have fallen 80 % since then. So, don't look at the absolute numbers; look at the distribution. The highest cost is not the profit

margin or making of the cell; it is the wafer. It is not surprising, as we have discussed how hard it is to make ultra-pure silicon, how pure the input materials must be, and that adds a considerable cost. You would like to reduce this expensive silicon usage as much as possible, which the industry has tried.

The silicon solar industry has set up an ITPRV roadmap to project the directions they want to go. In 2011, it predicted that they would reduce the wafer thickness as the years progressed, reducing the silicon usage and cost. Unfortunately, despite their best efforts, it did not happen even today. At least in India, no silicon solar cell manufacturer I know uses wafers thinner than 150 µm. They break easily.

In CMOS processing of a 6" wafer, Intel uses 700-800 µm thick wafers. It doesn't want any of them to break. It should go through high or low-temperature processing or rapid thermal processing without developing destructive stress. But that is not an option for the solar industry. The only way they can reduce silicon is by reducing the thickness. So, they settle for 180 µm. It is significantly thinner than what Intel uses, but any more, and they break too many wafers. The cost is one thing, but the yield is essential. The loss of a wafer is far worse than a slightly more expensive process.

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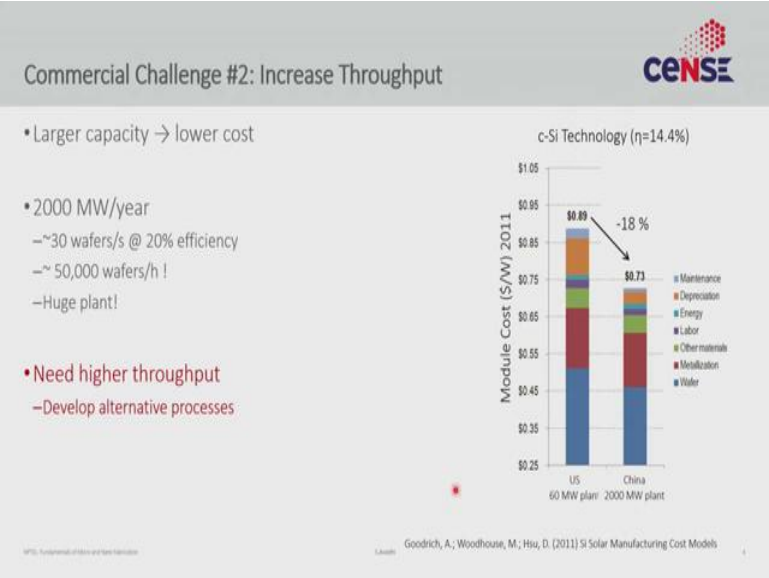

The other commercial challenge is to increase the speed or throughput. How many wafers can you process per second? For CMOS fabrication, they increase throughput by scaling the devices down. So, they can process a lot more devices in one batch. Silicon

solar cells can't scale down. All you can do is expedite the process. In a series of steps, the slowest one decides the production rate. Here are some (old, 2011) numbers from a 60 MW/year US plant, at 89 cents/watt. At that time, other large manufacturers were already producing around 2000 MW, > 30 times! They must have 30 times higher throughput. Some of that came by having a lot more equipment, but a lot of it came by careful optimizations. By sheer volume, they reduced the cost by ~ 20 %, and in a cutthroat market, it makes the difference between a solvent company and a bankrupt one.

How much is this throughput? 2000 MW/year at 20-30 % efficiency and some hours per day, you have a throughput of around 15 wafers/second. That number translates to 50000 wafers an hour. Think of how we do photolithography, recipe optimizing, evaporation, sputtering, dry etching, or ALD. Is it possible to have this kind of throughput? If each step takes an hour, you would need 50000 machines if the throughput is one wafer/hour! The capital expenditure explodes; it is not viable. High throughput is essential in any fabrication, more so in solar cells where scaling is absent.

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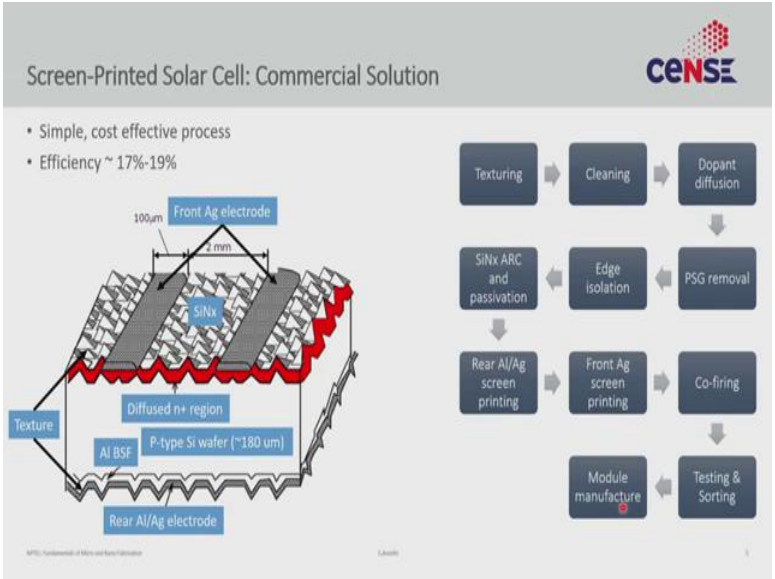

Most of the commercial silicon solar cells have more complicated versions and better technologies. I will discuss only the simple aluminum back surface field screen-printed silicon solar cell. It is a simple, cost-effective process, with efficiency ~ 17-19 % at the cell level and 15-17 % at the module level. We have a p-type wafer (180 μm), thinner than that structure (400 μm) to keep the cost low. A p-n junction is necessary for all solar

cells, but we see only one n-type, no n^+; one less diffusion means cost saving. There is also no p^+ layer, bur an aluminum back surface field (BSF). Aluminum is a group 3 element, and theoretically, a p-type dopant in silicon. Its use is uncommon because it is a little lossy, but here, you want to optimize the cost, and for various reasons, the aluminum BSF is very efficient. Consider it similar to a p^+ layer.

One difference is this p^+ is continuous, while it was only at specific places in that structure. Why is it everywhere? To avoid lithography and save a considerable cost. Unlike inverted pyramids in that structure, we have pyramid-up texture even though it is a little less efficient, as it is easier to produce. You have 100 µm wide metal front electrodes. It is vast as compared to logic and memory, where the critical dimension is ~ 10 nm. As the width is so much larger, the patterning can be more straightforward. We use screen printing, and hence the name, screen printed solar cells.

Here is the process flow: we start with a wafer, do texture, cleaning, dopant diffusion, PSG removal, edge-isolation, Si_3N_4 ARC+passivation, rear, and front-metallization, cofiring, testing, sorting, and finally, manufacture the module. We shall look at each of these steps, one by one, in the next few slides.

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We have discussed CZ silicon solar cells. I have kept a slide on multi-crystalline silicon solar cells. The structure you saw, you can make it using monocrystalline or multi-

crystalline silicon cells. Multi-crystalline is more popular, but monocrystalline is a little more efficient and has become more popular and captured a larger market.

We start with a polysilicon feedstock, put it in the square-shaped crucible of refractory material like Al_2O_3, and put that in a furnace (probably) under vacuum, and do fractional crystallization. Melt the silicon and cool it down in a controlled fashion. There is no seed crystal, rotation, or slow pulling. You don't get a single crystalline but a multi-crystalline wafer. With some optimization, you can get large grains, as large as mm or cm. In general, the most common type of wafer is p-type. So, during this process, you add p-type dopants. The most popular wafer size is 6", or 150 mm. So, you cut this ingot into these cuboids with a 150 mm cross-section. Now, you need to slice them into wafers by wire sawing. You see the rollers, and these shiny wires, thin steel wires impregnated with diamond. You mount the ingots on a holder and push down onto these wires and slowly cut into slices that become silicon wafers.

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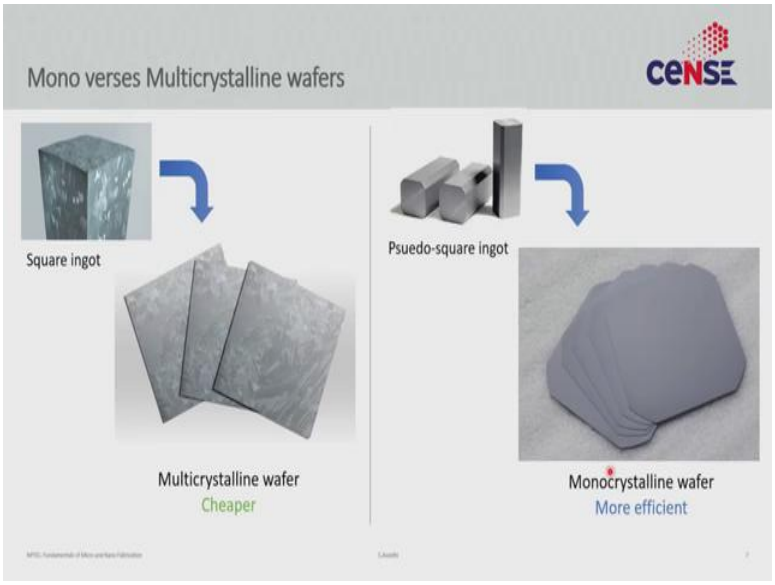

From these cuboid ingots, you get square multi-crystalline wafers. In the CZ process, you get cylindrical ingots and circular wafers. When you use circular wafers in a module, you lose area in the middle as circular shapes don't fill a flat plane very well. You don't make the cylindrical wafer a square; that would waste too much material, but a pseudo-square (a square with rounded edges). Mutlicrystalline is faster and easier to make; monocrystalline is more efficient and expensive.

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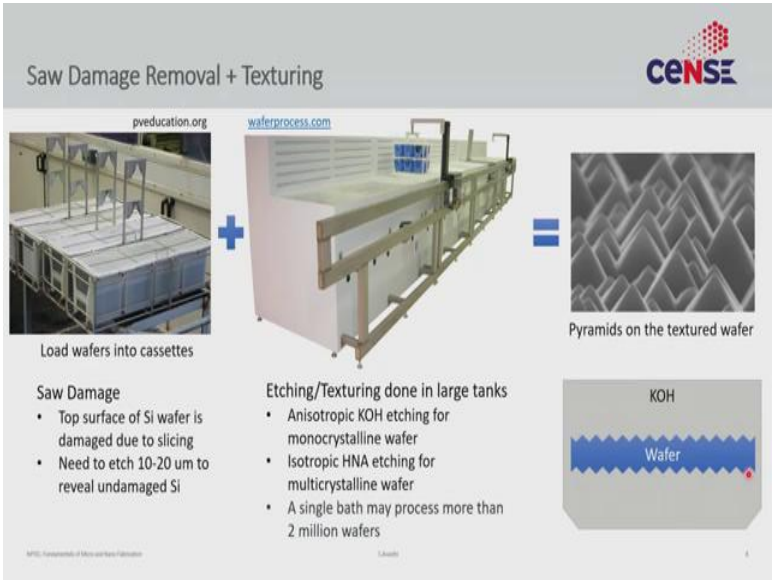

First, you clean the wafer. Before cleaning, the silicon solar people texture it; you create those rough surfaces upfront to trap the light. You mount the wafers into these cassette carriers. For 1000s of wafer/hour throughput, you mount several 100s of these wafers in these cassettes and process them in large vats or baths of chemicals. A robot or an operator takes thousand of these wafers, dips them in one tank for some process, takes out and put in the next tank for another.

How do you make a texture on the surface? By anisotropic etching, and the easiest is KOH. It is not CMOS compatible as it creates a lot of potassium contamination. It would not be allowed in a CMOS factory but is okay in a silicon solar cell factory. They don't care much about the Na, K contamination. They clean some of it, but they do not care about the trace contamination. They use the cheapest chemical they can find, usually NaOH or KOH, and dip these wafers without any mask or lithography. The surface gets randomly patterned pyramids with (111) faces for a single crystalline (100) face. But a multi-crystalline cell doesn't have one orientation. Anisotropic etching will not give you pyramids. You use a slightly modified HNA etch to have some textures simply because different facets etched in different ways. A single bath may process more than 2 million wafers before replacing the chemical with the fresh ones.

We also want to remove the saw-damage. As we saw the ingot into wafers, you damage the surface. So, we etch it during this texturing. We don't just get the texture. We also

etch the top surface to expose undamaged bulk. In the animation, you have the wafer with some damage on the top and the bottom. You put it in a KOH bath; it removes the saw-damage and gives you this pyramidal structure.

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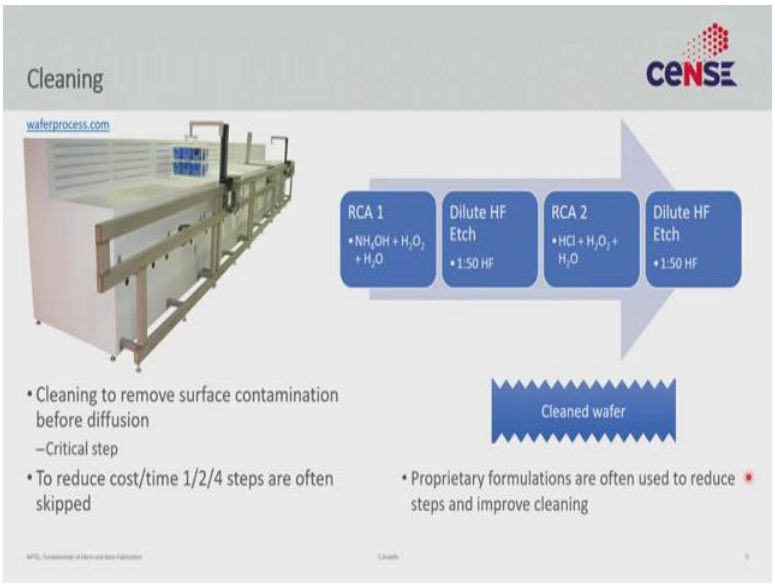

After texturing, you want to remove the potassium contamination and also metallic and organic contamination. In a typical system, we would do an RCA clean. Some research labs and high-efficiency solar manufacturers may still do that. But the problem is this process becomes too slow, and each of these chemical baths is very expensive. Because of the H_2O_2, the chemicals don't last long and require constant replacement. For a host of reasons, practical solar cell manufacturers skip one or two of these steps.

A lot of them don't do the final HF; some avoid the middle HF, some altogether remove the NH_4OH, and only do RCA2. Some only have HCl. It depends upon what works for you and what contamination you have in your process. How clean is your system? What minimum cleaning is enough? Do you create many defects? It is all about a meticulous cost-benefit analysis. As you see the cross-section, you still have the pyramids, but now the surfaces are clean.

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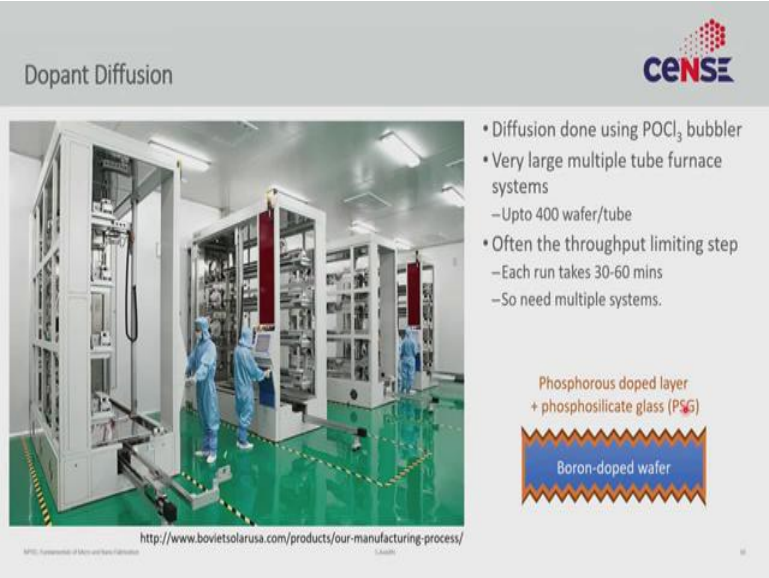

After this, we have dopant diffusion, a high-temperature and critical step. If you are not careful here, any contamination will diffuse and kill the wafer lifetime, crucial to silicon solar cells. From a uniformity and purity perspective, this step is critical. Diffusion is easier than ion implantation for doping. CMOS processing has wholly moved to implantation because it provides better control. But solar cells have not; implanters are too big and too slow. A couple of startups tried using implantation, and they were able to make more efficient solar cells. I don't know because of ion implantation or other reasons; they couldn't compete in the market. Most silicon manufacturers in the market today use diffusion, specifically the $POCl_3$ bubbler. You bubble gas through the $POCl_3$ liquid, get phosphorous inside that dopes the wafer.

It is a batch process in a furnace. To increase the throughput, you have massive batches. This example, I think, is from the Boviet solar production system. There are four furnaces with four tubes each. Each one, I am willing to bet, can accommodate 200-400 wafers. So, you can process ~ 6400 wafers simultaneously. If the diffusion takes half an hour, you can process > 12000 wafers/hour in this system. Diffusion is a slow step. It takes at least 10 minutes to diffuse and some time to load/unload. Since the fundamental step is limited in throughput, you have to compensate by having a lot of equipment. That increases the cost. Furnaces are relatively inexpensive, but if you have to do the same for ion implantation, it is much more expensive; it would become financially untenable. That is why diffusion won over more accurate repeatable implantation.

In the cross-section, this orange represents the phosphorous doped layer. As we haven't used any pattering, you get doping on both sides, which we need to fix, and the phospho-silicate glass (PSG, dark orange) that you need to etch.

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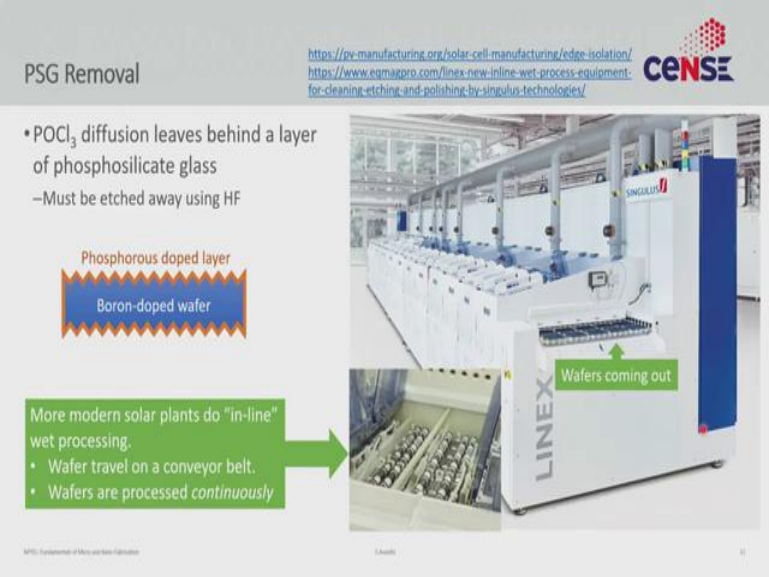

After etching this PSG in HF, you have this phosphorus-doped layer that wraps all around the textured surface. The previous etching system was a batch process where you load the wafers into cassettes and dip them in a bath. For a modern design (as in the slide), even that is too slow. Here, you see inline wet processing. The wafers enter the assembly line on the back of this equipment. Internally, it has rollers, and the liquid filled to the brim. As the wafer goes over these rollers, it touches the liquid underneath, the etching or whatever process you want happens, and then the wafers come out.

It is like a conveyor belt; wafers go in, wafers go out. Robots can do it reasonably fast, without human involvement. That increases the throughput, reduces cost, and is the result of a lot of innovation. It is a significant departure from how Intel or AMD would do wet processing. Solar cells do it at a mind-boggling scale.

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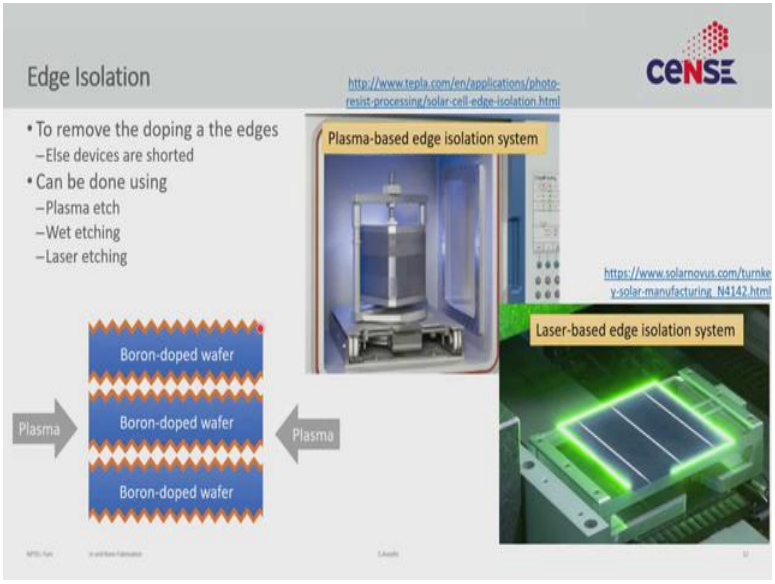

Now, we have to solve this wrap-around emitter doped layer. First, you cleave these edges using edge isolation. The traditional way is the following: you stack hundreds of wafers on top of each other, exposing only the edges. Put this stack in some plasma that can etch silicon. As only edges are exposed, only they etch. The plasma etches the edge, so the top and bottom doped layer electrically isolate.

In modern plants, we try to move away from batch processes and human involvement. If you load/unload the cassette, it takes time and has more damage. We prefer the inline method. You put the wafers on a belt and detect them. A laser on the top scribes a rectangle and creates a groove that electrically isolates the top diffused layer from the bottom. Newer production systems use laser-based isolation.

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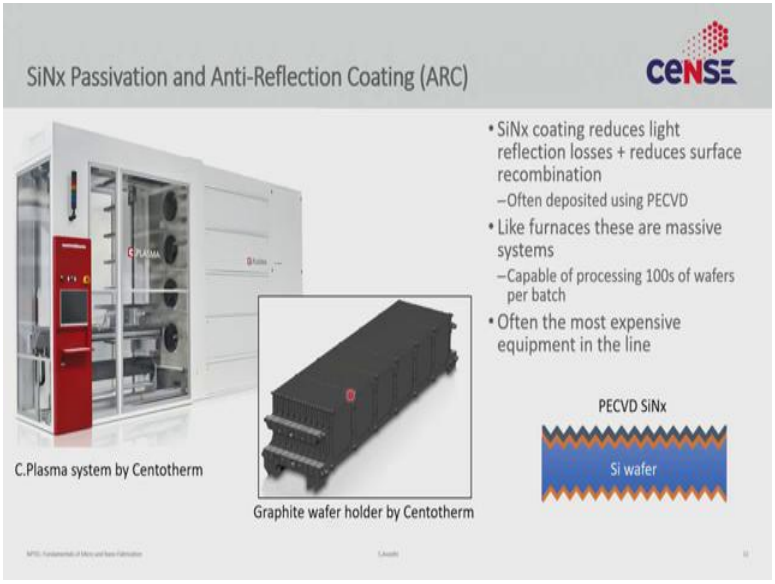

After the junction, you deposit anti-reflection a passivation layer. The thin Si_3N_4 passivation layer on the top reduces surface recombination and prevents reflection losses. We could do LPCVD, but it requires high temperatures and another bunch of furnaces. PECVD is a slightly lower temperature process but is usually is a single wafer process and requires an expensive RF power supply. Some older manufacturers tried LPCVD; some try PECVD; most modern ones use PECVD these days. But it is very different from the PECVD you see in your research facility or an Intel fabrication system. These plasma systems look like furnaces and are RF deposition system.

An RF deposition system requires electrodes. How do you provide electrodes to 400 wafers? You make graphite wafer holders with hundreds of grooves that can hold a wafer. A robot loads/unloads this cassette inside the deposition system. These optimizations and advances allow you to do that many wafers per hour, which otherwise would not be possible. After this process, you have a silicon nitride film on the top. In the next lecture, we shall look at how to make the rest of the silicon solar cell.