Fundamentals of Micro and Nanofabrication
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Lecture – 56
Process Integration

Process integration is not an integral part of this course. Still, it is useful to understand some fundamentals so that you can make devices successfully. It's tough to teach process integration (PI) in a very structured manner; you learn it by making mistakes and getting better with time. The best way I have found communicating some of these concepts is to discuss case studies. Most of this lecture is a description of the problems students face and how we solve them.

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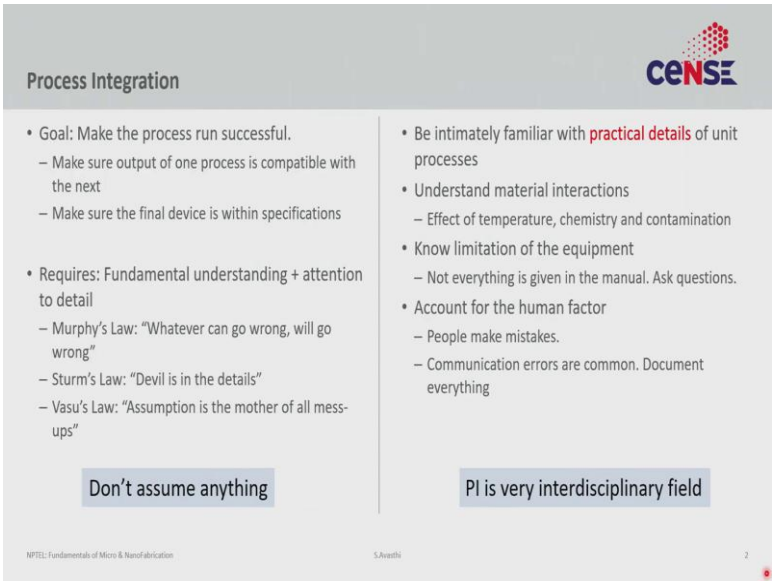

What is process integration? Process integration aims to use the techniques of individual unit processes together in a chain such that the end device is successful. It requires a fundamental understanding of unit processes; you need to be an expert in all the process details. Should you use sputtering or evaporation? What is the impact of sidewall deposition? Under what condition is it isotropic? How much selectivity is enough? Do I need an etch top? The person doing process integration should answer these questions, such that the eventual device works as per specifications, has a high yield, and is repeatable.

The devil is always in the details. We have discussed so many points in each of the modules. Those details help you in being a better process integration person. PI is a very interdisciplinary field. It requires some understanding of chemistry, physics, material science, devices, and experience of working in the cleanroom. As far as the jobs inside the fabs go, it is one of the most respected jobs. The best people in the fab tend to be the PIT, Process Integration Technicians.

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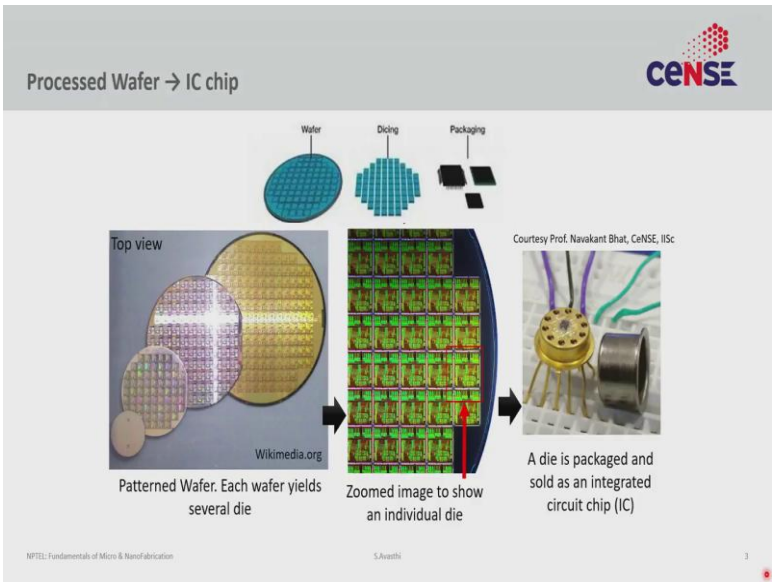

After, say, 50, 60, or 100 steps of deposition, etching, patterning several layers, you end up with a processed wafer, but this is still not a device. You need to cut it into individual dies and package them into devices. You put these packaged devices in a circuit that the end-user uses. The process integration person should make sure that this works perfectly. For this device to function at the packaged level, you need many optimizations at a wafer level. While the job is limited to the wafer, the PI person should have a clear idea of how you package the eventual device.

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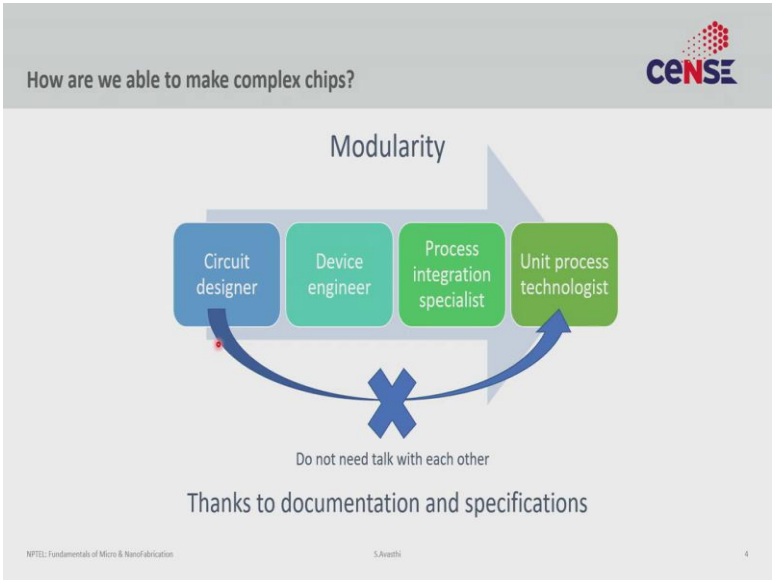

We make remarkably complex chips. A typical Intel device has more than a billion transistors. We have looked at many nitty-gritty details, but we have just scratched the surface even then. It is fundamental of the micro nanofabrication course. We can do an advanced micro nanofabrication course; we may not cover all these process details even there. It is incredible how all of this comes together and the final device works. Part of the reason is there is inherent modularity in the system. A laptop has a motherboard with a processor chip. Inside it, there are devices designed for a specific function. There is a process integration person to develop a process to make those devices. A unit process specialist focuses only on unit processes; for example, only deposits metal and optimizes the recipe.

There are so many layers of the problem. You start with a unit process and go all the way up to the circuit design. The system works in a modular fashion. The circuit designer never talks to the unit process person. All the circuit designer wants is the information on the device characteristics (current-voltage) and doesn't care about making the device. They design a circuit depending on the device's properties. A device engineer also doesn't think about how the device gets fabricated; that is a process integration engineer's problem. The process integration person asks the unit process capabilities and doesn't optimize it. We have a clear demarcation of the responsibilities. People talk based on documentation or specifications but don't necessarily sit in the same room and discuss.

This modularity is the key to make sure you get a new chip every two and a half years that works the way you design. Documentation and specification is a crucial aspect of process integration. You should keep detailed and copious amounts of notes on the fabrication process. Otherwise, a few months or years down the line, you will not remember them and will not be able to recreate those devices.

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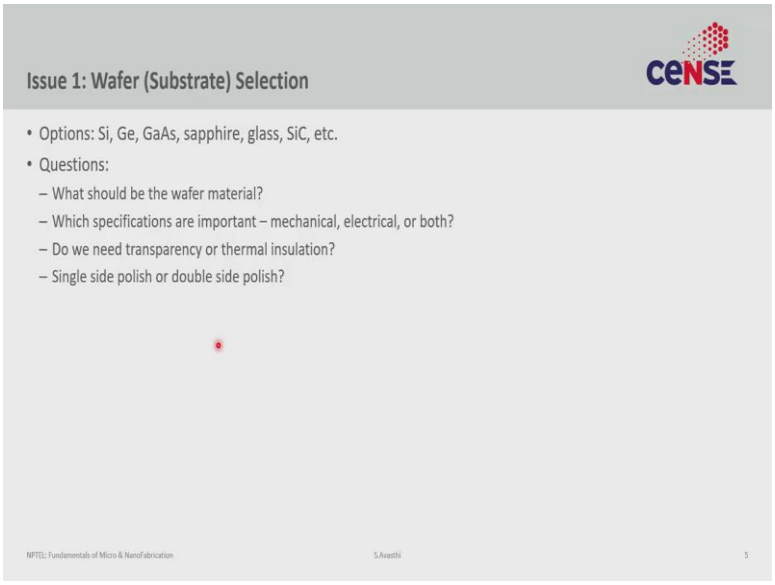

The process integration starts with substrate selection. There are so many options; we have silicon, germanium, gallium arsenide. What properties do you need? For optoelectronic properties, if you want to make an LED, GaAs is much better than silicon because of the direct bandgap. If you are making a MEMS device, you care about the mechanical specification, but you care about mechanical and electric properties while creating a solar cell. You also have to select an appropriate wafer grade (test, prime). For transparency, silicon carbide and sapphire are suitable, but silicon is not, at least not for visible light. For high power devices using GaN, thermal conductivity is hugely important. You can't have GaN on silicon easily; sapphire or silicon carbide are better substrates. You choose, depending on the thermal load. Single side polish may be enough, but you should start with a double-side polished substrate if you want to pattern both sides. By selecting an appropriate substrate, you can upfront manage many things that will be important down the line. It enhances the success rate. You can figure these problems out by making a mistake, but you waste a lot of time and resources.

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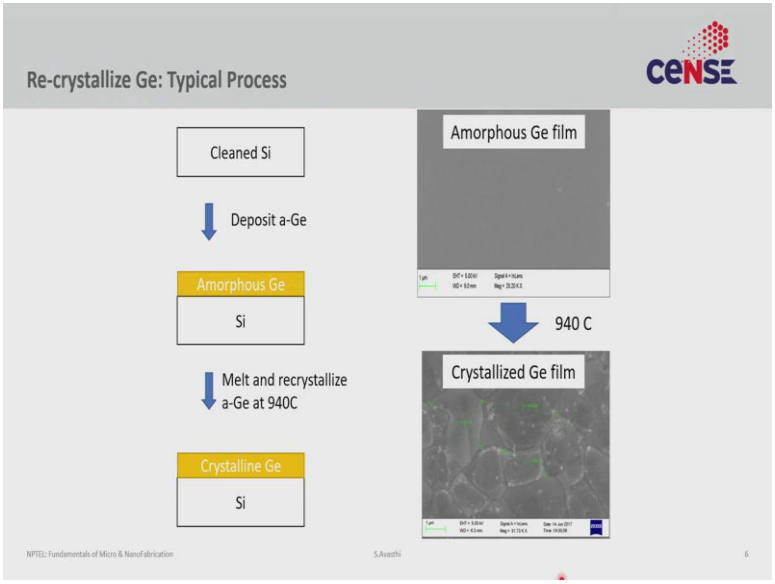

Here is an example from our lab; We are trying to get a germanium film. On a silicon substrate, it works very well. You see grain boundaries and polycrystalline germanium.

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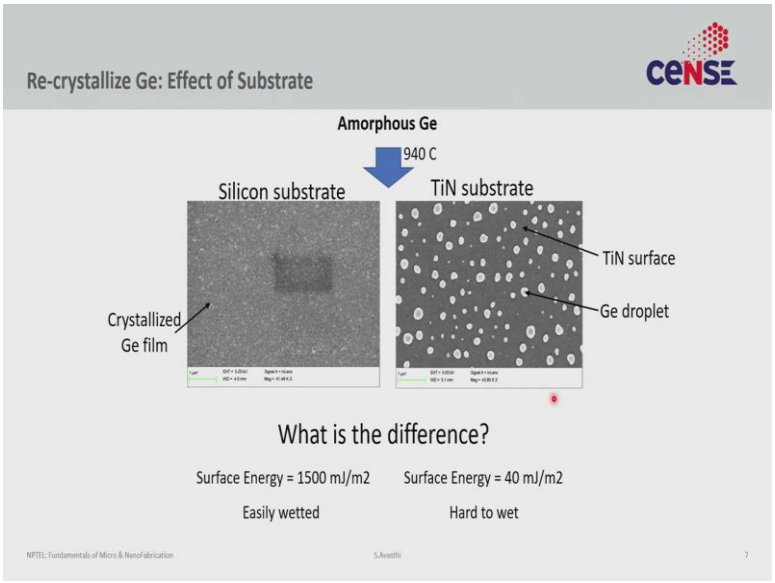

However, when we try the same thing on titanium nitride coated silicon, germanium forms droplets and not a continuous, uniform film. Why does that happen? During this process, we are melting and recrystallizing or re-solidifying the germanium. When the germanium is liquid, it is sensitive to surface tension. It wets the silicon surface and forms a smooth layer but doesn't wet the titanium nitride surface. So, it forms droplets. If

you look at the literature, the surface energies are different, and it's hard for germanium to wet TiN. If you think ahead, you can predict and prevent the problem and save time.

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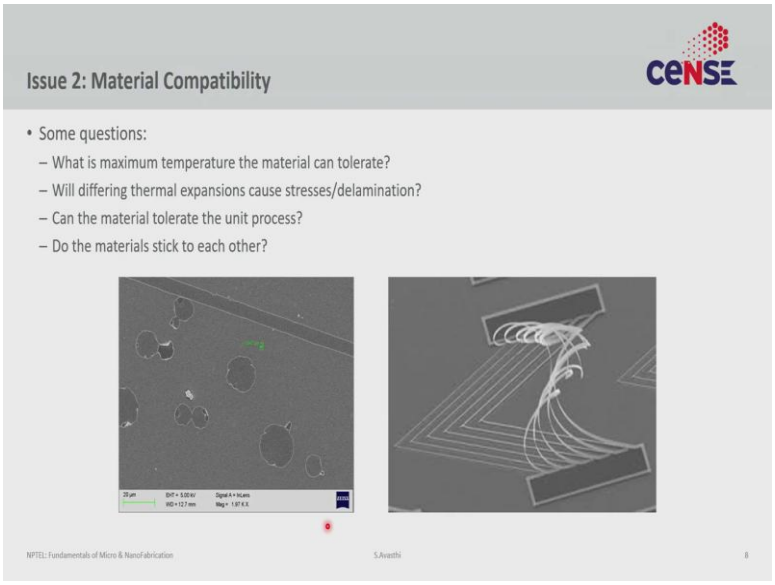

Material compatibility is another issue. What is the maximum process temperature can your material tolerate? With a glass substrate, you should never exceed 650-700^{o}C. Above that, it becomes soft. A film containing an aluminum layer should not heat above 600-700^{o}C because aluminum melts. When you cool the stack after a high-temperature process, you create stresses that can delaminate the film. This SEM image shows some delaminated metal layers.

Can you make some changes to prevent it? Can you add some adhesion layers? Can you change the process temperature to limit the stresses and avoid delamination?. When you deposit material on another, you implicitly assume them to stick, but they may not.

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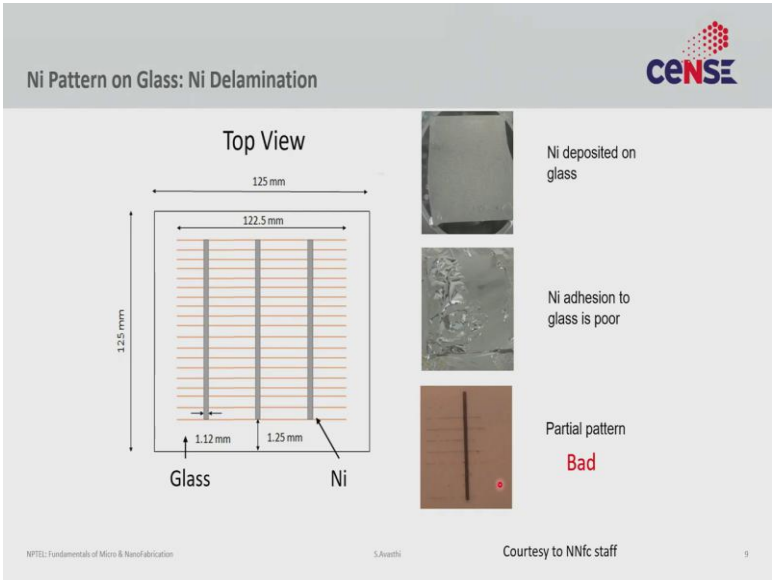

You are trying to make a nickel-metal grid on the glass. You pattern the nickel layer using lithography and etch, or lift-off. When we did it, we found that the nickel doesn't adhere to glass. When you try to pattern this poorly adhering nickel, it comes off or peels off. You see, some of these lines have blurred because the nickel has peeled off. You get a non-continuous pattern. What can we do about this adhesion problem?

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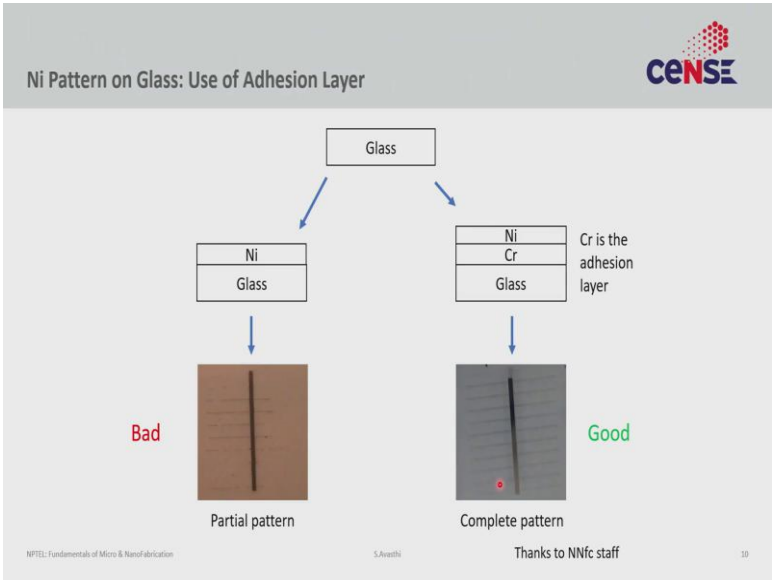

You can introduce a thin chromium layer between the metal and the substrate that acts as an adhesion layer. Titanium does the same thing. It can be 10 nm or thinner but allows

you to deposit nickel on the glass. You get perfect adhesion, patterning, and no peeling off. You pick up things like these with experience.

Always think of the effect of the process on the device. During any unit process, we may heat the wafer, expose it to chemicals or plasma. All of these can impact the device. During e-beam evaporation, we discussed that you could form a few x-rays that can cause defects in the Si-SiO_2 interface. Sputtering is a higher energy process. It can damage the surface, especially the organics. You should think in advance, what is the effect of the process on the devices?

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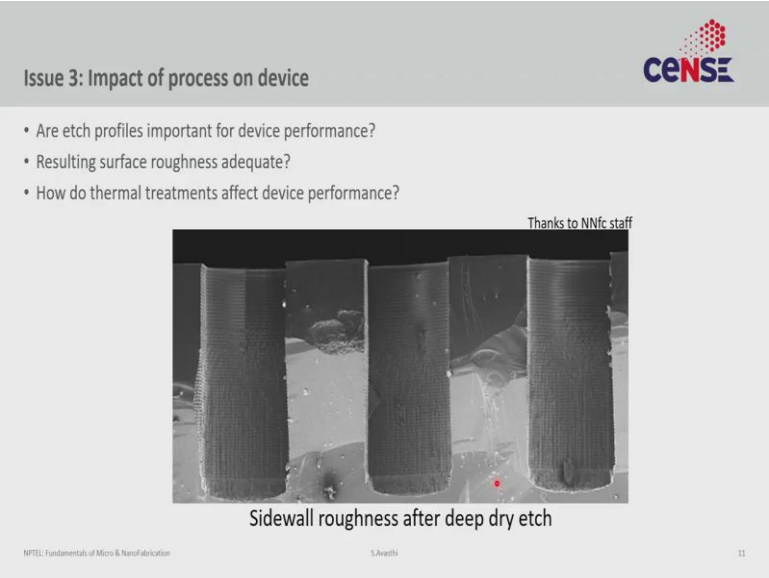

What kind of etch profiles you want? From the cross-section of this device, it is evident that we have used deep reactive etching. You can tell these from the rings or scallops on the wall that you get from each cycle. Is this surface roughness acceptable? For MEMS, maybe, but for a Laser, or a photonic waveguide, it is problematic because it scatters light and reduces the device efficiency. What can you do? You can try RIE or wet etch. If you need high aspect-ratio features, try combining DRIE and wet etch to smoothen it.

If you have aluminum, don't subject it to more than 800^{o}C. If you have metal, don't use acid cleaning. In BEOL, use a dry etch or solvents to clean organic contamination, not an RCA. Use the basic concepts of the unit process you have learned, and apply them to the process integration.

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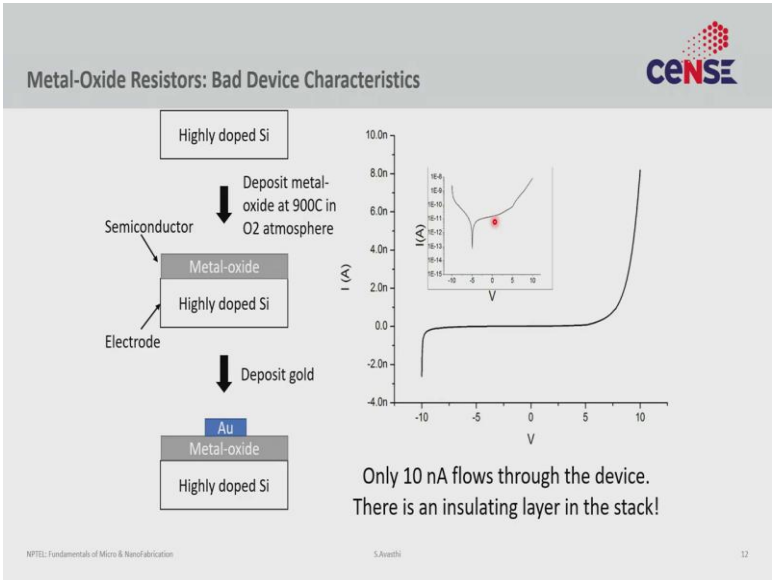

Oxides are usually insulating and not attractive. But you also have semiconducting oxides. Imagine you are trying to study a particular metal oxide. You deposit it on a highly doped silicon wafer, as it is easy and can serve as one of the electrodes. You deposit the oxide at 900^{o}C in oxygen ambient and sandwich it with gold on top to measure I-V characteristics. When you get the data, you find out that you flow only 10 nA current, a tiny amount. You would think that the oxide is very insulating, but it may be a wrong conclusion. If you deposit it at 900^{o}C in an oxygen atmosphere, can you guess the problem?

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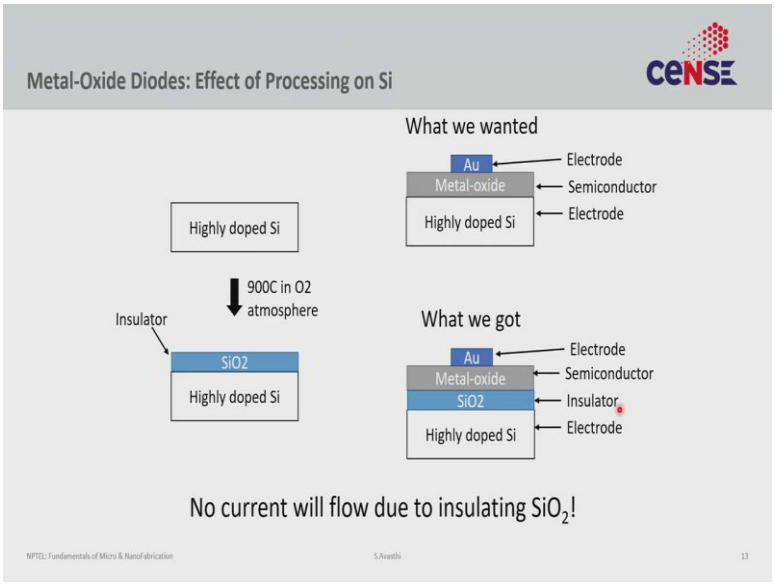

The problem is, the highly doped silicon oxidizes at 900^{o}C in. So, you get a layer insulating SiO_2 in the stack. Then, it doesn't matter whether the metal oxide is conductive or not. The insulator that adds because of the way we did the process decides the I-V characteristic.

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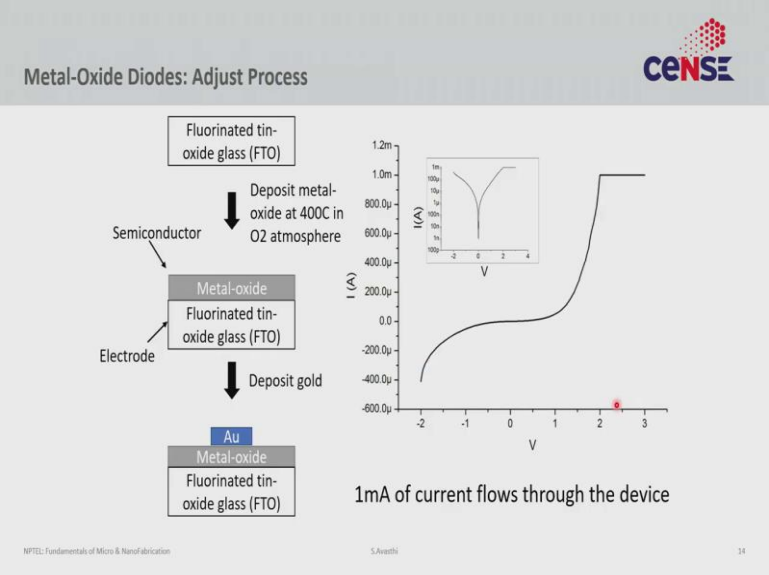

FTO is a conductive oxide and doesn't oxidize anymore. You deposit the metal oxide on this conductive substrate, at a slightly lower temperature, instead of silicon. Now you see microamps of current that you expect. So, the problem was not metal oxide but the formation of SiO_2. You can come to the wrong conclusion by not thinking about the process's effect on your device.

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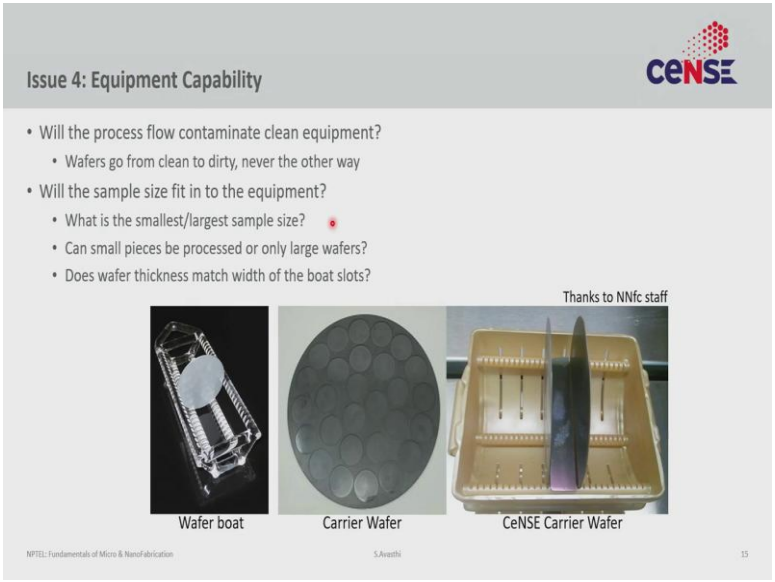

The next issue is of equipment capability. A lot of people don't interact with the unit process specialist enough. You should always ask a lot of questions; what is the proper size of the wafers? Can you take small pieces or only full wafers? What temperature range do you allow? What is the contamination policy, and what materials can we use in the tool? How do you load the sample? Can I clean the sample 24 hours before, or do I have to clean it immediately before loading? A successful PI person has an excellent handle on these nitty-gritty details. Here is an example; you can process the full wafers with this boat but can't load a small sample of, say, 1 cm^2. You can make make-shift boats or use a carrier wafer.

However, it requires you to prepare in advance. If you do not think about the problem, you do all these cleanings, go to the tool, ready to deposition, and suddenly realize that you cannot. It wastes a lot of time, energy, and it's very demoralizing.

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Unit process usability: You should deliberate a bit more than a direct read-out of the capability specifications. What is the deposition rate, the minimum or maximum thickness? Does it work for my flow? In this example, we want a conformal coating of SiO_2 and Al on the patterned silicon. There is an inherent assumption that the deposition is conformal, and hence, Al never touches Si. It can be an excellent gate. If the process is not conformal, SiO_2 can have a little break, and Al can contact the silicon. It can create a short circuit, as you have a metal-semiconductor interface instead of a metal-insulator-semiconductor one.

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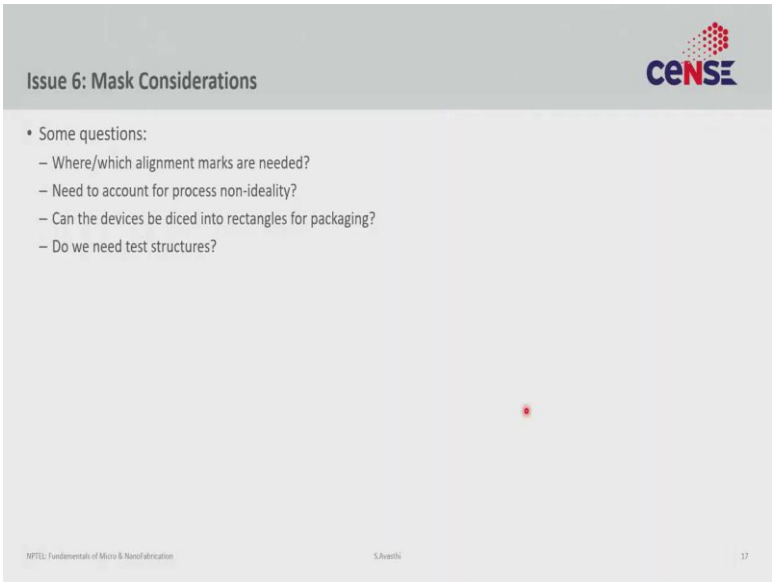

A mask is often the first thing you make. Because it is the first thing, any errors or omissions at the mask level can bite you later. Invest a lot of time and thought into designing a correct litho-mask. What is proper litho-mask?

You should have appropriate alignment marks. Alignment marks for a critical dimension of 1 µm vs. 5 µm are very different. Account for process variability. If your mask pattern requires you to wet etch with 0.1 % precision, it is not possible. You may need to change the design. If you are going to package the devices, have thought of how will you cut these devices into dies and how will you mount them on the packaging platform? Have you placed test structures? If you make a transistor, and it doesn't work, you have no way to say which process has failed. You require a whole bunch of test structures to measure the oxide thickness and leakage, the metal thickness, step coverage, pinholes, or at least the presence of pinholes, someplace where you can take nice cross-sections to inspect in SEM. If you have these test structures on your mask, it becomes easy to fine-tune the recipe, figure out what went wrong, and fix it. Otherwise, it's a black box.

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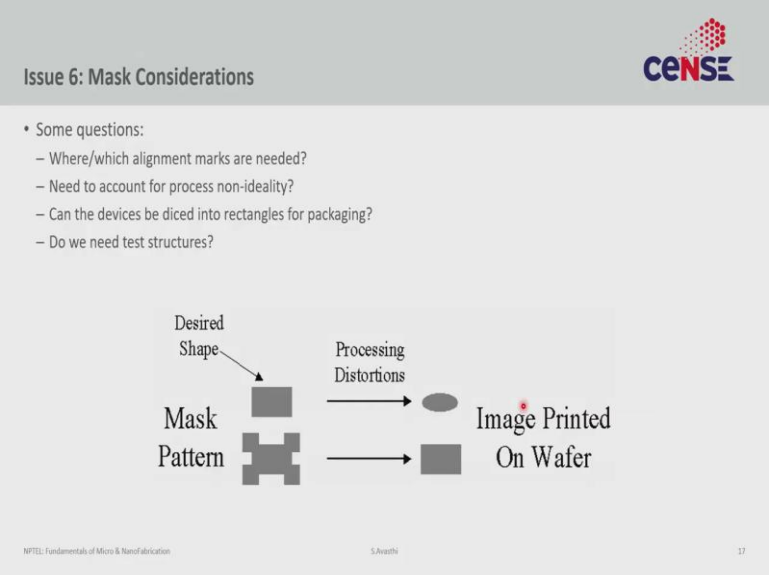

If you start with a rectangle, you may get a smooth oval, especially if the futures are small. If you want a rectangle, you should start with a slightly different shape. You can solve these at the mask level and save a lot of time down the line.

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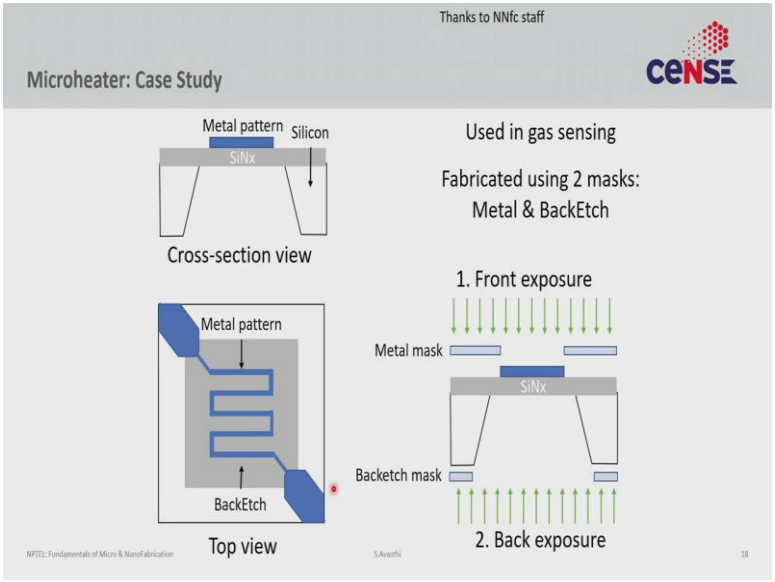

Here is an interesting case study of what can happen if the mask design is a little flawed. The users were trying to make a microheater. It is a (micro) metal filament that you can heat by flowing current, like a bulb. It can, in turn, heat the substrate. In the cross-section, you have metal on Si_3N_4 on silicon. It requires just two lithographies to pattern the metal on top and cut out a silicon hole from the bottom. There are two depositions, Si_3N_4 and metal.

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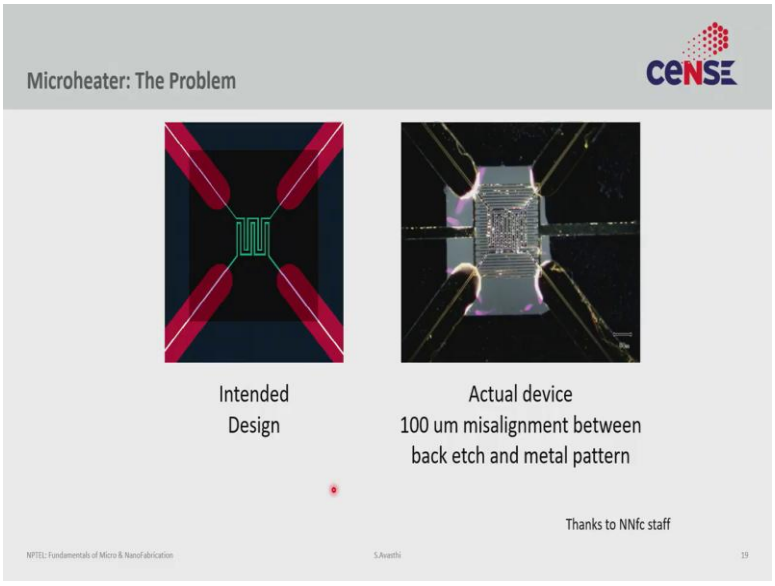

You see the metal lines and the grey Si3N4 membrane over the back-etched hole in the fabricated device. The metal grid is not in the center of the membrane, as you would expect from the design, but is off by a large amount (~100 µm). The grid is the heater, and if it is not in the middle, it heats nonuniformly and may cause device failure. We can't tolerate this issue. From where does this issue come? You may blame lithography, but we did a lot of tests to check the equipment.

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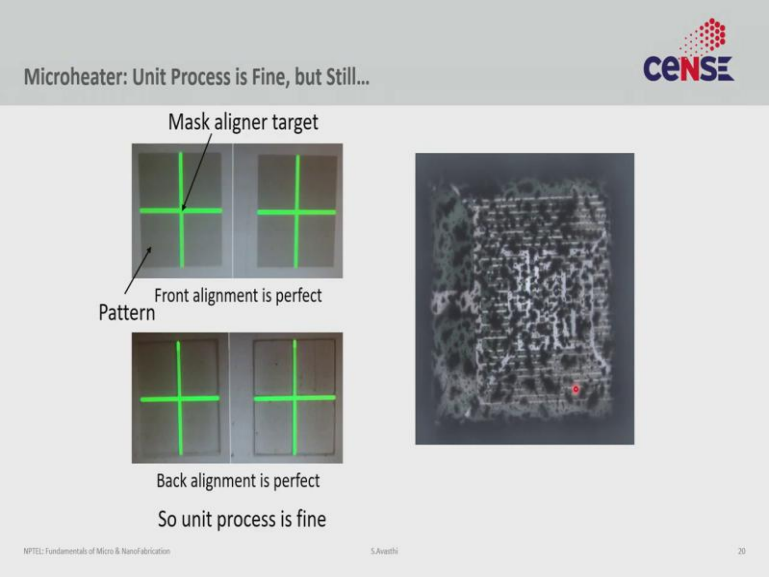

If you don't understand this figure, don't worry about it. It shows that the front and the back alignment is perfect. This device did not work, but other people's devices worked. There was no problem with the lithography unit process. Also, the misalignment in this heater was repeatable. It was the same every time we made the device. Then, what is the issue?

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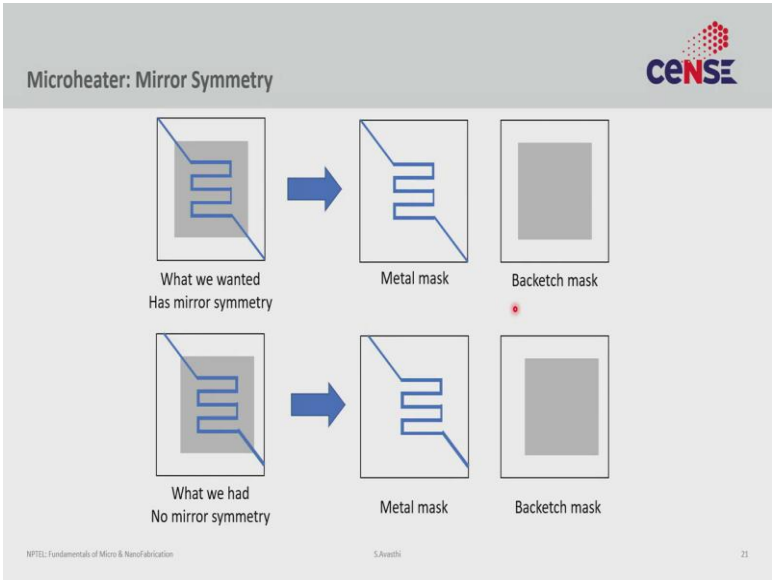

Here is what happened. The grey region represents the back hole, and the blue, the metal electrode. The design has mirror symmetry. The designer broke it into two different masks; one for the metal pattern and another for the back etch hole. The problem is they erroneously made the structure slightly off-center, breaking the mirror symmetry. On its own, there is no problem; both the masks have the same relative offset.

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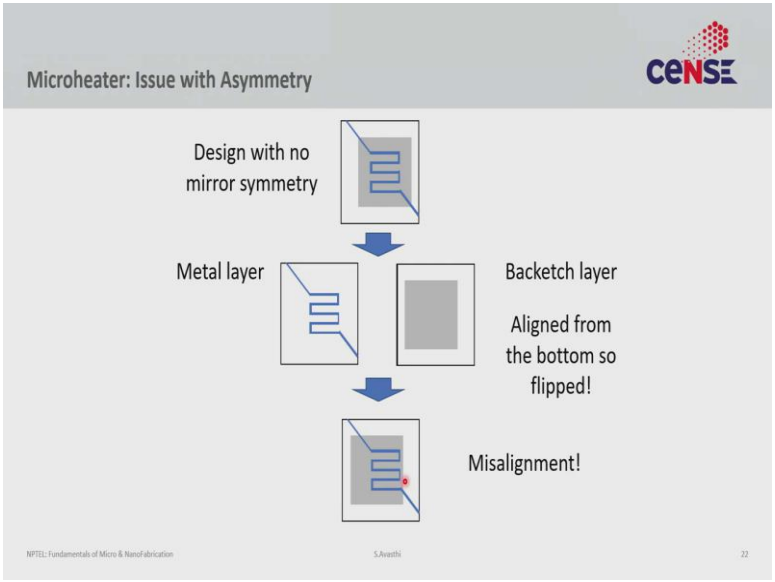

The problem is how they did the lithography, by patterning the film from the top and the back-etch hole from the bottom. Now, these patterns are off by the same amount, but in

the opposite directions! Because you flip the bottom mask from left to right. The problem was not in the unit process but the mask design. Once they fixed the mask-design, the issue went away.

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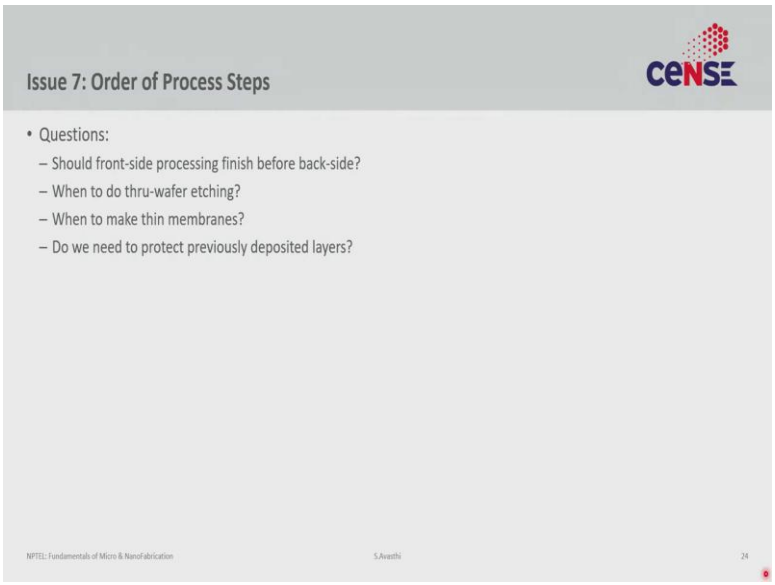

The next issue is the order of steps. If you have multiple patterning steps, you often have to choose the sequence. The question comes to, which is more repeatable and clean. It is worth thinking about before processing.

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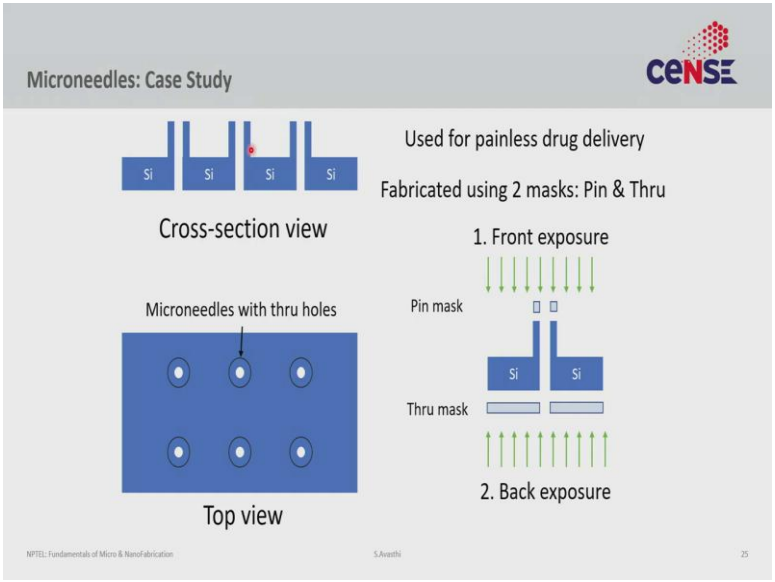

Microneedle fabrication is a good case study. We are trying to make small and sharp silicon microneedles. Theoretically, the advantage is that they can inject things like insulin into the body without pain. Syringes are painful because one macro needle pierces you, and that is hurtful, but if you have these 100s of microneedles piercing, you might not feel it much at all. You have a silicon wafer with a lot of hollow cylindrical holes. Once they breach into your skin, they can inject. It has a simple fabrication process; all you need is two lithographies and etch steps. The pin mask defines the outside of the needle, and the thru-mask, the hole. How would you do it?

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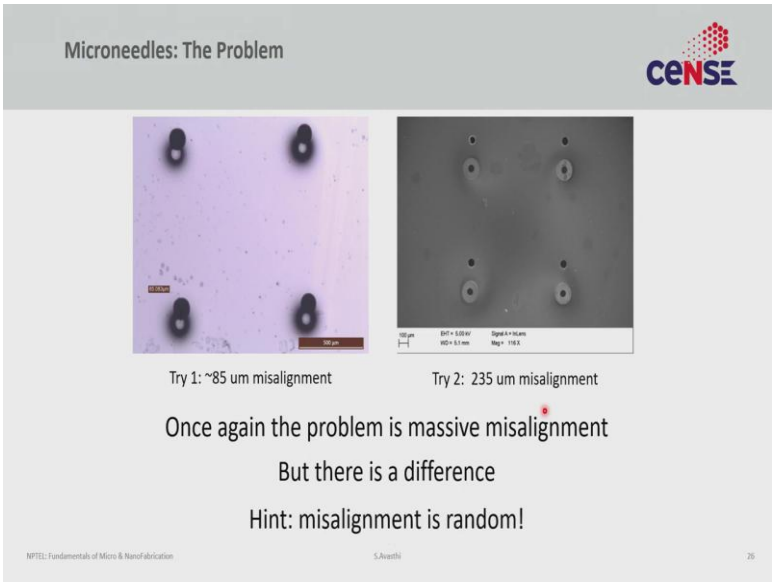

We started making them in our cleanroom at IISc, and just like in the previous case, we consistently saw misalignment between the pin and the hole. We didn't get the hole in the center of the needle cylinder. However, here, the misalignment was random. Again, the problem was not in the unit process; the unit process worked fine. Then why do we get the misalignment? Think about the order of the steps.

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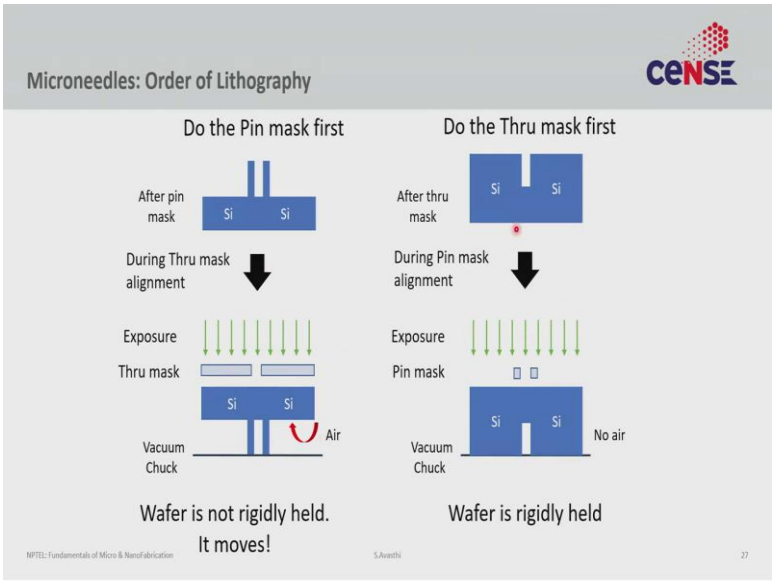

We were patterning with the pin mask first. You have to turn the wafer upside down to pattern the thru-mask next. For aligning the layer, you hold the wafer to the chuck by vacuum contact, by evacuating the air. The outside air pressurizes the wafer snugly on top of the chuck. But look at this cross-section; the bottom surface is not flat. The wafer rests on the pins! When you try to create a vacuum, it does not hold the wafer because the air continuously leaks in through the bottom. The wafer can move. Even if you start with an aligned wafer, it misaligns through vibrations during the exposure. Hence, the misalignment is random.

So, we have to do the second patterning process first; switch the order. We did the thru mask first and then turned it upside down. Now, we do not have these needles at the bottom. We still have holes, but, by and large, a flat silicon surface. The wafer holds tightly on the vacuum chuck and doesn't move around while you align the pin mask.

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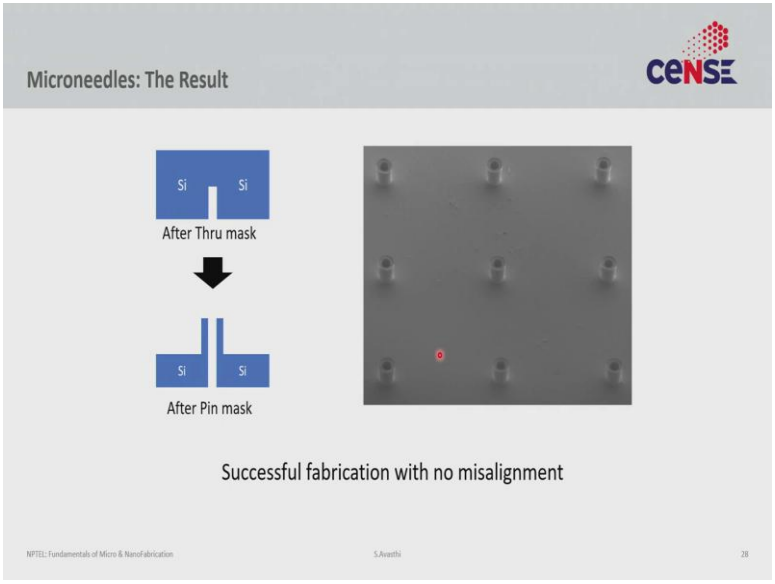

On the left, we have the cross-section for the switched order of the patterning steps. On the right, we have an SEM image of beautifully developed microneedles.

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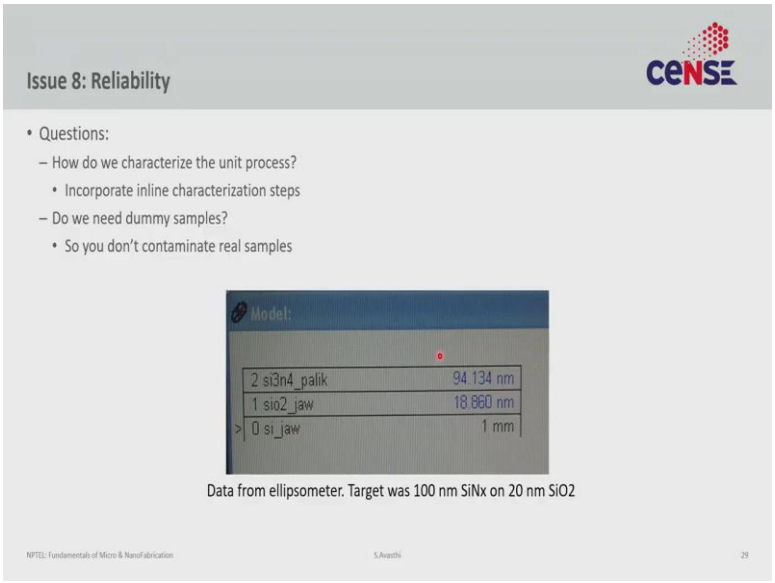

The final issue I would like to highlight is reliability. Often in academic circles, we don't give reliability its due weight. The goal is to show one successful device, write a paper, and move on. In technology, you have to offer repeatability. You have to make the same device repeatedly and make sure it performs the same way.

Even in academic circles, it sometimes necessary to think of reliability. If a student is doing ten process runs, and only one comes out successful, it takes ten times longer. To improve it, you incorporate a bunch of characterization steps in the process flow. Don't wait till you fabricate the whole device to find out that the metal or the SiO_2 you deposited was too thin to work. If there is a failure, fix it or start a new run. Why waste all the time and effort completing a device that will not work?

A lot of times, it is good to have multiple dummy samples. Say your process requires 30 steps. If a piece has gone through 25 successful steps, it needs just five more to become successful; it's a costly and precious sample now. When you approach the 26th step, first try that process on the dummy samples to ensure the equipment is functioning, the recipe is stable, and you get what you expect. Then you process your precious sample. Then you have a high probability of success for the 26th. Dummy samples, in-line characterization, a lot of test structure can improve the reliability of your fabrication.

Here, we wanted 100 nm Si_3N_4 on SiO_2, but what we got was 94 nm Si_3N_4. That may or may not be okay, depending upon the process tolerance. But it's essential to do these measurements during fabrication, not to get a surprise at the end.

That was a concise introduction to process integration and what it takes to be a good process integration person. I can't tell you everything you need to know. You learn a lot of it by experience, thinking, spending some time, and being an expert in the unit process. The more you understand the unit process, the better you can be at process integration. We discussed a lot of case studies; hopefully, you would have found some interesting and illuminating.