Fundamentals of Micro and Nanofabrication
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Lecture – 55
Design for Manufacturability: A case study

A Design for Manufacturability also affects both the front end and back end of processes. So, let us look at what do we mean by the front end and back end. Though we have seen in earlier lectures, let us recap what we mean by the front end and back end first.

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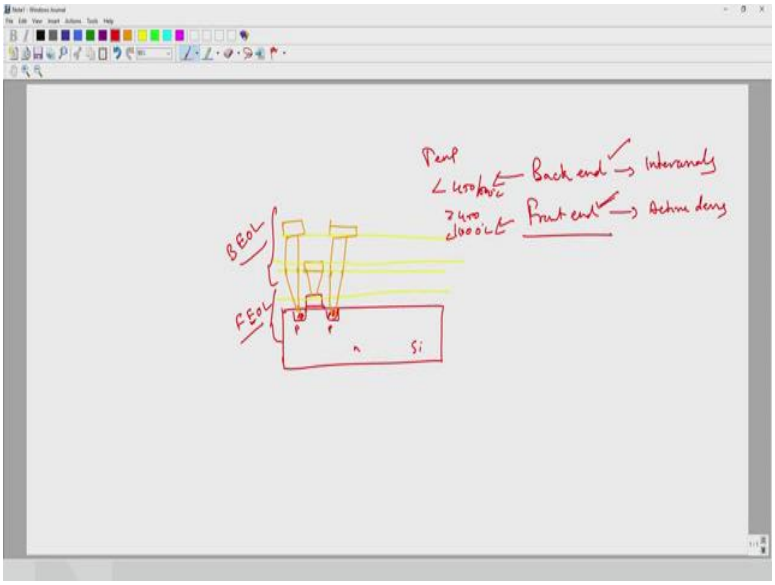

Let us say we are fabricating a device on silicon, which may or may not be an electronic type device. In this case, let us assume that we are fabricating some electrically active structures. So, we take silicon and dope it to make junctions. Then, let us say we make a gate and coat this surface with an oxide layer. To connect one transistor to another, we make our metal contacts and then further on, we take these contacts to connect to different layers.

Now we have the devices on silicon, and then we have metal and dielectric on the top. So, here the front end of the line, FEOL, means the doping region and the critical active layer just below the contact; gate. And then all the metallization and the connectors that we do is called back end of the line, BEOL. So, these connectors are very important to connect various transistors at the same time FEOL is what we use to define the transistors and so

on. So, there is a functional difference between these two. So, functionally speaking, the back end primarily means interconnects, and the front end is primarily the active device. If we consider process-wise, for the back-end process, the temperature that we can operate should be less than 450 or 500 °C while, for the front end, we can go from 400 to 1000 °C for a doping activation so on. So, we can have two temperature bands.

So, the reliability depends on how well we take care of both of them. So, the front end is primarily defined by active device fabrication, and the back end primarily dictates interconnects.

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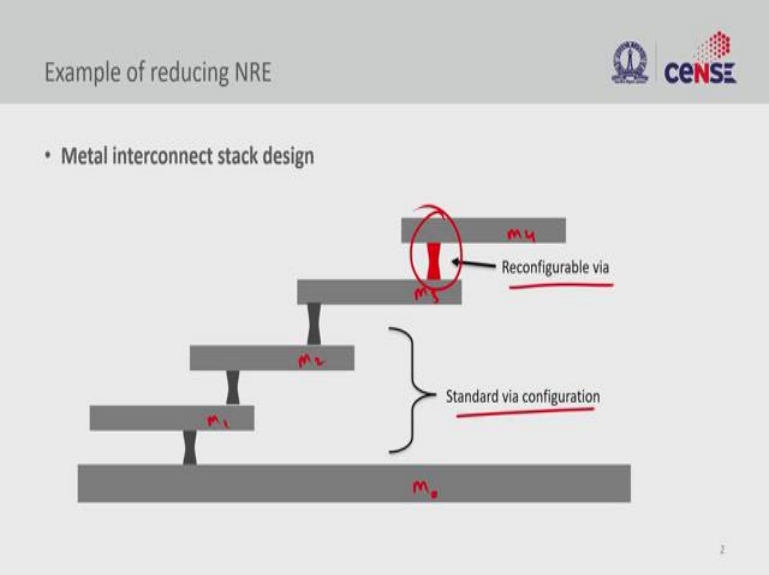

So, let us just have a quick look at how the back end helps in addressing reliability. A way to reduce the non-recurring engineering costs is by using reconfigurable vias. So, we saw these multiple metal lines named M_0, M_1, M_2, M_3, and M_4.

These metal layers are connected through this metal via. If we want to reduce cost in designing and fabricating these multiple device and circuit architectures, we keep some standards via configurations; in this case, 1 2 3. So, these first three metal layers are connected by standard via configuration.

And now we have some layers that are reconfigurable. So, by doing this, we only change via of metal three to metal four layers. So, only by changing that particular metal via, we can reconfigure, and then we can make circuits that we want. So, what we have done now

is instead of changing the whole metal stack, we are only changing one intermediate layer. This will allow reducing the cost of fabricating or releasing a new product or realizing a new device, it is not just the cost, but it is also reliability. Now we are not really changing all the metal layers and all the interconnects; we are only touching one layer. This also tremendously improves yield when we go from one device architecture to another device architecture while keeping back end or interconnect architecture relatively stable and standard. This may or may not be possible in all the cases, but we try to explore if it is possible to maintain the standard architecture.

In this case, we have only one reconfigurable via; maybe we can do two reconfigurable via in difficult cases. So, it can be two immediate layers, or you can strategically take different layers to define new architecture. In this case, M_1 M_2 could be made reconfigurable, or M_3 M_4 could be made reconfigurable. So, the whole idea of this reconfigurable interconnect is to reduce overhead in development and keep reliability and yield at the maximum level by not redeveloping processes for a new device or circuit architecture.

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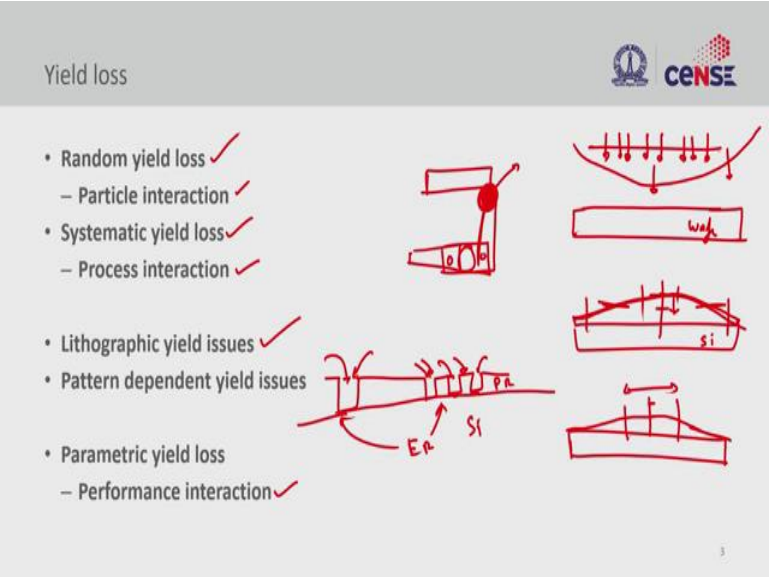

So, there are various factors that contribute to yield alone. Yield is a very important thing that will affect your product cycle. We are taking yield from various perspectives; there is a random yield loss, systemic yield loss. So, these are two are primary yield losses that we could see.

As we already saw earlier in Design for Manufacturability, random yield loss could be from particle interaction. So, we can have random particles coming and settling onto a wafer or structure that could really affect the circuit. So, we have a certain configuration, and if a particle comes and sits here, as shown in the slide, then we have a short circuit. But now you have via here which should be connected, and then if I have a particle that is sitting in between, it will make an open circuit instead of short. Depending on the nature of the particle, whether it is insulating or conducting, particle interaction with the circuit will give random yields. These are called random yield losses, as we do not know where these particles are going to come and sit on a wafer or circuit.

The other type of yield loss is systemic yield loss. So, this is primarily coming from the process. For example, if we are depositing using the plasma process. So, we have a deposition plasma and wafer, as shown in the slide. Ideally, we must have a uniform plasma, and hence material coming onto the wafer is also uniform. But it is possible that we are unable to create a uniform plasma on top of the wafer. So, this will create a depletion of radicals; on the sides, we have a very low number of products, at the centre, we have a high number of products. If that happens, we will have a very thick layer at the centre, thin layer at the edge. This can be anywhere between 10 to 15 % if it is worse. Ideally, we want to maintain it below 5 % on uniformity, but this is systematic. So, we can see here this yield is very systematic. So, if target thickness is somewhere, as shown in the slide, we will have over deposition at the centre and under deposition at the edge. If we reduce the maximum thickness we have at the centre to the required value, the overall thickness will come down.

In this case, if we are going to optimize thickness based on the yield thickness, we will have our yielding device within a range below which we will have very thin films, and we are going to lose those devices. In the previous one, we have yield somewhere away from the centre, but also a large window of devices where we were able to use it. But now we are reducing that window. So, one needs to take a call on how to optimize the thickness for a certain application. Again, the design should also give the process developers whether the certain thicknesses that we are proposing can be used with a certain variation. If the variation is ± 5 % so, our corner simulation should help to give confidence; even with this 5 % variation or 10 % variation, you should be able to get the desired yield. So, the

systematic yield loss is because of process interaction. So, the process has certain systematic repeatability.

So, we saw the front-end lithography-related yield; this primarily comes from the difficulty in patterning these devices and how we address these problems that we saw earlier. Pattern density yield issues are something new that we are introducing here. We will see in a few slides what do we mean by density-dependent yield.

So, lithography also has a density-dependent phenomenon, what we call the proximity effect. There are other processes, for instance, the CMP process or dry etch process, which are also patterned dependent. In a dry etch process, we have density dependents etch rate, So, you have a structure as shown in the slide. We want to etch these features, which are on photoresist, and transfer them to silicon. Here we will have more radicals to come and etch near isolated structures while we are depleted of radicals near dense structures as all of them are consumed. So, the etch rate between these two structures is going to be different and is pattern density-dependent. This will also affect CMP or filling.

The next yield issue is parametric, which is performance-related. So, we discussed timing-related issues; if the timing is not good and if the memory is not yielding the required performance. These are all parametric yield losses. So, that is again another form of yield, which is functional yield. So, the others are mostly structural yield-related issues. Functional yield is often affected by the structural variations that we get during processing.

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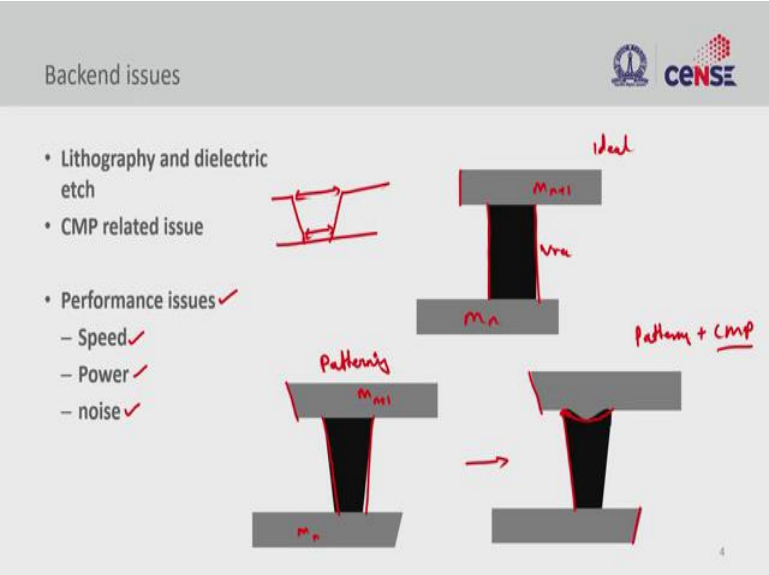

Just to give a few examples of the origin of these various performance limiting issues primarily coming from the back end. Here we are looking at interconnects. So, the slide above shows an ideal interconnect. We have, let us say, metal M_n and metal M_{n+1} connected by via. But after fabrication, we see something like this, which has a sloped sidewall. This is coming from dry etch or pattern in particular. These sloped sidewalls will vary via width; as a result, conductivity will be affected. The resistance is going to be higher compared to what we actually perceived it to be.

The third figure shows another possibility which is coming from patterning and chemical mechanical polishing. So, here you can see you have sloped sidewall and dishing created due to over-polishing. This dishing is again going to reduce the total resistance that we actually get out of this particular via.

These are all structural changes that we get; instead of a very simple via hole, we have a tapered profile, and also, we can have a dishing. This is going to affect performance as well. For example, in terms of speed, because of high resistance, we need to spend more power in transmitting the data, and it will also end up in noise-related issues as well.

Another minute thing that we also want to notice is these sorts of slanted sidewalls in the metal lines, which is again affecting the metal line resistivity. And the other important thing we would also like to highlight here is how we are going to address alignment issues.

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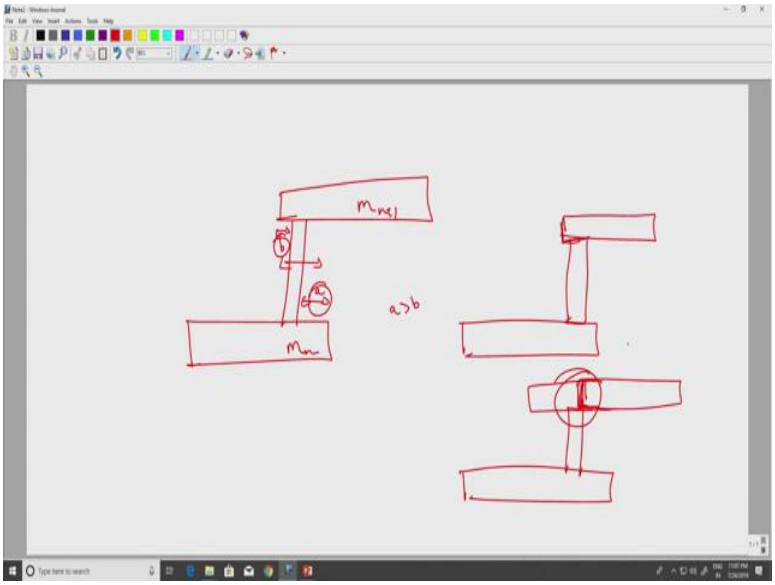

So, we have metal M_n and metal M_{n+1} and one interconnect. But if we look at the distance to the edge, let us say a and b, we see that a is definitely larger than b. Any misalignment that we have left or right connecting to M_n is highly tolerant compared to b. So, we want to make sure that we give enough space or tolerance so that when there is a misalignment, we still have enough metal overlap and avoid an open circuit. If there is not enough overlap, we might have a reliability issue. There might be a small contact; it is just a matter of time where we will have a very high large current field, and electron migration can happen that could result in failure. So, we want to make sure that metal layer overlap is taken care of by applying the right amount of clearance so that we avoid alignment issues.

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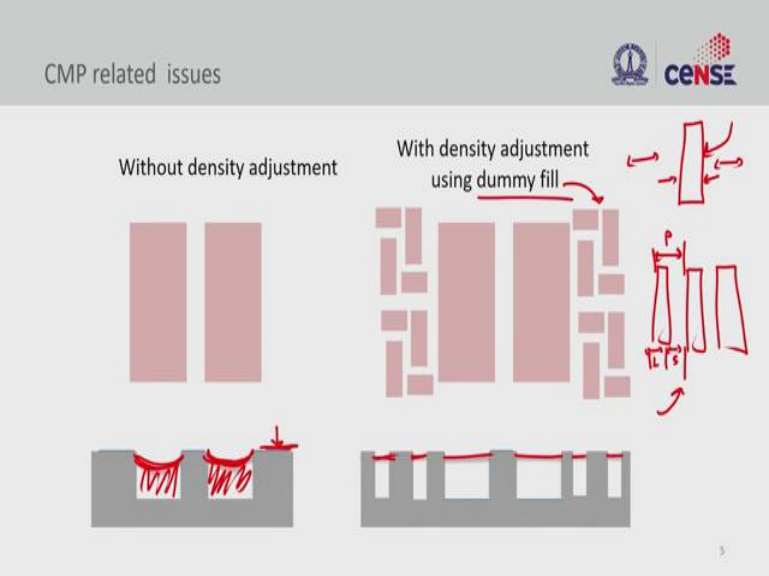

So, the next issue is about filling. We make a trench, and we want to fill it with metal. This is again a via or metal line connection that we are making here. The slide shows the cross-section of such vias. After making them, the area is filled with metal. So, now, we see a dish here that is very severe. But then there is nothing much we have done from the design side or a process side because this is what the designer gave to us, and then we just fabricated it. To make sure we do not have any metal on the pillars, we did some over etch, which has resulted in dishing. But now, if we do a process-aware design, we will add some dummy filling.

So, what this dummy filling will allow us to do is complete a planar CMP. Here we are not going to do over-etching because the metal distribution is equal. This is something we

also saw in CMP that if the metal distribution density is uniform, then removal rates are uniform. We can achieve uniformity by using some dummy structures.

This will not only help us to achieve CMP uniformity but also in etch uniformity. So, when we have structures that are equally distributed, we do not have regions having so much open space. There will not be regions where we have too many radicals available for etching, and in other parts, we are starved of these radicals. So, we want to make sure that we have a clear balance, and dummy fill allows us to do that. This is a very good method to neutralize the filling density.

So, an isolated line is always an interesting structure to study because isolated lines are very simple to fabricate. When we have devices with a varying pitch, then we put a certain restriction here; it should be of a certain pitch, and this line width and space width should be equal, and so on. But then, if you ask any process engineer, it is easy to achieve a periodic pattern with the required specification compared to an isolated line or isolated trench.

The reason for that is the open space that you have; this open space is the reliability or process difficulty, where even the etch is going to be slightly hard because we will have faster etch in lateral portions. And if the isolated lines are not uniformly distributed, we will have to etch depth variation. When it comes to CMP, again, this is a very difficult structure to get a plane finish; we will always end up with a dishing because we have large metal outside the structure compared to on the structure. But when we have a uniformly distributed structure density, it is much easier to handle the process both in patterning and also CMP.

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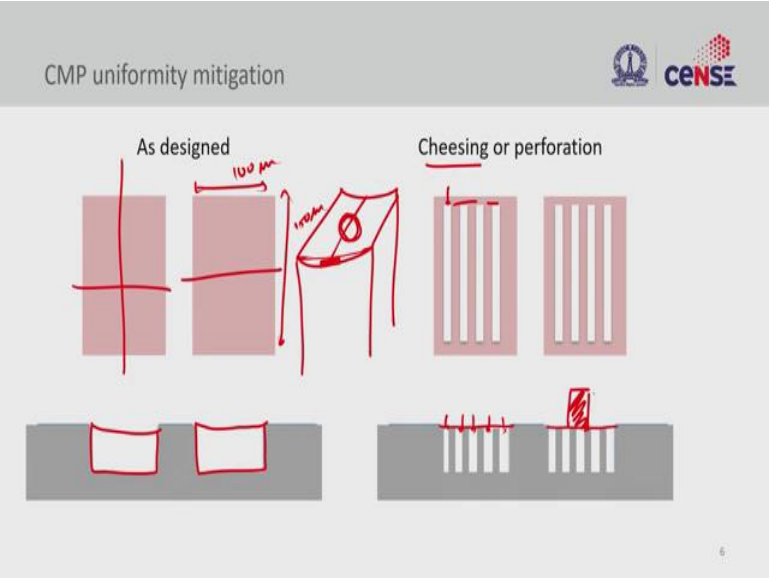

Here we see again an example of the CMP uniformity issue addressed where we take a structure that has a trench that will end up with dishing when the filling is done. As this is a large open area, we will have dishing in both vertical and horizontal directions. So, continuously we will have a boat-like structure. So, we will have high bowing at the centre compared to the edge. This becomes a reliability concern, and also, we are going to make a device or a contact on top of this, then the contact becomes the difficult point at the centre. If we put oxide on top of it and then etch it, we want to make sure it clears everything, but already we have a thickness variation because of this bow.

Another way of handling this is by using perforation. So, perforation helps in addressing this density issue. Let the trench width be of few tens of microns, say 100 microns by 150 microns. What we do is, instead of using this flat open area, we can make this segmented trench. They are all connected electrically at the top. So, when we do this, the filling is going to be uniform, avoiding dishing, and it becomes very reliable. And then we can also have a larger contact that allows to make this further contacting or bumping pretty easy.

This is only a concern at a higher metallization level. So, not at lower metal levels where the structures are much smaller so that instead of dishing, we might have some erosion and so on. When we have large open areas with metal fill or even dielectric fill, we see this kind of issue. So, I am just discussing case by case, but your problem could be slightly different.

We might have a large open dielectric that we are trying to do, or we have a large metal opening that we are trying to get a uniform thickness. So, these are all the ways that we can handle.

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So, the next thing is about interconnect itself; we briefly introduced this earlier, but let us look at what is the problem here. We normally do some single-point contact, and the important thing is to place these contacts right at a very good clearance from the edge. But we may not have the luxury to put these contacts where we want; we may not have enough clearance. In those instances, it will be very hard to place the contacts.

The alternate way of improving this contacting yield is by doubling. So, now, we have double contact. So, if one is misaligned, then we have another contact that will take over and will give us the contact required. This also improves conductivity; we have two parallel paths, and we should be able to pump in more current and be able to do better contacting.

So, this is how one can improve contact reliability. As mentioned, in some instances, we may not be able to do multiple contacts. Then we just live with one making sure that the contact holes are reasonably spaced. But wherever we could add multiple contacts, we should exploit this so that we have better yield. So, these are all the few examples that we can find in improving yield by understanding the process limitation and integration limitation.

So, DFM is all about interfacing design knowledge with process knowledge. As mentioned in the first lecture on DFM, the designer and the fabrication group are not separated anymore, and they should work as a group. This helps the process team and the process integration team understand, what the designer needs are and the same way designer also understand what all the limitation of any process and the challenges that we have in integration are. Accordingly, we can modify the structure and alter some of the circuits that we are trying to realize. So, at the end of the day, we yield the device or the circuit that you want. That is the primary goal. During this task, the designers are pushing the fabrication folks to improve their process and putting their process window to the test, and at the same time, designers are also pushed to think of new ways to improve yield by innovative design strategies, contacting strategies, and so on.

So, DFM is something very important early on in your understanding one should be aware of this. We should not isolate ourselves from only design, not understanding how these devices are fabricated and what are all the limitations. That will only result in miscommunication, and we would not be able to realize desired device and circuit. So, I hope you appreciate the importance of understanding the process while also looking at new innovative design strategies to improve the yield and reliability of circuits and devices.