Fundamentals of Micro and Nanofabrication
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Lecture – 54
Design for Manufacturability-2

Design for Manufacturability is an important area in device fabrication, circuit fabrication, getting the correct yield, and deciding the performance that we want. It is a broad area, as we already saw in the last lecture. So, in this section, we would go through one unit process; to look at how the design for manufacturability could be implemented, while designing or developing a process.

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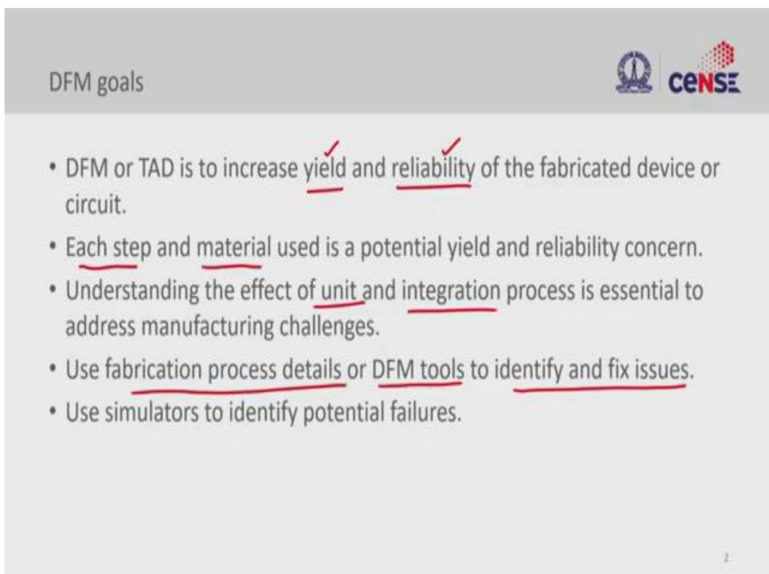

Let us look the goals of DFM. So, design for manufacturability or technology aware design is to increase the yield and also reliability of the fabricated device or circuit. We want to make sure that the device is reliable and also the yield is high so that we can get many devices out of one process step.

Every step in a process and also all the material we use is a reliability concern. So, processing required multiple steps. For example, we saw that the patterning needs optical lithography followed by dry etching. Further, optical lithography involves photoresist, illumination, development and so on. Dry etching requires material exposure to plasma; for instance, if we want to fill a gap with a dielectric material, let us say silicon dioxide.

Potential concerns arise like the reliability of that particular oxide over time; whether the dielectric constant will change over time. So, one needs to be aware of the quality of material and every step in a process.

If we want to achieve high yield and reliability, we should understand the unit process. By knowing the effect of the unit process and the integration process, we can address the manufacturing problems. So, if there is a unit process failure, we should be able to understand the implication of that failure. Or, if the integration process failed between two different steps, we should be able to understand; what is the reliability and yield implications of that? So that we could design our circuits in order to accommodate for such deviation from the optimal process.

We can either take fabrication process details, a complete detail on fabrication process, or use DFM tools; there are tools available these days integrated with design flow itself to identify and fix issues in design. So, as mentioned in the previous lecture, fabrication process details may or may not be fully shared with the designer. However, we can use a PDK that has encrypted data to understand the corners. Also, we can use simulators to understand potential failure. So, we will look at what kind of simulators and how we can do that. Here lithography is taken as an example for unit process

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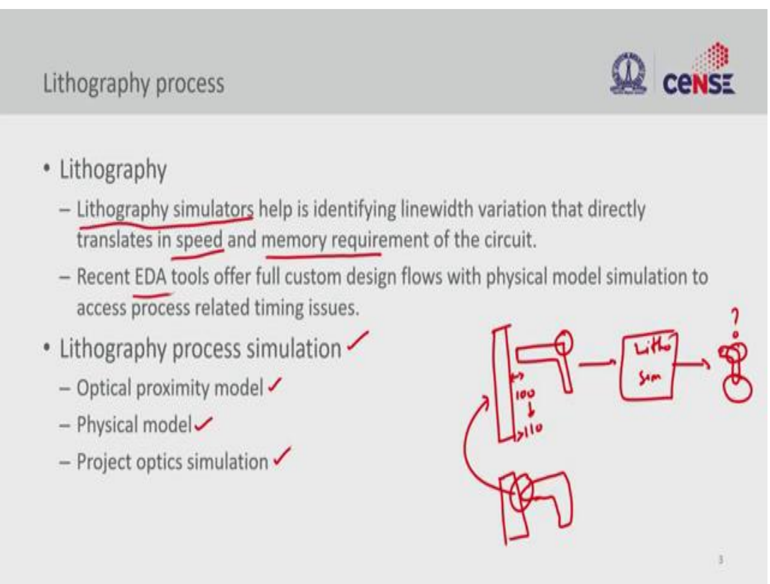

There are multiple simulators available for lithography based on the complexity of circuitry; some are proprietary, some are open source. So, we make a certain design, and

run through the simulator to see the image on the photoresist. We want to understand the effect on the edges, corners; and then use this to understand the parametric-related problems. So, if we are doing some high-speed circuits, we want to understand how these effects will limit the speed. Moreover, if we are designing a complex logic circuit, how the memory requirements of the circuit are affected if we have a lithography limitation. By understanding this, we should be able to design circuits in a better-performing metric.

These days, most of the EDA tools allow doing physical model simulation and extract timing issues. If we are doing a digital design and want to synchronize multiple blocks with a synchronized clock, we may want to have the clocks aligned without any delay between the different blocks. If one block is relatively slower than the other, we might miss the timing and the entire logic will not meet the requirement. Here we wish to know whether the timing will be affected because of the physical design or what is the margin available. So, all those things could be done using present-day design tools. When we say litho process simulation, this could be related to optical proximity correction.

So, if we have a line lying close to the particular structure, we want to have a certain clearance between these two and also want to look at these edge effects. In that case, we can run the optical proximity model on this particular design, and the model will tell us where to add or reduce features to counter the proximity-related issues. We can use a physical model and do a complete projection lithography simulation as well. The proximity model is much more refined, but the projection simulation can give the variations in line widths; whether it is widening or narrowing, all those effects could be extracted from the projection simulation. After the simulation, we will have enough information to correct those designs. In advanced tools, we can extract all these defect points or the locations to be addressed in the design. If there is a very narrow gap between the structures in the design, and post-simulation if the gap merges, then the gap can be increased to say 110 nm instead of 100 nm based on how much overlap we had from the simulation. So, the circuits can be made more robust to unit process variation or limitation, increasing the yield. So, we get better manufacturing capability when we go into the details of each and every hotspot.

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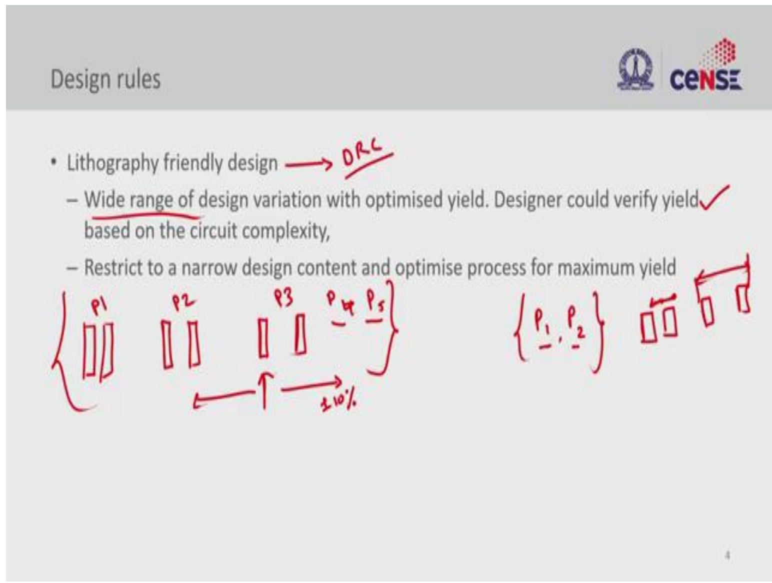

What we get out of this is a design rule which will help in making lithography friendly design. The first point in achieving a litho-friendly design is following DRC, a design rule compliance. Once the design rule is cleared, it is presumed that all devices are on spec, and we do not have to worry about yield. However, that may not be true; physically there are certain limitations and that will be used to define this DRC.

There are the two instances that can be used to make lithography friendly to design. First, we define a wide range of design variations with optimized yield. What do we mean by wide range of design variation. So, the process itself will allow multiple variations. So, let us say we have five different pitches; pitch 1 to pitch 5.

The process may allow all of this to be fabricated with one single lithography process. So, this gives a wide range of designs that we can use for a complex circuit. As we are not restricted with one gap or one linewidth, we might think of it as a perfect design. But the problem here is, the lithography may not be optimum for all five pitches. Probably it was optimized for pitch 3, let us say, while the window was achieved between pitch 2 and pitch 4; let us say the window here is $\pm 10\%$. But then when you are designing you presume whatever pitch that was given to you that is available; you presume that all these pitches are optimal, that may not be true right.

When the design has multiple variations and also if the lithography process also allows printing all of them, we should be little more cautious about the yield on each of these

designs or each of this pitch. If they are suboptimal, then we may want to rethink our design complexity; we do not want the circuit to rely on the narrow process window for individual pitches while there is a global overlap. So, one needs to be very careful about that. It might be very attractive to have a wide range of design to fabricate; but whether all of them will yield to our requirement is a question to be clarified.

The next way to improve yield is by restricting the number of designs that are allowed. So, instead of five designs, we will allow only two; pitch 1 and pitch 2. This will give a maximum yield because there are only two structures that are allowed. In this case, we can expect a tighter control of variation for these two pitches. It might be a little difficult for the designers who intend to have variety, but this will give a high yield and reliability. So, there are both advantages and disadvantages in going for variety having complex circuits. We have to note that if we cannot yield all the variations, the performance of the final circuit may not be optimal. But, on the other hand, we restrict the available design to one or two that will pressure the designer to comply with only these two variations, but then yield is going to be high. So, is the reliability.

So, there is always a trade-off between these two, and it is up to the designer to choose the rules and designs to yield better circuits.

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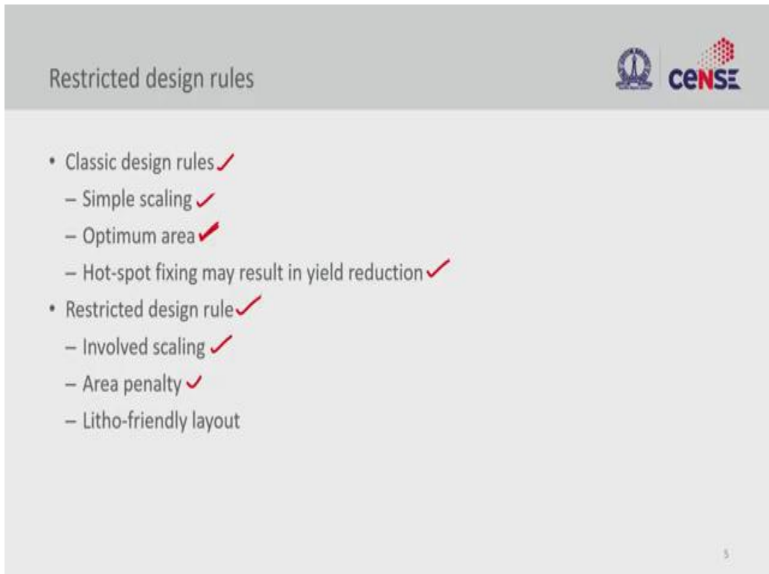

There is a difference in using the classic design rule and the restricted design rule. When we say restricted design rule, this is the follow-up of what we just discussed earlier; to

restrict to certain configurations, where the yield will be high. In a classic design, it is a very simple scaling strategy. We can use an optimum area to do this because the design variations are high. We can identify and fix the issues which may result in yield issues. So, we have to identify every hotspot, and fix it. Whether the fixing is going to be optimal or not is again a question. We can use large areas here; because the classical design does not restrict to use only a certain footprint as the scaling is very easy. Because if we use five designs and each of them is yielding at a certain percentage, then we should be able to apply these designs all over circuit.

The restricted design involves restricted scaling. So, we cannot increase the density or may not be able to play with multiple dimensions that freely. There is a problem with the area as well. Since we are restricting, we want a higher yield. So, this yield could only be guaranteed for a certain area. We would not be able to scale this independent of the rule or yield we are looking for. The expected yield numbers that we get out of this DRC is restricted to a certain area. And once we do all of this, we get a litho-friendly layout. So, once we have a litho-friendly layout, we are guaranteed that the output or the device will yield a higher percentage and be reliable.

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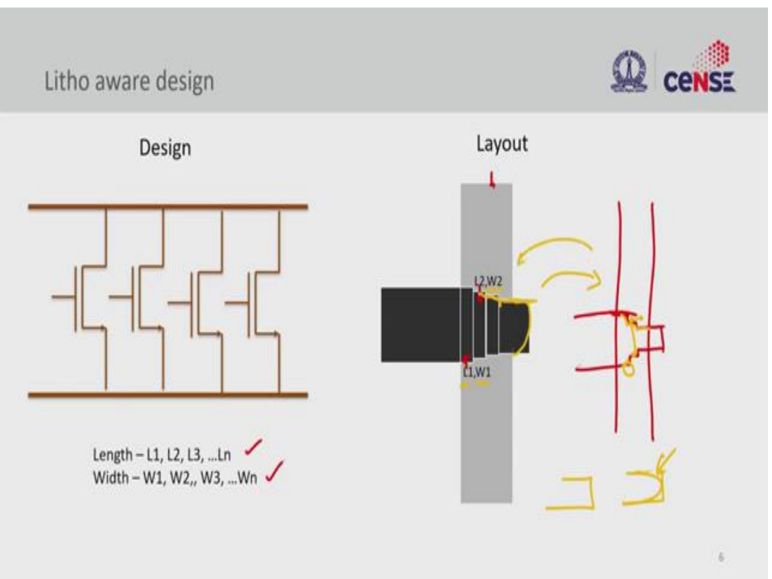

Here is an example of how one can do a lithography aware design; on the left side is just a stick diagram of the design, and on the right side is the layout. So, we have here four transistors with varying gate lengths and widths. In the layout, the gate, central channel is

defined as rectangles. But when fabricated, we get blunt corners instead of sharp transitions. So the effective length and width are going to be very different. Also, this rounding of the lines is undesirable if we want to extend the lines and connect to another line. So, one needs to be careful about what we have on the layout and the design. Also, avoid these kinds of rounding to get the desired dimensions by modifying this design.

If we understand the deviation from the expected design, we can design the layout in a proper fashion. This is what we call layout-aware design. By having prior knowledge of how the design is going to get fabricated and how it is going to yield as a circuit, we can come back to layout and fix issues.

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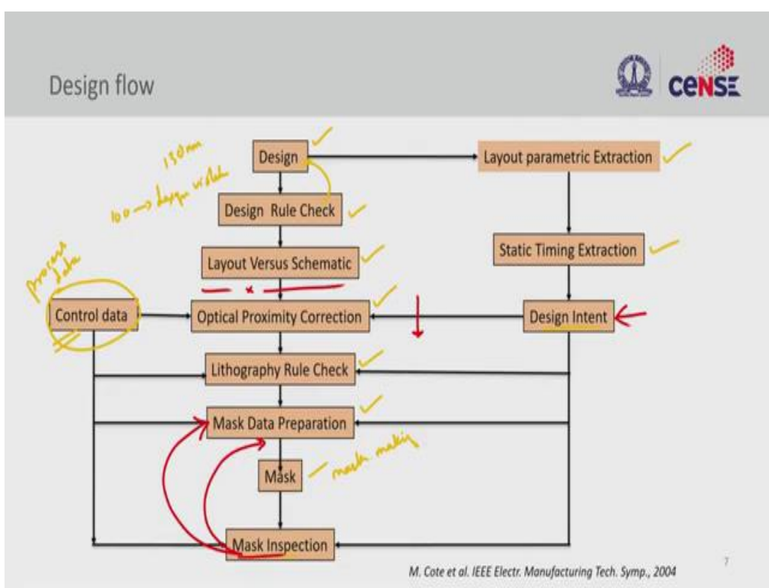

Here we see the general design flow; first, we start with the design, and then we run the design rule check; This is a very standard procedure for checking any violation of design. So, for instance, if we are designing a 130 nm node and the structures are 100 nm or below 100 nm, then the design rule check will be negative. So, if my structures are 100, then there will be a design violation. Then we can condition the program not to allow any design below 130 nm. The next step is setting the layout; how the transistor should be fabricated, how they are connected. These layouts are then checked with the schematic. Here few checklists are looked for, like whether all connections are correctly done? Are there any shorts or any open connections? Are the shorts and open connection swapped? Do we have any overlapping regions?

Along with these refinements, we also send the layout parametric data. So, after designing the first step is to extract the functional parameter. So, we design this particular circuit for a certain functionality. For instance, we design a digital circuit that will do something, but then there are synchronization data, there are timing data between different blocks. So, all those parametric details are collected and used for later use. So, this is intention aware intended application should be very clear.

After looking at the layout, the next thing to do is proximity correction. In proximity correction, we simulate the outcome of lithography. So, we check whether the structures are going to come out the way we wanted. After the proximity correction, we check it with design intent.

We have already extracted the timing and everything. Now, we are going to do all these extractions again of the proximity corrected circuit. We are going to check if the circuit yields the same performance after the proximity correction. That is what we will do by supplying this design intent data to the corrected layout; and this correction is done by using your lithography details.

This will be followed by a lithography rule check, and then we have the mask data and mask inspection data. Here, the control data is nothing but the process data. After the lithography process, we will get to know its limitations. Then, we will feed these data for optical proximity corrections, rule checks, data prep, and mask inspection.

Now, the process is very involved; because we involve how the device will look after fabrication. So, even before fabricating the mask, we will check whether the current design with certain process specifications will yield the desired circuit or not. So, that is the beauty of this whole process flow; it is very involved, but we will get better circuitry in terms of both the yield and reliability.

After the optical proximity correction, we do a lithography rule check, which is again a kind of design rule check. However, in this case, it involves projection simulations as well. Once the litho rule check is done, we prepare the data for mask writing. As it is a writing process, we need to find the positions where we want chromium and transparent. So, once it is prepared, we make the mask. Then we do an inspection which allows to find defects. If found, we do the corrections again. So, there are two types of defects; one is a random defect that could happen because of process variation or some process failure during mask

fabrication, or data preparation itself. If the data preparation was not clear and if we face some systemic failure in the mask writing, then we go back to mask data preparation, and fix that problem before making the m ask. Once these are done, then we can go ahead with fabrication.

Some of this involved process is taken care of by the designer until the layout comparison with the schematic and the rest is taken care of by the lithography team. However, the interface here is this design intent. So, what is the purpose of our circuit; we share this detail with the litho team, and they are going to use those data to do the timing analysis after doing proximity correction. In some cases, it is given back to the designer to run the timing analysis and also window and so on.

So, it is very important that there is a closed communication between the designer and the mask preparation team so that the designed circuit gets fabricated with the required parametric performance as well, not just the structural yield. So, the fabrication might yield a line. But the line must have the required resistivity if we are going to look at the timing.

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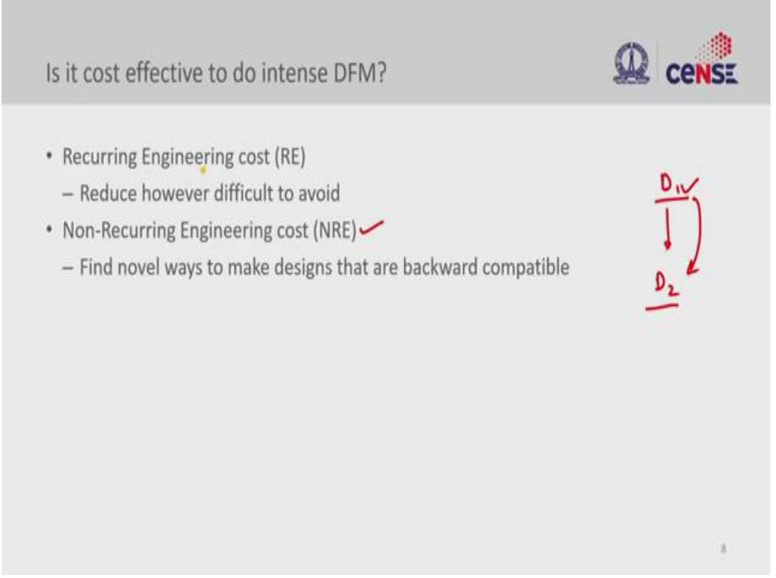

The entire process takes a lot of effort and in turn costs human and other engineering resources. We have to spend some cost on it; this can be hard cash, or time. There are two types of expenses that we have in a product; one is recurring engineering cost and the other one is non-recurring engineering cost. It is very hard to completely avoid recurring engineering costs; we can try to reduce it bit cannot eliminate.

But the non-recurring engineering cost can be wholly avoided going from one product to the other product. Say, two devices, D_1 and D_2, share majority of layers and structures in terms of layout. Let us not worry about a gate thickness variation between D_1 and D_2, which will not affect too much of the layout; if the line widths are maintained, then we are ok.

So, there are few design parameters that we can still keep unchanged going from one generation to another generation. So, this may be related to one generation of a node to other; but primarily the same node, which does different functionality. So, in this case, by having good compatibility between different device generations, we can avoid engineering costs.

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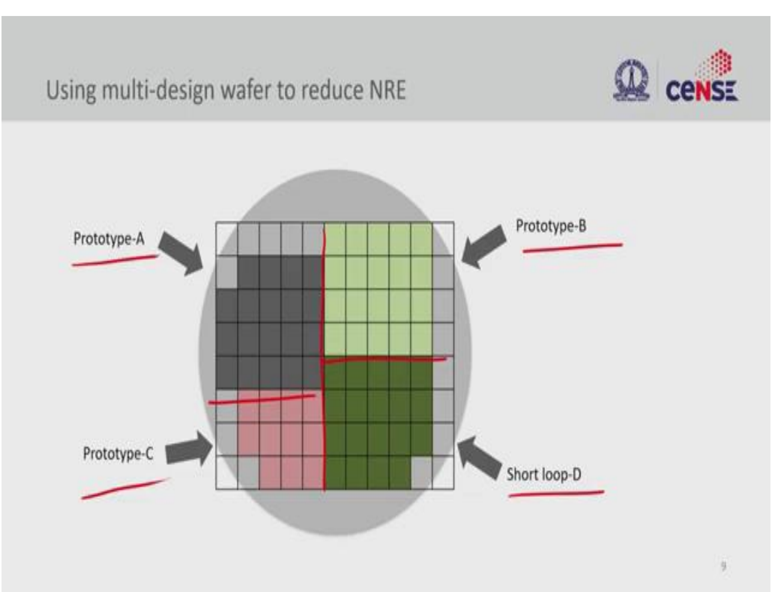

Another way to reduce engineering costs is by doing multiple tests on a single wafer. So, a wafer can be divided into four quadrants. We can have the prototype for device A, product B, product C, and some short loops to check some functionalities for product D all on a wafer. This is how we can reduce non-recurring engineering costs without wasting full wafers just for the development or proof of concept of a prototype. So, if prototypes can be shared, we can designate different spaces for different devices in optical lithography. Here, by using a part of the wafer, different circuitry can be tested while the processing like litho, etching, metallization is the same. So, this is how we reduce the non-recurring engineering.

So, with that, we understood how just lithography alone could help in DFM. Each unit process could contribute towards DFM in this way, where we are closely looking at the process variation; and then using those process knowledge to make the devices and circuits yield better. So, the design for manufacturability is very specific and detailed, like what we saw in lithography just alone, and we can apply the same for multiple process steps as well.

In the next lecture, we will see how to use DFM for doing backend and so on.