Fundamentals of Micro and Nanofabrication

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Lecture - 53
Design for Manufacturability-1

In this lecture, we are going to look at a design for manufacturability. So, design for manufacturability, or DFM in short, is a very broad area. As the name suggests, we have to design for manufacturing; the terms manufacturing or manufacturability are interchangeable. So, the whole idea in DFM is to understand the manufacturing process and apply the limitation of the manufacturing process in the design phase itself.

Initially, design and manufacturing were two different entities. So, the designer never interacted with manufacturing units. Whatever we design, we expect those designs to turn out to be as good as possible, relying on the manufacturer to give whatever we desired. But more often, there are certain limitations in manufacturing itself. There are variabilities, and there are some dimensions and some specifications that may or may not be achievable in manufacturing. So, there was a big misunderstanding between these two that resulted in the waste of resources more often. This also happens in research these days.

So, when we are developing a certain device or circuit, we should always keep in mind, how are we fabricating this? If, this device or circuit cannot be fabricated using the existing methods or whatever technology that we are going to use then there is a very little scope in exploring the applicability of the device or circuits that we are developing. So, it is very important to understand whether the designs can be manufactured or fabricated taking into account all their non-uniformities and variability's that one would encounter in manufacture.

So, ideally, as a designer, we design a circuit, we might have calculated the come up with values for, say, line width, the gap width, the resistivity, or the doping concentration. We might have a very good simulation platform that is telling us that this will be the best device that we can get. But if we cannot achieve all those specifications, then it does not matter whether it is the best device in simulation. Moreover, if we cannot fabricate, there is no usefulness in having such a design. It just remains as a design that we cannot realize. If, we want to realize such a spectacular device, we should understand the manufacturing

limitations and the variabilities to incorporate those in the design stage and achieve devices and circuits that can yield better results.

So, in this lecture, we are going to look at the overview of design for manufacturability. The topic itself is pretty broad, we can use DFM for mechanical manufacturing, computer science, microelectronics, chemical plants, and chemical engineering. So, the applications vary, but some underlying ideas are fundamental to the field we will apply.

In this lecture, we will not go deep into any specific field. However, we will try to understand the underlying principle and what one needs to be aware of while understanding the design when it comes to manufacturing.

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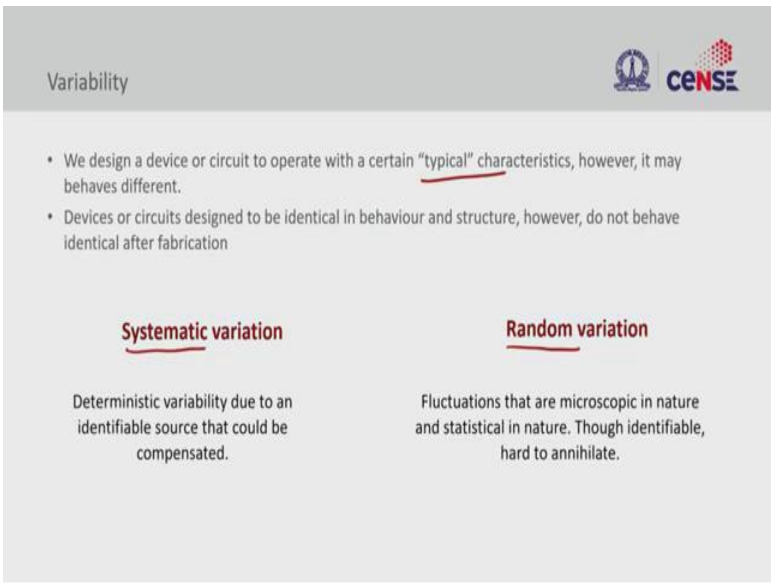

The first thing that comes to mind when we are looking at DFM is variability. The whole idea of a design for manufacturability is because of variabilities that we get during the fabrication process. So, we design a device or a circuit and expect that it should give us a typical characteristic. But when we get the device, it may not give the typical characteristic that we are expecting.

Also, we might have multiple devices, multiple circuits, that should have identical behavior, and we have designed them identical, let us say, in our layout. We can do copy-pasting; let us say we have just copy-pasted one block to the other die. But, when we get

these devices after fabrication, we find out that they are not identical. So, this is all coming from variability during the manufacturing process.

There are two types of variability or variation; one is systematic, and the other is random. The systematic, as the name suggests, is deterministic variability. So, it is due to an identifiable source that could be compensated. Systematic variations are the variation that could be traced. So, we should be able to find the source of this variation, and also, we should be able to apply some compensation method to counter the systematic variation. On the other hand, a random variation is a fluctuation that happens at the microscopic scale and, they are statistical in nature. We might be able to identify the source, but the source itself could be uncontrollable. So, it is very hard to avoid this random variation altogether; however, we should be aware of this variation that exists in the fabrication process.

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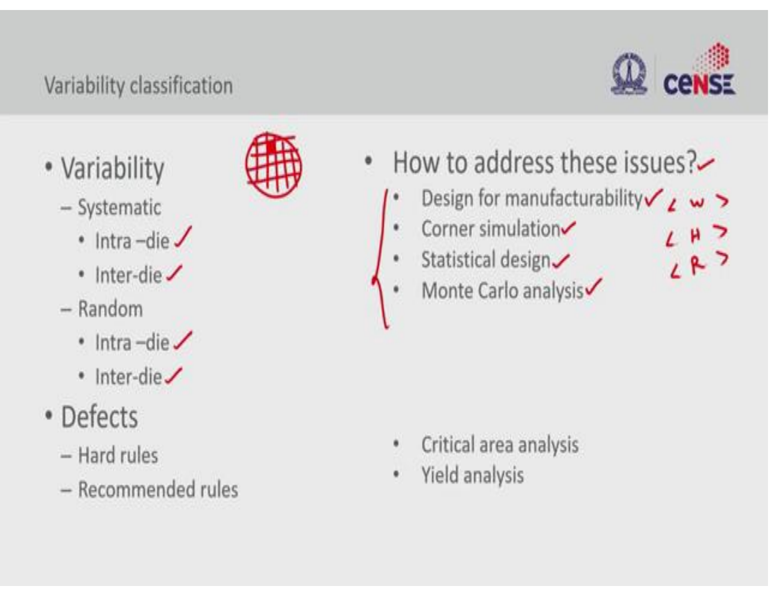

As we saw, the variability could be classified as systematic and random, and both could be further classified as intra-die and inter-die. The die here means just the chip. So, if we take a wafer, we can have multiple chips inside this footprint, and each of these chips is called a die.

Intra meaning, the variation is systematic or random within the die while inter means between the dies. These problems can be addressed by looking at the manufacturability of the design; whether our design fits into the manufacturing protocols, we can do simulations.

By taking the manufacturing protocol and looking at what is the width window that we have, what is the height variation that one could have and, for instance the resistivity variation that one could have, we could do a corner simulation. So, if width variation is within this window, how the device going to behave?

We could do a statistical design that is primarily for random variation. We can look at whether the random variation follows a Gaussian spectrum or a completely normal distribution or undetermined. So, there are multiple ways to take the data of this random distribution. Then we can model it, either throwing Monte Carlo or any other simulation to look at the device performance in the presence of random and systematic variation.

The next thing is defects which is slightly different from variability. Defects can be originated from hard rules; if you have violated a design rule, then it becomes a defect. And, also there are few recommended rules that may or may not affect the performance, but this is also a defect in a conventional sense.

So, we should be aware of the design rules and all the mild rules and whether the mild rules become hard for the design. The mild rules could be for the process, but if that mild rule becomes a hard rule for design, it becomes a hard defect. So, in order to understand that we should do a critical area analysis; if within an area some rules apply, then whether the chip or the circuit area will be affected. Also, we look at the yield of the circuit or device based on these defects.

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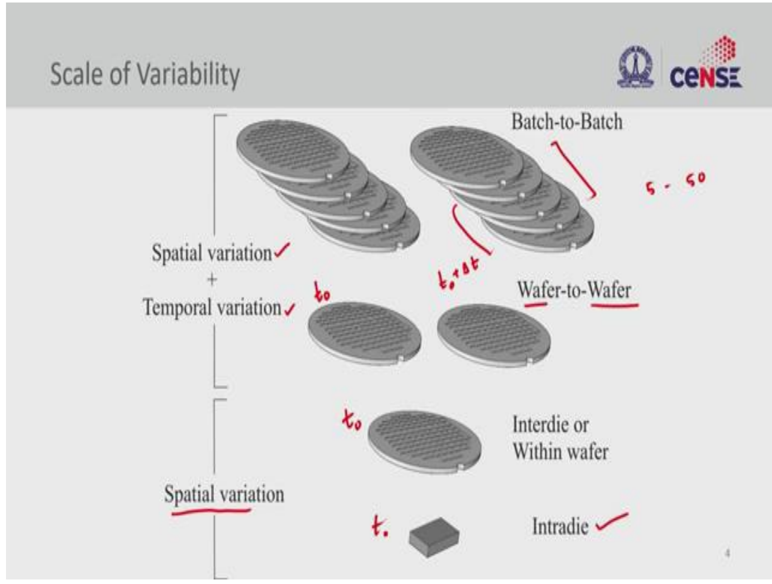

So, the variability can affect at various scales. In the last slide, we mentioned something about inter die and intra die. So, in an intra-die, i.e., we take a single chip, the variability could be within that chip. We might have two amplifiers design on the same die, but then these two amplifiers behave slightly differently; the gains, the threshold voltages are slightly different. Variability could be between the dies also; within a wafer, we can have inter die variation. These come under spatial variation, because this wafer is processed at a particular time t. So, there is no time lag between the two dies because this is parallel processing, and everything is done at t_0 let us say. If we go from wafer to wafer, we have both spatial variation and also temporal variation So, one wafer was done at t_0 and the other at $t_0 + \Delta t$.

Here, spatial variation is any non-uniformity on the sub substrate with respect to distance or position. The temporal variation is the difference in time; we process one wafer now and another after 10 minutes, but at the same process. But, between t_0 and t_1 few things might have changed. For example, there might be a change in the temperature of the chamber or the environment, or the wet chemical we are using. So, this will also affect your variability.

A group of wafers is called a batch. The number of wafers in a batch depends on the fabrication unit; it can be anywhere from 5 to 50 in a single batch. Within the batch, and also, batch to batch we can have variability. This is where we have both spatial variation and also temporal variation. So, the variability becomes harder and harder to mitigate.

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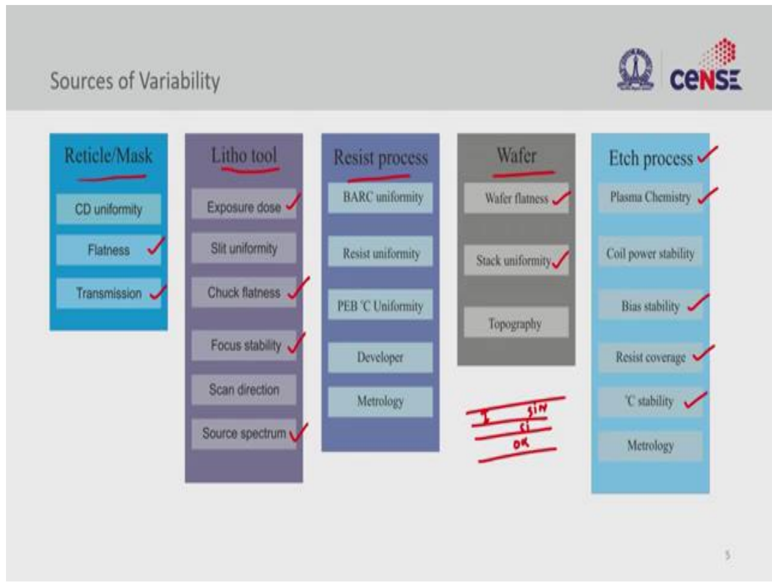

So, here we are just trying to capture three processes; wafer, lithography, and etch. So, let us look at the possible things that can go wrong or that can create variability. If we look at it, everything that goes into the processing can induce variability. Just to give an example, we take a mask. So, the mask flatness could give us some variability. Ideally, we expect the mask to be flat. If the mask is not flat, the bow in the mask can affect diffraction. The transmission variation can also result in variability.

Let us look at the lithography tool itself. There could be variation in exposure dose, the chuck flatness; chuck that is holding your wafer. There could be focus instability and source spectrum might be slightly shifting. The resist process and the wafer itself could have variability. If the wafer is not flat, it is going to affect the focus. Similarly, stack uniformity; if we have multiple layers, say a stack of oxide, silicon and then silicon nitride, any thickness non-uniformity in these layers can result in reflection issues.

In the etch process, any change in the bias voltage, temperature, resist coverage which is the density-dependent issue, can result in variability. The chemistry; if the chemicals are not mixed properly, density variation of these radicals within the plasma will also give rise to variability. The variability can be in terms of line width or etch depth. So, when we process a wafer, the parameters that dictate a process are responsible for this variability.

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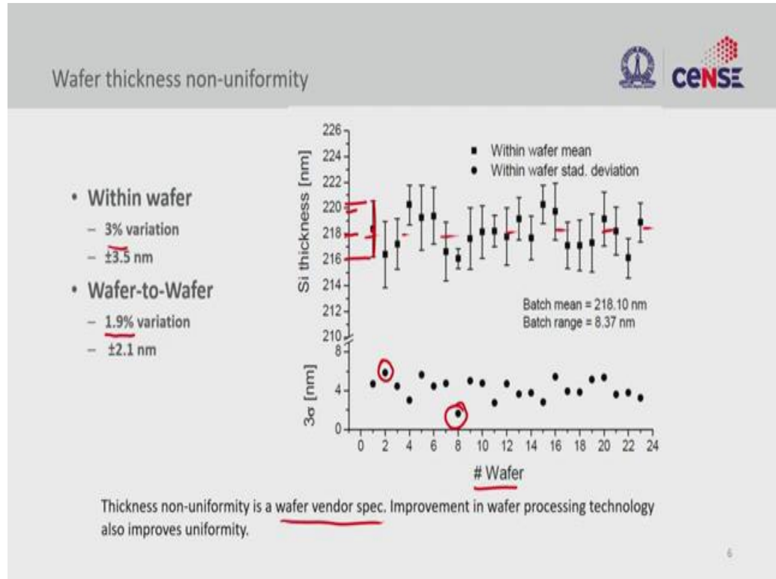

Here is an example of thickness variation. We see the silicon thickness variation and 3σ plotted against the number of wafers. We have variations in between wafers and also within the wafer. Within a wafer, we have a pretty large distribution around the mean, and the standard deviation of the thickness is around 4 nms. Among the different wafers, we have some good wafers with low variation, while there are also wafers with high 3σ values.

The intrinsic thickness variation can also contribute. For instance, within a wafer, we could have 3% variation in thickness, and wafer to wafer can be 1.93% variation. Uniform thickness between the sample dictates the final result. So, one needs to be aware of this variability if we are going to process a large number of samples.

When we are buying a wafer from an external vendor, the specification is given by them. So, we do not have much control over uniformity. However, over time, the thickness uniformity is also improving, which is something very good. It is important to be aware of the thickness variation, which may or may not affect the design based on the critical nature of the design with respect to thickness. If our thickness variation is 1 nm and the device would not work, then we may want to relook at the design. Because here we have a range of about 4 or 5 nm. So, if the thickness variation is 4 nm, we should make sure the design can accommodate this 4 nm variation. Because we do not know where this device will sit on the wafer, whether the device will sit on the part which is 218 nm or it is going to sit

on 220 nm. So, there is a 2 nm variation already. Whether we will be able to support this sort of variation or not is a critical question that one needs to answer.

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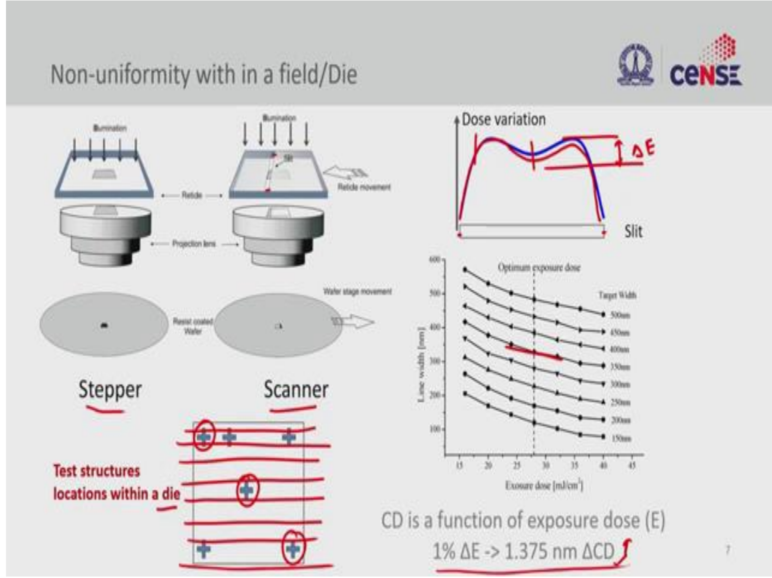

And, the next thing is again related to a lithography exposure itself. So, we know that when we change the exposure dose, the line width changes. Let us look at the stepper and scanner example. So, in the illumination option, if it is a stepper, we have a flat illumination of structure, but we have a thin slit in a scanner.

The assumption here is that the slit has uniform illumination or uniform intensity, but in reality, we do not have that uniformity; we will have a certain change in the intensity profile from one end to the other. We should be aware of this variation ΔE. If we take a simple die and scan through the slit, the slit will give a certain dose over this wafer. If we have identical devices in these points marked across and measure all these devices, they will not give the same response. This is because we have a certain dose at the center, and at the edge, we have a different dose. The variation in intensity exposure dose will result in a slight variation in CD. We have seen this in lithography as exposure latitude which we want to reduce.

For instance, 1% change in the exposure dose could result in a change of 1.3 nm in the critical dimension in a highly controlled system. But, if the system is not really tuned and controlled, we can expect CD change to be much larger. So, we need to be aware of non-uniformity in the intensity, which can also cause variability.

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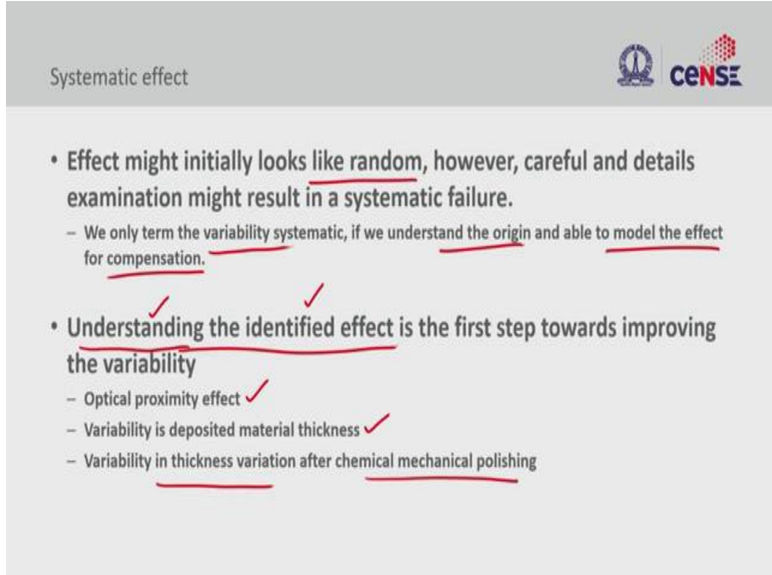

The systematic effects can be traced back. So, we call variabilities systemic only if we can understand the origin and model the effect for compensation. If we can identify but cannot model the effect, then it becomes a random issue. So, if it is systemic, we should be not only able to identify and understand the origin and but also able to compensate.

What kind of failures are systematic? We should first look at the effect, which may seem random because we encounter it for the first time. So, we have to run multiple tests, multiple experiments and examine the data. Then we will see that this random nature is not random; it is actually systematic. One of the experiments could have resulted in the conclusion of a random effect. The repeated measurements can give us a clear indication that it is systematic.

Understanding the identified effect is the first step towards improvement. Once we understand and identify the effect, then we can attack the problem. So, we should not blindly start cleaning if we see a particle. We should identify the source of these particle defects and annihilate them.

The particle defect might be seen in the next wafer also. It becomes resource-heavy, if wedo not address the problem.

So, that is why understanding the problem and identifying the effects are the primary steps in addressing the variability. The variability could be optical proximity effect, which needs

thorough investigation, and also, we could have thickness non-uniformity during deposition. In a plasma process or a CVD process, improper flow rates, wafer placements might also result in variability.

So, once we encounter a variability because of deposition, the best thing to look at the process that we are running, whether the process in itself is outside the process window or not. In chemical mechanical polishing, we could have local variability and global variability in thicknesses. This could be either from the process or from the design itself. So, we need first to understand the origin of the problem and then address it. This becomes a systematic understanding of the problems that we encounter.

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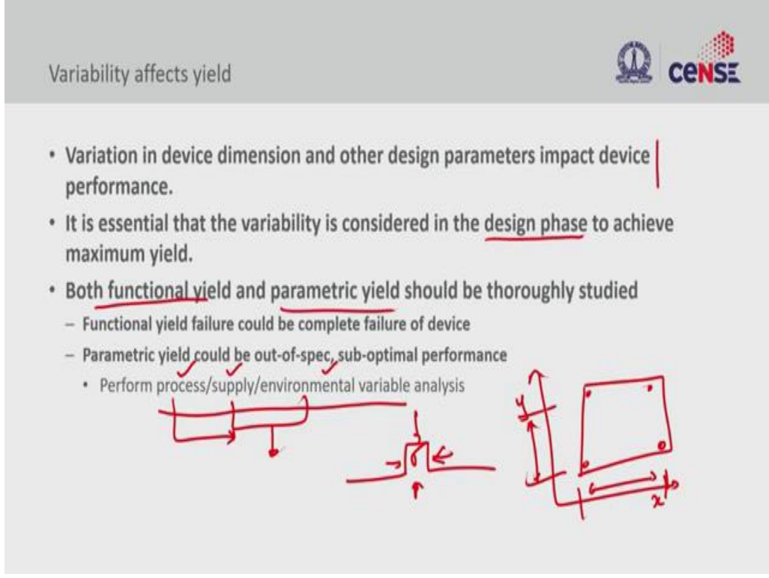

The variability also affects yield. We know that variations in dimension or any other design parameter impact the device's performance. Whether this impact is terminal or not is the question. It is best to include the variability during the design phase itself. As mentioned previously, we should do a corner analysis. We take parameters x and y that will affect the device performance and run the window for x and y. We then look at the performance of this device and check whether the figure of merit of this particular device is within spec or not.

So, if not, then you have to redesign because the process window that we have is hard. We either request foundry or the fabrication facility to tune the process to get a better process window or redesign. More often, we will be given a window because re-optimization is an

expensive process, probably they have done the best to give the window that we can use for better yield.

However, if our device is not yielding within that window, it is better to go back to the design board and design to the window that we got from the fabrication facility. So, we need to do two things: functional yield analysis and parametric yield analysis. The functional yield analysis looks at whether the device is working or not.

In parametric yield, the device will be working, but it is out of spec or working suboptimally. So, in that case, also we need to do an analysis of these three important factors; the process variation, the supply variation, which can be input power or voltage, and environmental variation, like variation in temperature. As a designer, we will do supply and environmental variation, but then we should also do process variation. Because, when the process variation happens, we will have a change in line width, or height, or it could be the material itself; the properties like resistivity of the material could also change. So, we need to incorporate all of these parameters to look at parametric yield.

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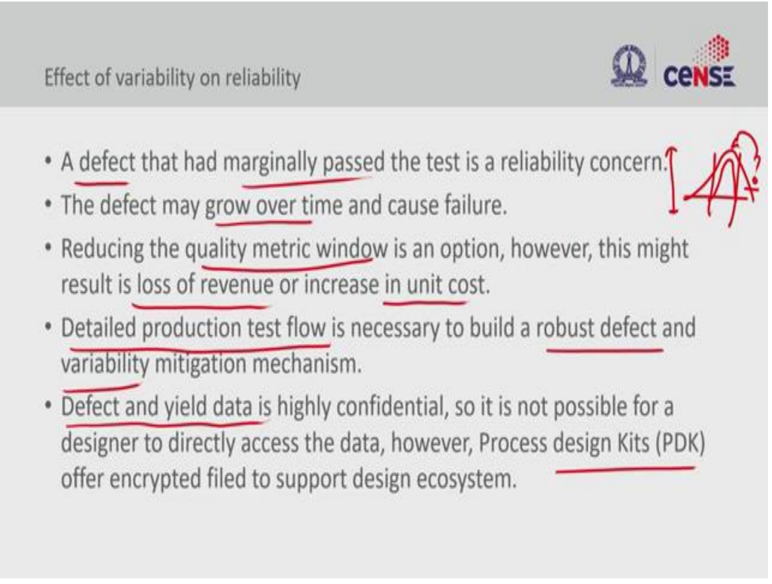

So, the variability of the device or circuit has a direct implication on their reliability. A defect that has marginally passed during the test is a concern for the reliability. So, the defect that we identified could grow over time and cause failure. If this happens, then your customer would not be happy, and also, when we are running long-term measurement, if it fails, we have to redo that experiment again.

In order to take care of these defects, we can reduce the quality metric window. Let us say we have a distribution. We can tighten the distribution; say, we will allow device with a certain metric, then that will give us better reliability. But the unit cost will increase. Because, the devices that are outside the window will be wasted. So, their cost should be considered while costing for the device that we sell and also will result in a loss of revenue. Therefore, one needs to be careful about choosing the right quality metric window and the defect analysis here. So, addressing defects is more important than working towards quality metrics.

To understand and mitigate the defects and variabilities, we need a thorough test flow. So, we have to test the quality properly whenever we get a wafer or a device is made. We can make the first batch and then feedback to the designer regarding the required changes needed in the design.

The defect and yield data are highly confidential. So, we will not get these details from the fabrication facility or any manufacturing facility. But we get Process Design Kits, PDKs, which have support design data to help us understand the yield and defect. These are all encrypted and will have all those details to run the corner simulations and so on.

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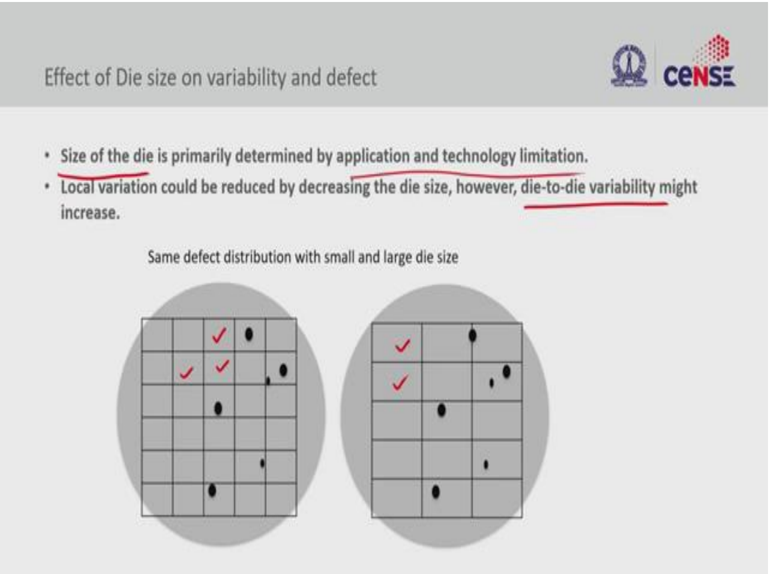

Now, we shall look at the effect of die size on variability and defects. We have two images here, both are of the same size wafer, but the only difference is the die size; on the left side, we have smaller dies, and on the right side, we have larger dies, but the defect density

remains the same. So, if we reduce the size of dies, we see that more number of defectless dies are obtained. We should also look at die-to-die variability, which also affects the uniformity when we are building a system using them.

So, it is all about respecting the defect distribution. In some cases, we may not be able to reduce the size of the dies also. So, the die size is primarily dictated by application and technology limitation.

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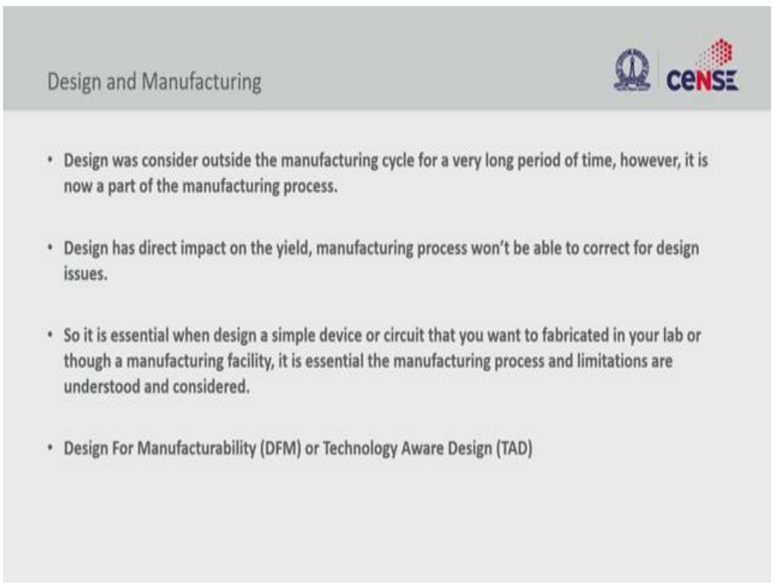

To summarize, initially, the designs used to be separately done, but now design and manufacturing are put into a single process. So, design is now part of the manufacturing process itself; we give feedback to the designer from the manufacturing process to design better circuits and achieve better yield and reliability. When designing even a simple circuit or a device, we must understand the limitations of a lab or fabrication facility so that they can be fabricated; otherwise, they will never be realized. So, design for manufacturability is one word. The other term like Technology Aware Design is also used, which thrives on the same idea.

So, this brings us to an end of the brief overview of design for manufacturability. So, as mentioned, design for manufacturability is a very broad area. Here we tried to create awareness about, the places you could expect this variability, types of variability both in terms of spatial and temporal and sometimes both spatial and temporal together.

There are limitations to the manufacturing process. So, one needs to understand those limitations and design accordingly. It is possible to design a suboptimal device, that has high yield and the best device having poor yield. It is something that one should be aware while designing. So, make sure that we understand the manufacturability before venturing into manufacturing.