Fundamentals of Micro and Nanofabrication
Prof. Sushobhan Avasthi
Centre for Nano Science and Engineering
Indian Institute of Science, Bengaluru

Lecture – 45
Wet Etching Recipes

We shall continue the module on subtractive processing, specifically wet etching. This lecture will conclude the wet etching discussion. We shall look at some more recipes; gallium arsenide etching, defect etching, and some metal etch and end with an exciting process called lift-off, fundamentally an etch process, often used for patterning metals.

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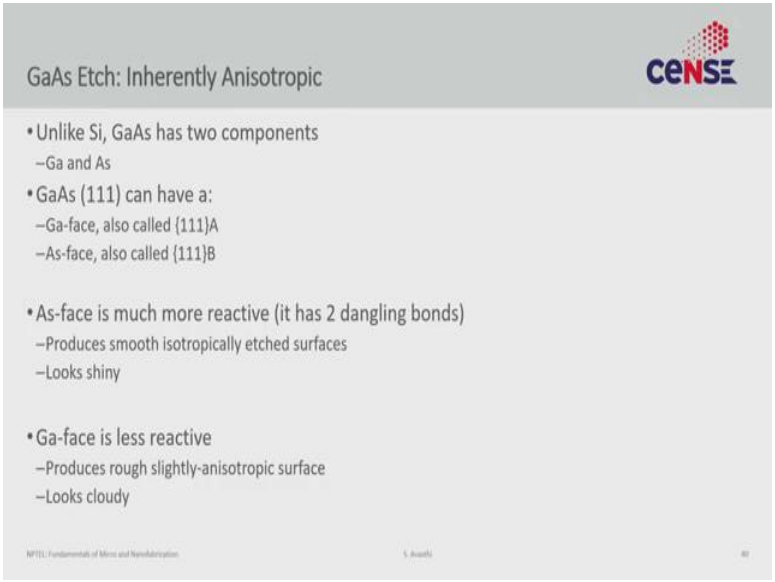

In the last lecture, we discussed silicon anisotropic and isotropic etch. The silicon isotropic etch had three components; hydrochloric acid, nitric acid, and acetic acid. We had also discussed iso-etch curves. We also looked at how the concentration of these components affects the etch.

Gallium arsenide is another very popular semiconductor; the etch is functionally similar to silicon, but the chemicals are slightly different. For most compound semiconductors, the etches become relatively complex with the chemistry of the material. As GaAs has two elements, GaAs (111) can have a gallium face called {111}A or an arsenic face, {111}B. We have to distinguish because you get chemically different outcomes if the etchant sees gallium on the surface vs. arsenic. The fact that gallium has a valency of 3

and arsenic 5 complicates the matter. You can argue that the arsenic face has more bonds than the gallium face, and hence, the etching rate would be different also for that reason.

In a multi-component etchant, we have to think about the effect of individual etchants. If the semiconductor is also complicated like GaAs, we have to think about which facet or orientation we are etching. It becomes even more involved with a tertiary material. It becomes increasingly challenging for the complex materials to find truly isotropic etches, as there is no isotropic property that you can use to design an isotropic etch.

The canonical GaAs etching is anisotropic. There is no isotropic GaAs etch per se, as the As-face is much more reactive. It etches faster because As has a valency of 5 and has two extra dangling bonds on the surface than Ga-face. These reactions diffusion rate limited, and not surface reaction limited, so they etch isotropically and leave a shiny surface. It is advantageous if you are making optical devices with GaAs. Ga-face is less reactive, so the etch is often surface reaction rate limited. Hence, it is usually anisotropic and may produce rougher or cloudy surfaces that can impact your optical devices.

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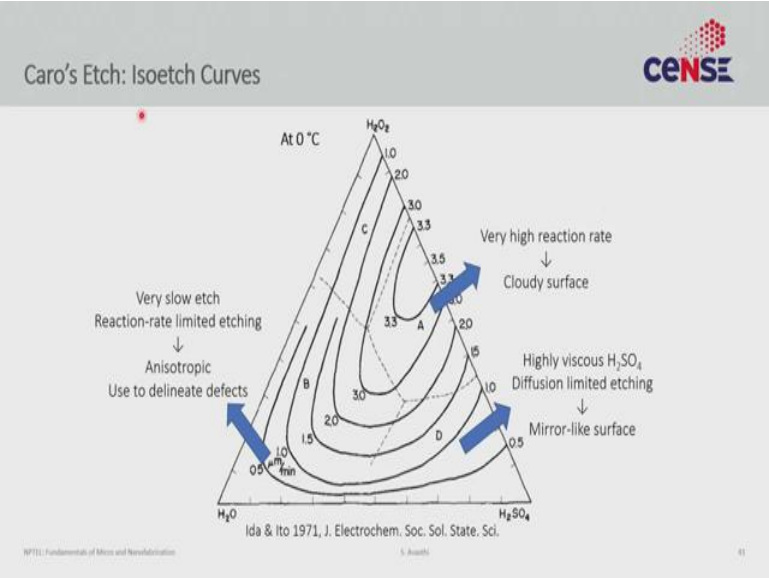

Caro's etchant is a canonical GaAs etchant, a three-component solution. It has peroxide, the oxidant, H_2SO_4 acid, and water as a diluent. As we don't have HNO_3, there is no need for a low dielectric diluent like acetic acid. You can make a similar Isoetch curve to what we saw for the HNA etch of silicon. The axes represent the concentration of water, H_2O_2, and H_2SO_4. Isoetch contours represent several unique concentration combinations with

the same etch-rate. At the corners, you usually wait on the sparse components. That leads to different types of morphology and surface finish. For very slow etching, you need a highly diluted system. It is reaction rate limited, which leads to anisotropy. It is also useful in delineating the defects. We will discuss it during defect-etch.

Somewhere in the middle, the etching rate is maximum because the concentrations of both H_2O_2 and H_2SO_4 are high. We don't use these regions for microfabrication because it is difficult to control the etching rates, and the surfaces come out cloudy, not clean. At the bottom right corner, the H_2SO_4 concentration is high and H_2O_2 low. It leads to a thick etchant, as in higher concentrations, H_2SO_4 is very syrup-like. In this regime, you are diffusion-limited and get mirror-like surfaces. Since GaAs is an optoelectronic material, mirror-like surface-finish is useful.

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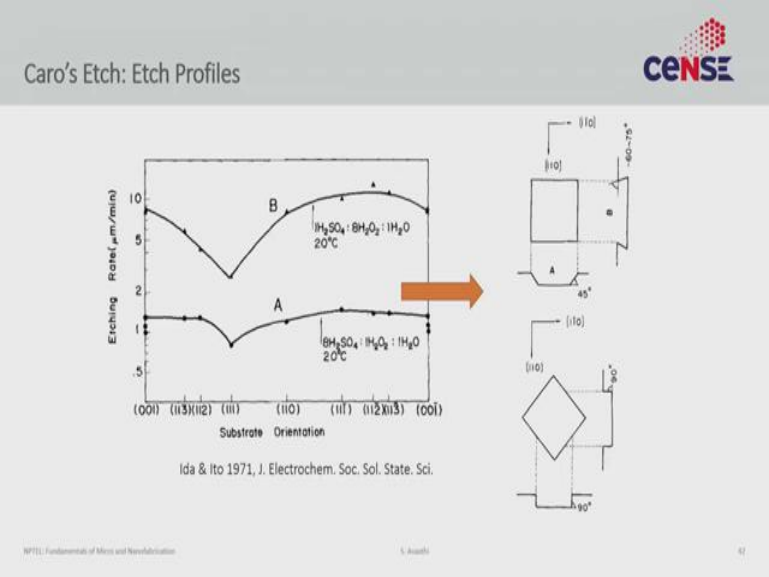

Caro's etch fundamentally is an anisotropic etch. So, the Isoetch curves that we saw correspond to a particular temperature (0^oC) and orientation. For a specific composition, the etch-rates depend on the surface-orientation. (111) has a slightly different rate than (110). With A ($8H_2SO_4$:H_2O_2:H_2O), because of high H_2SO_4, the etching is diffusion-limited, and hence, relatively isotropic, while with a low H_2SO_4 fraction composition B (H_2SO_4:$8H_2O_2$:H_2O), the etching is reaction rate limited, and thus, more orientation dependent.

As this etch is anisotropic like silicon anisotropic-etch, you should see it in the cross-sectional profiles. You start with a square mask pattern. After the etch, you would not get perpendicular sidewalls. In the cross-section along [110] direction, you get sidewalls with a negative slope, with an angle ~ 60-75^{o}. In silicon, it was~50-60^{o} with a positive slope and (111) face. In GaAs, you get a negative slope; the hole is broader at the bottom than at the top. It is also direction-dependent. In the cross-section along [1-10] direction, you get a positive slope. If you rotate that square by 45^{o}, you get perfectly 90^{o} etch-sidewalls. You have not changed the etchant or the substrate. All you have changed is the orientation of the masking pattern. We will not discuss it in more detail here.

The etching rate depends not just on the substrate orientation but also Ga or As-face and the cross-section orientation. The anisotropic etch complexity (and likelihood) is significantly more in GaAs than in silicon because of the crystal lattice complexity. 3D visualization of the etch-pattern becomes a little tricky; Simulators can help with it.

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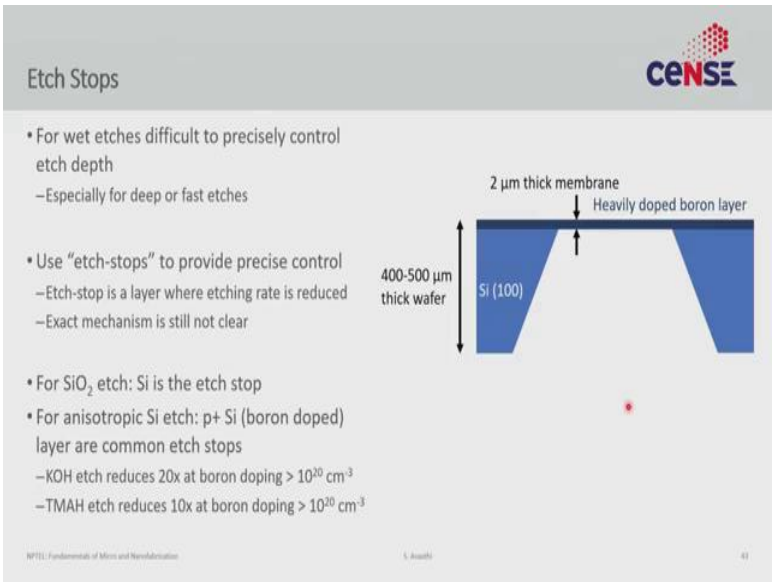

The next concept I want to introduce is an etch-stop. You are etching silicon (100) with TMAH, an anisotropic etchant. Etch-stop represents a film which doesn't etch in the etchant. In this case, it is this dark blue layer. As soon as the etch-surface reaches this layer, the etching will stop or greatly slow down. Thus, they make the etching stable against small variations in rate or the substrate thickness.

We discussed that while etching SiO_2 on silicon, HF etches SiO_2 very well but stops at silicon. So, silicon is an etch-stop for SiO_2 etching using HF. Etch-stops can be slightly different too. We create heavy boron doping on Si (100) through diffusion or implantation in this specific etch, which acts as an etch-stop for silicon anisotropic etch. It may not make sense because the chemistry of the material does not change by doping, at least not too much. Why does silicon (100) etch quickly, but as soon as you add a little boron (ppm, or maybe 1-2 %), the etching stop altogether? Again, most etching is electrochemical, not just chemistry. There is an appreciable difference between the work function of highly doped silicon and un-doped silicon, enough to stop the etch.

Etch-stops can be useful. Suppose you have a 400-500 µm thick wafer, and you want to etch a window from the back to make a 2 µm membrane. The etch-rate in KOH is 100 nm/min. In an hour, you remove 6 µm. To go 400 µm, you need 60 hours. For that long an etch, you leave the wafer in the solution and come back after 2.5 days. If the etching time is that long, it is tough to stop at a film thickness of 2 µm precisely after etching, say 498 of 500 µm wafer. It is a challenging processing problem.

The process becomes much more repeatable if you use an etch-stop rather than a timing approach. With the timing approach, assume a canonical etch-rate of 6 µm/hr with a variation of 10 %. If the etch rate is only 1 % higher, you can easily overshoot - etch a through-hole and not end at a membrane. However, if you first create a 2 µm thick doped layer and then start etching, even if the rate varies by 10 %, it does not matter. Once the etch-surface reaches this highly doped boron layer, the etching stops. You still roughly get a 2 µm thick membrane that you intended.

For this, you need highly doped films, $> 10^{20}/cm^3$. How much does the etching rate slow? For KOH, the etch-rate reduces 20 x. So, 6 µm/hr would become 0.3 µm/hr, which is relatively low. That is the basic idea of etch-stop. There are several etch-stops. If you need to end the etch with thin membranes, it's often better to use etch-stops instead of using a stopwatch and trying to time the etch.

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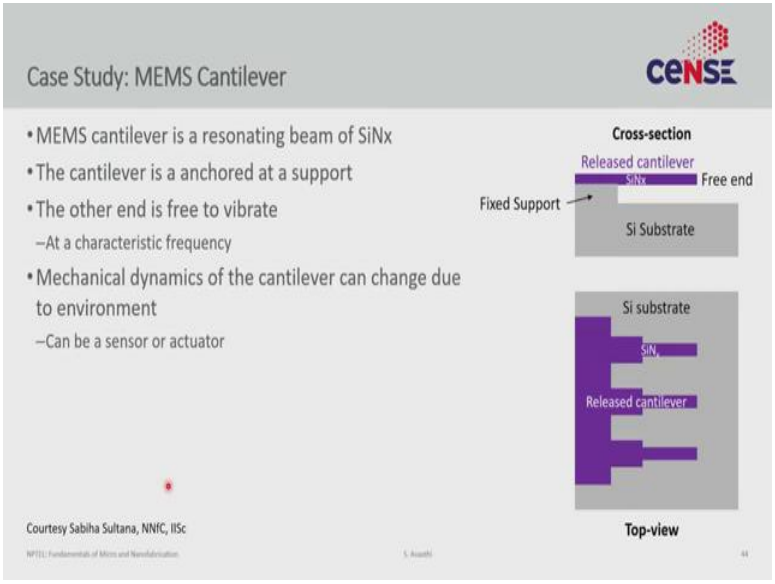

Let's discuss a practical example of making a MEMS cantilever. It involves both wet and dry etching, anisotropic as well as isotropic. Towards the end of the course, we make this cantilever in the lab. Before you see the fabrication video, let's go through it step by step. What is a MEMS cantilever? A cantilever is an overhanging beam. In the cross-section, you have a silicon substrate and a Si_3N_4 film on it. The film has a free end that can vibrate and a fixed or constrained part to hinge it. We can use this vibration for sensing and actuation. These devices are a general class of MEMS devices; MEMS stands for **M**icro **Me**chanical **S**ystems. If the cantilever is at the nanoscale, it is called NEMS. The one we are discussing here is in the order of microns and is a MEMS cantilever.

We have to figure out a way to etch Si_3N_4 to pattern it, as you can see in the top view. Some Si_3N_4 is on the fixed support, but beyond that, it hangs out. Looking from the top, it is a strip, not a membrane. We have to figure out how to etch the silicon underneath to have this overhang. You require lithography to define these features. Typically, you design MEMS cantilevers for vibrating at a specific frequency that strongly depends on its geometry. To have a device that exactly vibrates at a particular frequency, you need precise control of its geometry.

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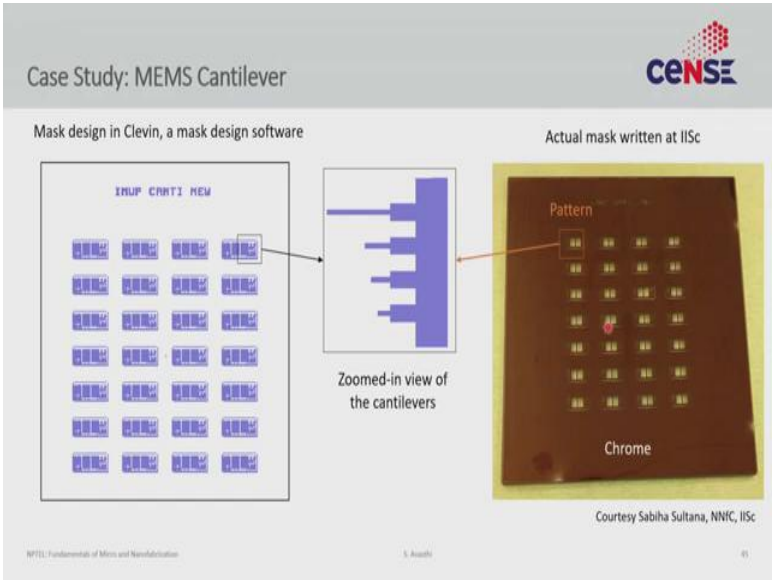

First, you make this device design in any CAD software, like Auto CAD or Clewin. If you zoom in on one of these fields in the left pattern, you can see the cantilever. Then you write this mask on a chrome layer of a mask plate (on the right). As you zoom in to the transparent regions, you see the intended pattern.

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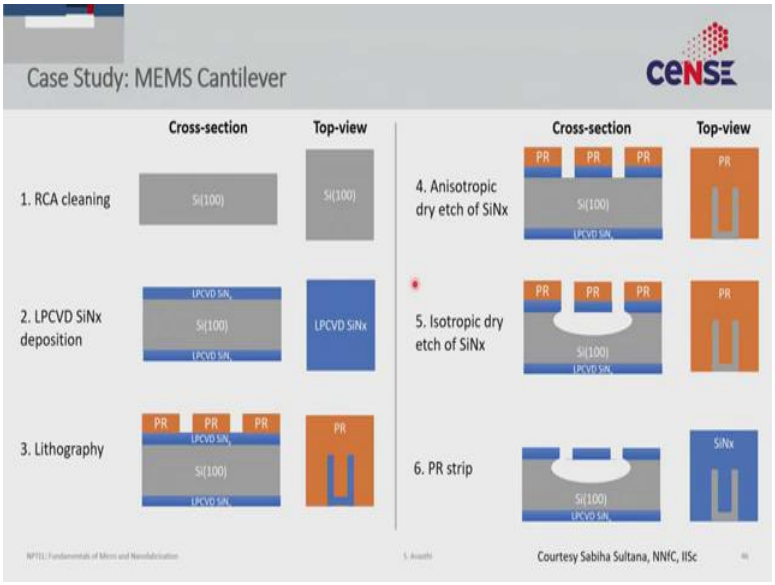

We start with a new silicon wafer in the cantilever process flow and deposit Si_3N_4 using low-pressure CVD (LPCVD). Since we are using LPCVD, we get Si3N4 deposition on the silicon wafer's back surface too. Next, you pattern the photoresist on the Si_3N_4 layer

using this mask via optical lithography. Use it as a mask to etch Si_3N_4 using anisotropic dry etching. You will learn dry etching in the next module. As it is anisotropic, you don't have an undercut.

The back Si_3N_4 doesn't etch because most etch dry etch tools are top surface facing. The etchant never sees the back surface. You now have a patterned Si_3N_4 but have no overhangs. To create an overhang, you need to etch the underlying silicon laterally. The etching must be isotropic to get an undercut. So, we do dry isotropic etch. There is an undercut on both sides. If you make it large enough, everything underneath this PR and Si_3N_4 gets etched, and you have a hanging/free-floating Si_3N_4. After that, you remove the photoresist using a PR strip. Thus you get a simple MEMS cantilever.

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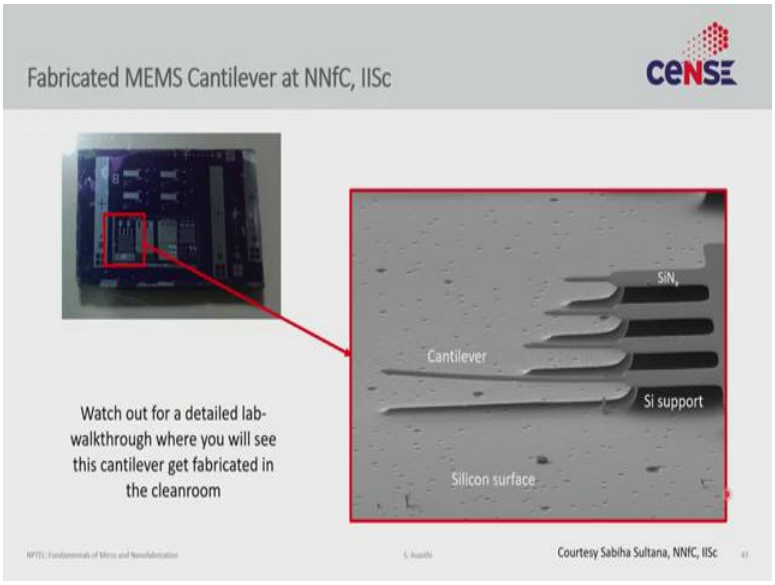

In this SEM image, we have microcantilevers that you will see us fabricate in the lab module. You can also see the silicon support. We have made them in different sizes. So, their fundamental vibration frequencies are different. You can tell that we have done isotropic etch by the spherical or smoothish profile that is not vertical. From the sides, the walls are relatively flat. It is a combination of isotropic and anisotropic etch.

Why is this cantilever bending upwards? Depending upon the Si_3N_4 deposition conditions, you would have built-in stress. Since the film is highly dense, it often has compressive stress. After a high-temperature deposition, as you cool the wafer, Si_3N_4 contracts at a different rate than silicon because of different thermal expansion

coefficients. There will be residual stress in the Si_3N_4 layer when you come to room temperature, either compressive or tensile, depending upon which CTE is larger. When you etch the silicon underneath, all the stress gets released, and that energy goes into bending the cantilever a little up or sometimes a little down.

There also adhesion effects; this is dry-etch, so there is no liquid involved. You can have surface tension in wet etching, pulling the cantilever towards or away from the surface as you remove the etchant. You see pitting damage due to etching. In dry etching, we bombard the surface a little, causing some damage. For MEMS, it is not very severe.

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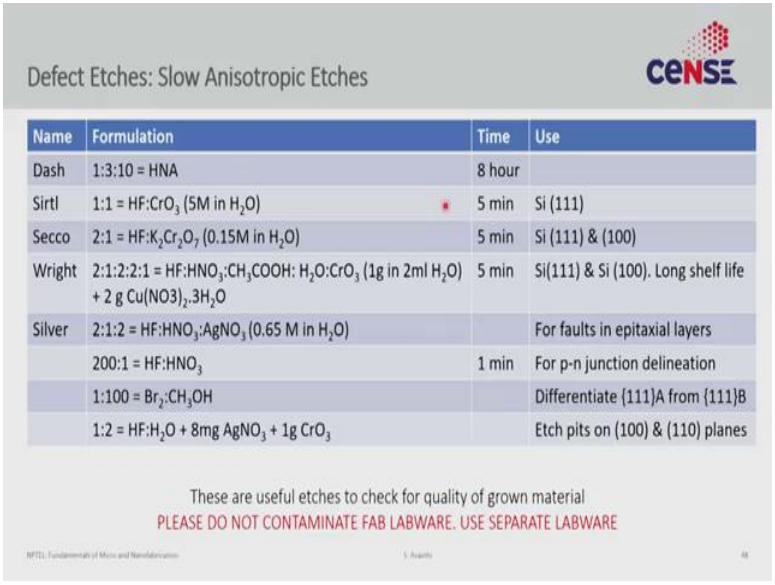

In modern semiconductors, we have defects. We want to see them for understanding them, but we are victims of our success. We have become so good at depositing these films that the defects are few and far between; their density is low. There is one defect for thousands or millions of atoms. In the '60s and '70s, when access to TEM and SEM was not prevalent, you could not dedicate hours of tool time scanning thousands of pictures looking for one defect. We had to develop a better, higher throughput method to see the defects like dislocations or precipitates, smaller than the optical wavelengths. You don't see them in an optical microscope. But, if you enhance the defect-size and make them visible, you can capture a large area. You can take high-resolution visual images, zoom in, and check for them.

You enlarge the defect using defect-etch by anisotropic etchants. We shall not discuss the mechanism in minute detail. The surrounding region can be at higher energy (because of stress or other factors) and have a different etching rate than the bulk. You can use that difference to create a hillock (the defect doesn't etch but the rest of the material does) or a pit (it does, very fast, but the rest of the material doesn't). Thus, you create a morphological feature, usually more extensive than the defect, because it creates stress in an area larger than itself. This hillock or a pit can often be ~μm, and hence, visible under an optical microscope.

There is a library of defect-etches. We have some popular ones in the slide. The Dash etch, an old one, is just a modified HNA etch. It is a dilute isotropic silicon etch, with more HNO_3 than HF. W. C. Dash found this etch to delineate defects in silicon. The issue is it takes ~ 8 hours, a very long time, to show defects. In modern etch, we use chromic acid as a primary etchant in place of HNO_3. You have an HF and chromium oxide solution with water as a diluent. There is a family of chromium oxide-based etches. Sirtl, Secco, and Schimmel (not mentioned in the slide) use chromium oxide. The advantage is that you can see the (111) and (100) facets. And the etching times are reasonably short.

Another class of defect-etch uses both HNO_3 and chromic oxide. Wright etchant also uses some copper nitrate. Some of these etchants are complex, and it is challenging to identify the mechanism even if you read the original paper. Maybe there is some intuition the authors had but not shared. There is some method to the madness, but a lot of defect-etch has become more art than science. You use these as ready recipes. The advantage of Wright etchant is its long shelf life. You can store it in your fridge. Silver etch are $AgNO_3$ based defect-etch.

Some bromine-based systems can distinguish between GaAs A snd B faces. The etching rates are very different for these faces. You can use the HF-HNO_3 etch to delineate the p-n junction by marking the line between p-type and n-type material. Silver-etch can highlight the defects in the CVD epitaxial films. Most of these chemicals are not CMOS compatible. For example, chromium is a contaminant we want to avoid. If you are using defect-etch, please keep separate LabWare to prevent contaminating your CMOS grade LabWare. Don't use the samples you have etched with CMOS incompatible defect-etch for device fabrication; You can't clean them.

Here are some references for each of the defect-etch that we discussed.

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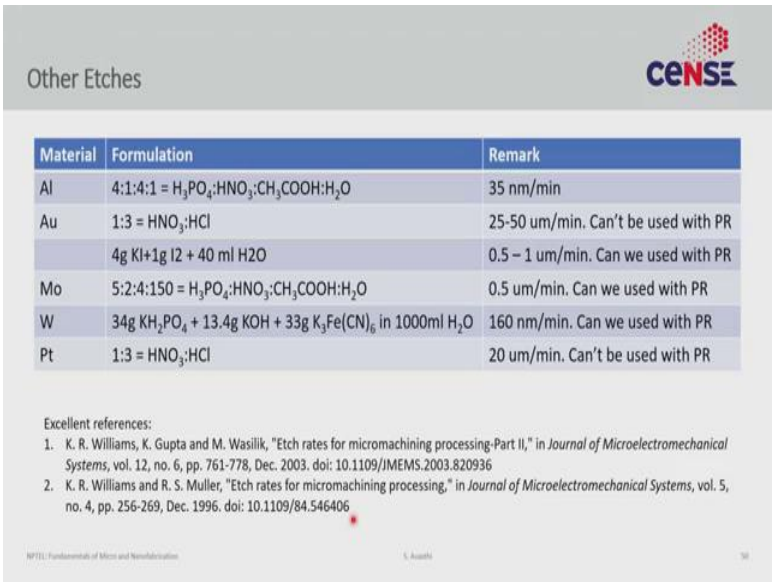

Metal-etch is another useful etch class. We simply use either an oxidant or an acid for wet metal etching. For Al, the common etchant is H_3PO_4:HNO_3 with a rate of about 100-150 nm/min. Gold is a noble metal. So, it does not etch with most etchants. You use a strong etchant like aqua regia, but it degrades photoresist too. Thankfully, there are some iodine-based gold etchants that you can use with the photoresist. If you have to pattern gold, you may have to use this. For Platinum, we don't have any etchant that will not destroy the PR. So, you cannot pattern it by etching. In general, patterning metals by etching is difficult. We use a technique called lift-off.

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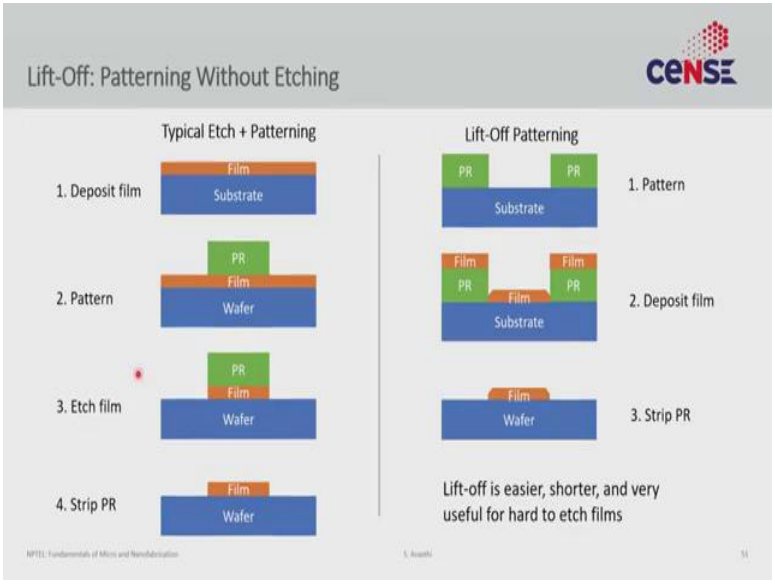

Typical patterning: you deposit a film, coat it with a photoresist (PR), and pattern it. You use it as an etch-mask to remove the unwanted part of the film. It doesn't work with Platinum because no etchant will etch Pt but not PR. There, you can do a lift-off, where you define an inverse pattern. You keep the PR where you do not want Pt to deposit. You deposit Pt after (inverse) patterning the PR, and then, when you remove the PR, all the unwanted Pt floats away. You only get Pt where there is no PR. There is no etching here, just lithography, deposition, and PR removal.

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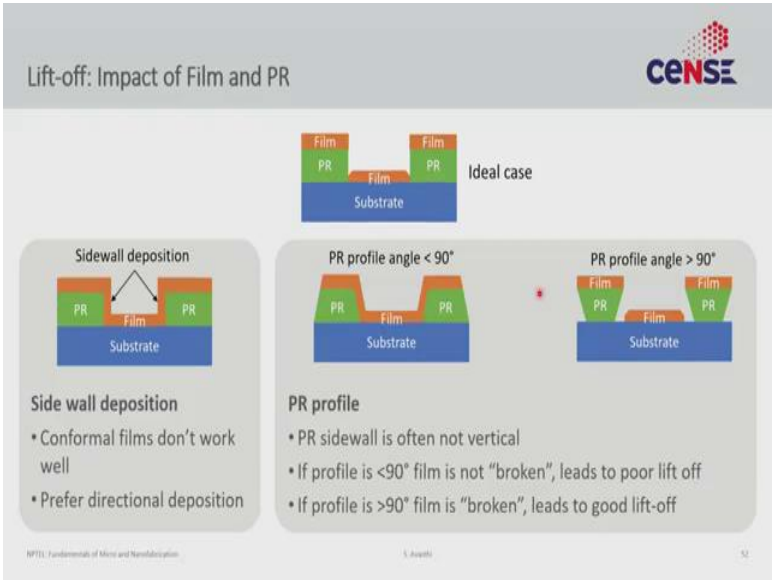

The first cartoon is the ideal case you expect, but you may get sidewall depositions. It becomes unclear how the film will peel when the PR goes away. So, you don't want this to happen. We prefer directional-deposition over conformal; evaporation over sputtering. The practical photoresist profiles are not precisely 90^o. For < 90^o wall profiles, the film doesn't break easily and leads to a poor lift-off than > 90^o faces.

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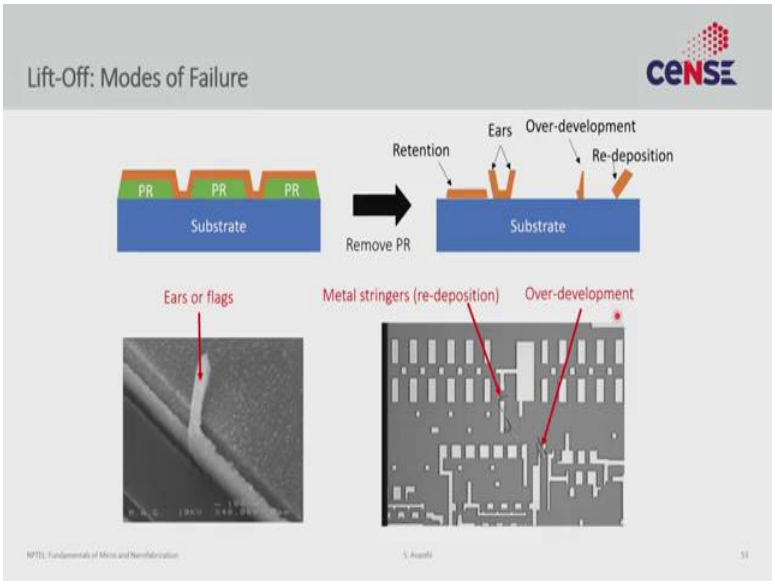

Failure Modes: Retention – you may get the film where you don't intend it to be. You may get ears if you have a conformal deposition and the sidewall metal remains. If the PR is under-developed, the metal peels off from where it should stay. The unwanted feature that floats with the PR can sometimes fall back on the surface and redeposit. Lift-off is a little tricky or a non-repeatable process, but necessary for metals like Pt. You can try a lift-off resist to enhance the success of patterning.

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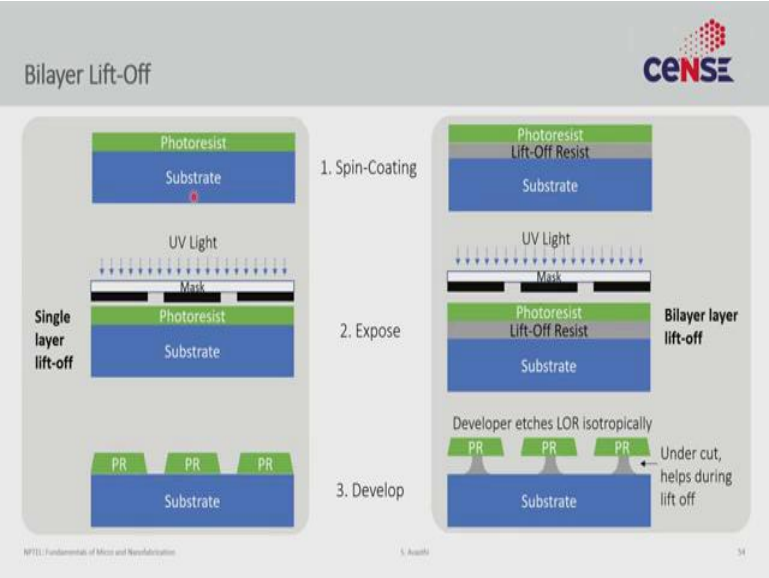

A lift-off resist (LOR) is not a photoactive material; you deposit it between the PR and the substrate. After exposure, PR develops as usual, but you design the LOR to etch isotropically in the developer. So, you get undercuts in the LOR layer. You get a T-looking profile instead of < 90^{o}. This T is much better for lift-off because there is no concern of sidewall deposition.

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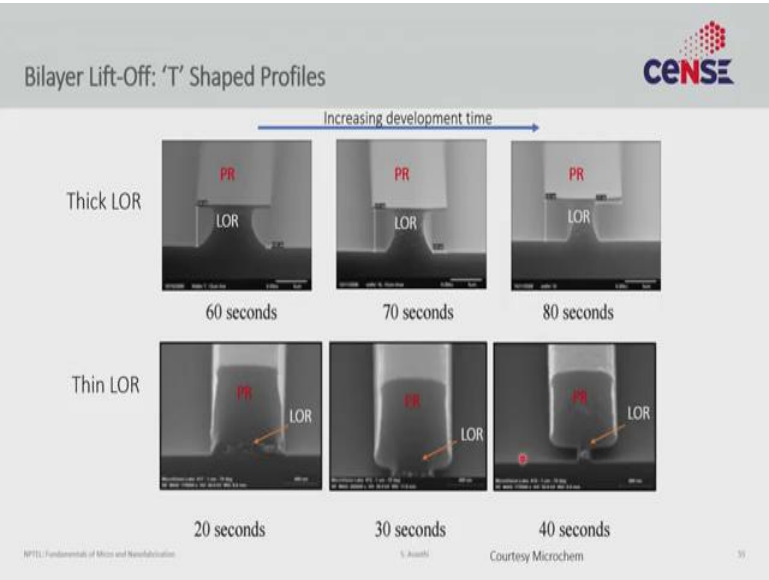

Here are some actual figures from the manufacturer of this LOR. You see the undercut in the LOR and the PR on the top. If you etch for longer, the undercut increases, the T's

base narrows, and the overhang look longer. You can also change the LOR thickness as compared to the PR. Depending on your application, you can select the resist profile.

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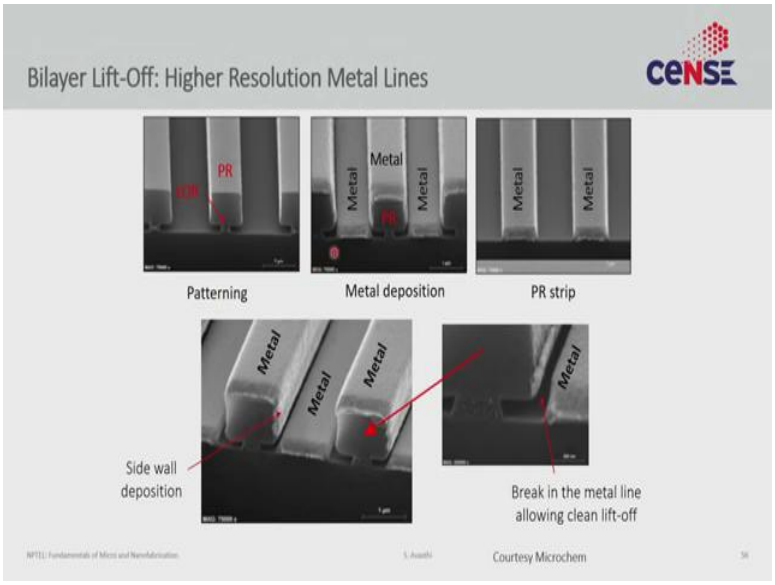

When you deposit metal on this T, at the edges, there is no conformal deposition. There is always a crack because the photoresist is not continuous. It allows you a cleaner lift-off than what would be otherwise possible. If your lift-off features are tiny, you may use LOR to improve the process's fidelity and repeatability.

This lecture is the end of the wet etching module. Towards the end of this course, we will have a class on process integration.