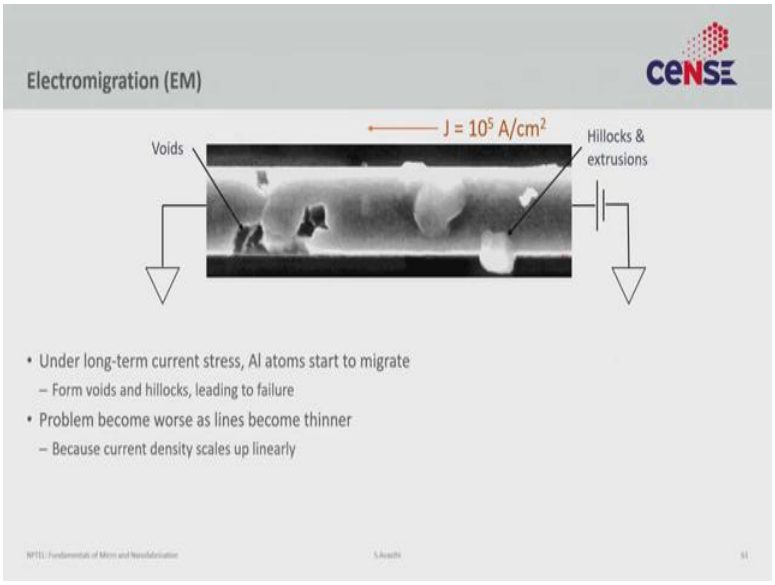
Fundamentals of Micro and Nanofabrication
Prof. Sushobhan Avasthi
Centre for Nano Science and Engineering
Indian Institute of Science, Bengaluru

Lecture – 27
Metallization: Electromigration and Epilogue

This lecture concludes the module on additive processing and the discussion on physical vapor deposition/metallization. We have discussed that there are multiple metal layers in a chip. We have to consider the contact resistance, the silicide formation, and the maximum substrate temperature while making metal contact with silicon. In this lecture, we discuss other problems with metals: electromigration and diffusion, and the use of a diffusion barrier layer.

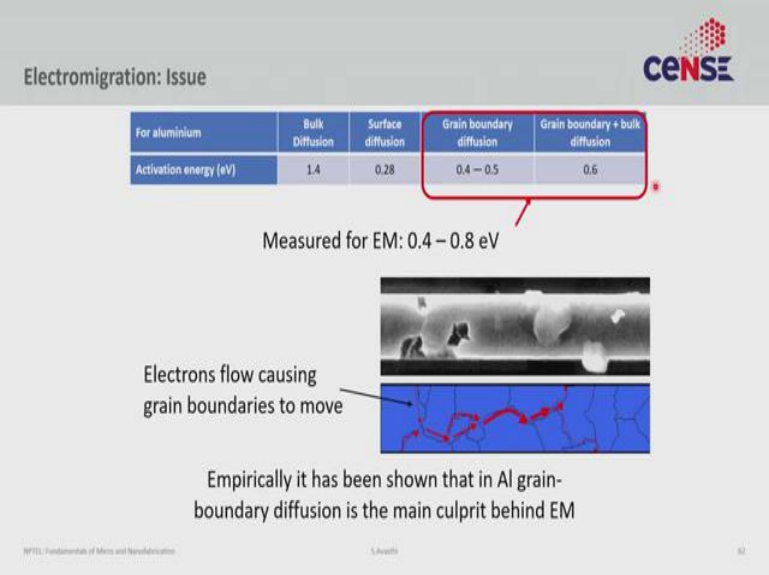
(Refer Slide Time: 01:26)



What is electromigration? In this top view of a metal line in a microfabricated device, assume the right side to be at a positive voltage and left at ground. The current flows from right to left. Since the metals are very conductive, and the dimension is in nano-micro meter, the current densities can be high, say 10^5 A/cm^2. The actual current maybe 1 A or so. If you keep flowing it for a long time, the metal lines start to degrade. This figure depicts such an aged line. Initially, it may have been a nice smooth line, but now it has voids, hillocks, and protrusions. It seems that the aluminum migrates from these voids to form the hillock. There is some mass transport; as the current flows to the left,

the aluminum appears to flow to the right at a slow rate. As the devices scale down due to Moore's law, the lines become thinner, and the problem worsens. It was a considerable reliability problem. Even though silicon devices are very reliable, the metal lines would degrade with time, the delay would increase, or they fail, rendering the device useless.

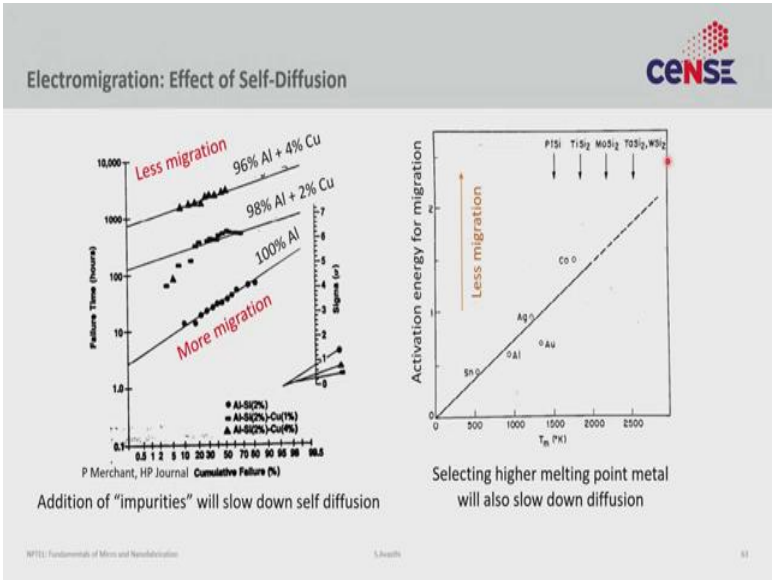
(Refer Slide Time: 03:25)



We see aluminum mass transport; the first guess would be diffusion, but through what mechanism? To analyze it, we compare the electromigration activation energy to that of known aluminum diffusion mechanisms. The activation energy for the aluminum diffusion in the aluminum bulk is 1.4 eV. On the surface, it is 0.28 eV. Since it is a PVD polycrystalline film, we have grains and grain boundaries. The grain boundary mediated Al diffusion has an activation energy of 0.4-0.5 eV. The grain boundary + bulk diffusion has which have an activation energy of around 0.6 eV.

We deposit the metal films using evaporation; it has a random orientation and is polycrystalline. As the current flows from right to left, the electrons flow from left to right. The sheer momentum of the electron pushes on these grain boundaries and moves the material out of the way. That causes this electromigration. By empirically comparing these activation energies, they were able to deduce the mechanism. The measured activation energy for electromagnetic migration is about 0.5-0.6 eV, and it matches with the grain boundary and the grain boundary + bulk diffusion. Those are the probable mechanisms.

(Refer Slide Time: 05:41)



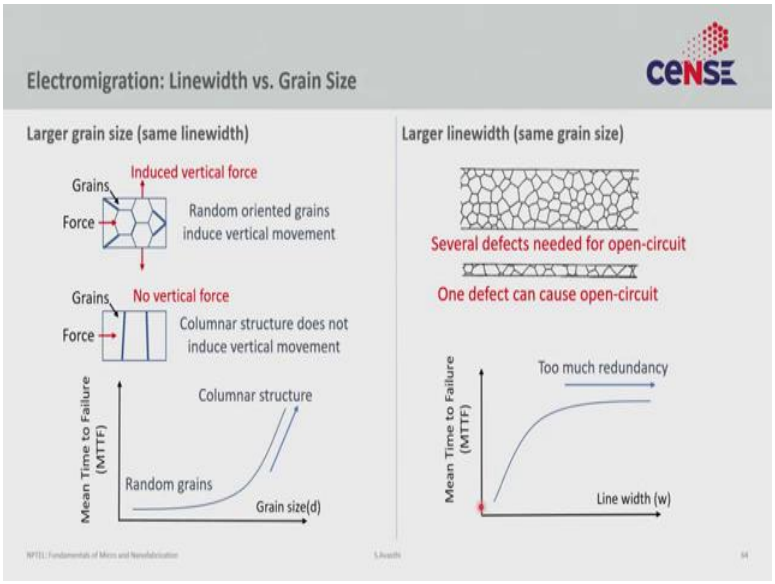
Another fascinating insight came from a lucky discovery that the electromigration changes with tiny amounts of impurities. If there is electromigration, the device will eventually fail. If it is bad, the time to failure will be short. We make a failure plot for 100s or 1000s of devices on a log-log scale. As the devices start failing, we mark the fraction of the failed devices (cumulative-failure) on the x-axis, and when they die (failure time) on the y-axis. The cumulative-failure will ultimately reach 100 %. For the same cumulative-failure rate, the electromigration problem is smaller if the time to failure is higher. Pure aluminum is the control case. As you added a little bit of copper, the failure time increases. If you add 4 % Cu, it takes even longer to fail. To make metal lines, you better add 4 % Cu in Al than using pure Al, vis-à-vis electromigration. The addition of impurities slows down self-diffusion. Aluminum has to now diffuse into a copper-aluminum matrix, which is a little slower. I don't know whether it is a true story or not, but this is how it goes: The author got the Cu contamination as he was using e-beam evaporation, but the beam was a little misaligned. It also fell on the Cu hearth along with the aluminum pellet. They saw much lower electromigration rates.

The second way of reducing electromigration and improving reliability is to use higher melting point metals. Look at the electromigration activation energy versus the melting point curve. As you go from tin to aluminum to cobalt, the melting point increases, and so does the electromigration activation energy. If you replace Al with Co, you may get more reliable lines, but the resistivity would also increase. Silicides like platinum

silicide, tungsten silicide, moly silicide, and tantalum silicide are also very high melting point materials, as discussed before. These are much better for reliability because they have much higher activation energies for migration. So, in devices where reliability is more important, say in military-grade or satellite grade devices, people have moved to either silicide or high melting point metals such as tungsten or cobalt.

Let's discuss how to prevent electromigration. If you have to use aluminum, what can we do from a morphological standpoint to avoid the problem?

(Refer Slide Time: 11:24)



We will discuss the effect of the grain size and the linewidth on the electromigration. To understand the impact of grain size, we have two metal lines (top view) with the same linewidth. One has some random grains that I am representing with hexagons and triangles. The current is from right to left. Each grain sees the electron flux from left to right. In the second line, we have large or columnar grains. The grains are so large that you see only those boundaries perpendicular to the current flow from the top.

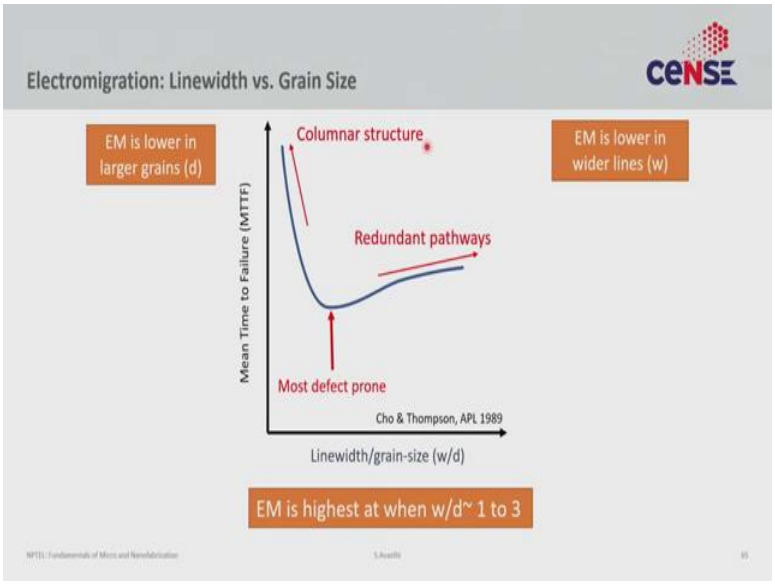
The only thing we change is the grain size. Let us do a thought experiment. The electron flux applies force on the grains from the left. If the grains are small or at angles, this force induces a component perpendicular to the line, represented by these red lines. It moves these grains out. It is electromigration that may lead to an open circuit. If you compare it with a large or columnar grain case, you have the same force. However, the component perpendicular to the line is negligible. There is no cos(θ) component that can

push this grain out. The only force is along the line. Now, this grain can't move along the line because the neighboring grains bind it. So, if you plot the meantime to failure (MTTF) as a function of grain size (d), the small grains suffer more electromigration and will have a smaller MTTF (will fail faster) than larger grains. MTTF increases with d.

How do you change the metal film grain size? We discussed that the substrate temperature, arrival angle, ion energy, argon bombardment, and sputtering pressure affect the morphology. You may tune these parameters to get larger grain films.

To understand the effect of linewidth (w), we compare the top view of two metal lines with different linewidths (w) but the same grain size (d). A broader line will have more grains than a narrow one. Under the same force due to electron flux, even if some grains move out of the broader line due to electromigration, it won't significantly change the characteristics. There is too much redundancy in the system; there is always some other grain to compensate. However, in a narrow line, some of these grains are critical for continuity. You may get an open circuit if they move out. If you plot MTTF vs. w, you have a smaller MTTF for a narrow line as the electromigration affects it more critically.

(Refer Slide Time: 16:58)

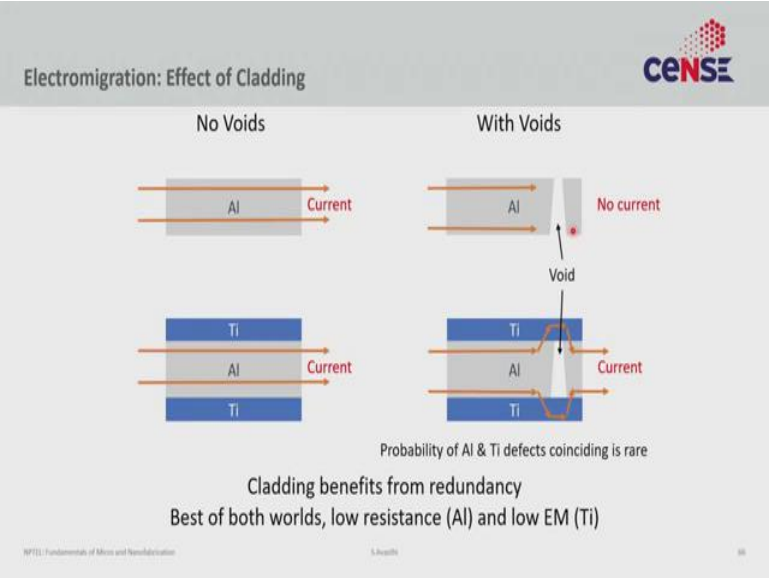


This graph combines the effect of the line width (w) and grain size (d) in one. We have MTTF as a function of w/d (linewidth to grain size ratio). w/d tells you how large the linewidth is, compared to the grain size. You see a U-shaped curve. You have higher reliability (longer MTTF) if the line is very wide compared to the grain size or very

narrow compared to d. However, somewhere in the middle (w/d ~ 3), you have the worst of both worlds. You don't have sufficient redundancy to work around electromigration. You also don't have large enough grains to prevent electromigration. This middle part is the region you would like to avoid; it is the most defect prone or the least reliable.

You may tune the morphology to have redundant pathways or a columnar structure to get better reliability. Another trick is to use higher melting point metals as barriers.

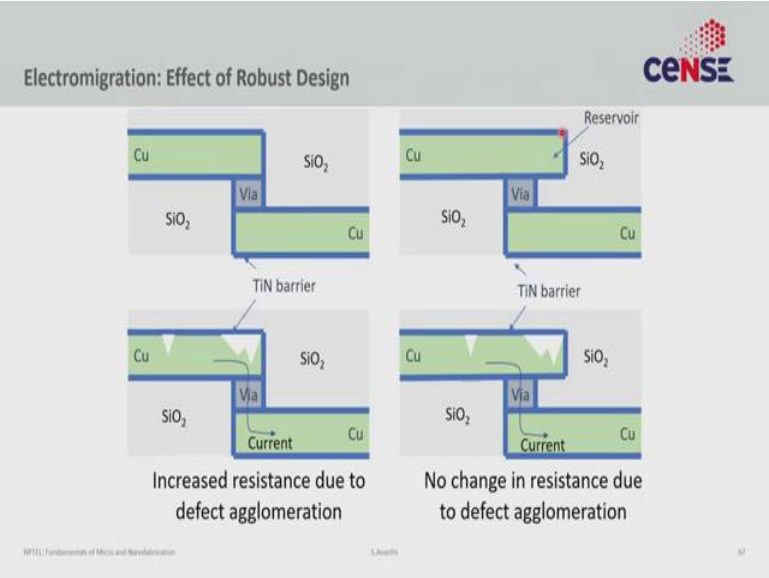
(Refer Slide Time: 18:48)



You start with a void-free aluminum line and accumulate void with time as the current flows. It may cause device failure. If you replace aluminum with titanium, it increases ohmic losses and makes the device slower. A common fix is divide and conquer! Sandwich the Al between top and bottom Ti layers. Even if you have a void in aluminum now, the current flow and the device function will continue as the current can now go through the titanium layer.

This small transport path in Ti doesn't change the device resistance or delay significantly. Titanium on its own will not suffer electromigration much because it is a high melting point material. So, you have used both the materials to your advantage to solve the electromigration problem. It is called cladding.

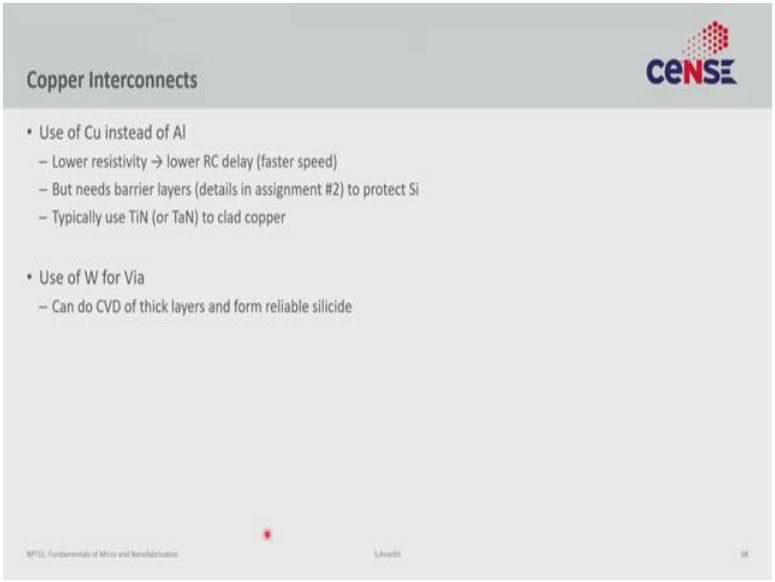
(Refer Slide Time: 20:11)



You can also solve the problem of electromigration by having some redundancy in the system. You have two different metal layers connected by a via, and the rest is SiO_2. Here, the metal is Cu, but you can make similar arguments for Al. The current flows from top to bottom; the electrons flow from bottom to top, which creates pressure on this copper. It electromigrates, and you get a void that becomes bigger and bigger with time, and you see an increase in your resistance.

You can create a reservoir to solve this issue. Have the copper metal layer extending and horizontally overlapping near the via. It doesn't improve resistance prima facie but solves the problem of electromigration. When the current flows, there is this reservoir. Even if you create voids there, it doesn't affect the critical path. So, with time, the resistance change you observe here will be much less before. You solve this problem by using a superior or robust design.

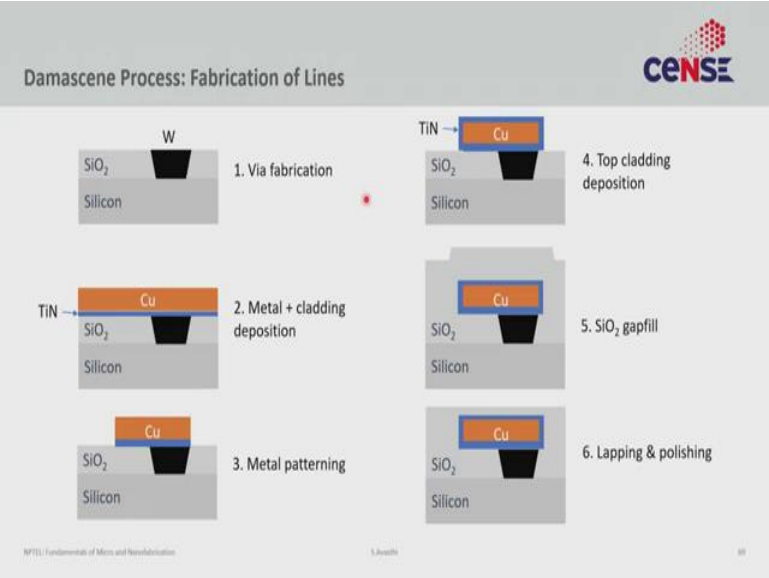
(Refer Slide Time: 21:40)



Another essential discussion is the industry's movement to copper from aluminum. Aluminum is excellent; it's low in cost, deposits by different techniques, form relatively good contacts with silicon after annealing, creates superior interfaces, and has very low resistivity, third or fourth lowest in the periodic table. However, it suffers electromigration. As the devices become smaller, even Al's resistivity reached its limit, and the metal line delay started deciding the device's speed. The only way forward is to reduce the resistivity by moving to copper, which has a high conductivity.

One of the challenges with copper is it is a very potent defect in silicon. Any diffusion of copper into silicon kills the device's performance. This issue counters the pressure to move to copper from aluminum. Somebody had to figure this issue out.

(Refer Slide Time: 23:00)

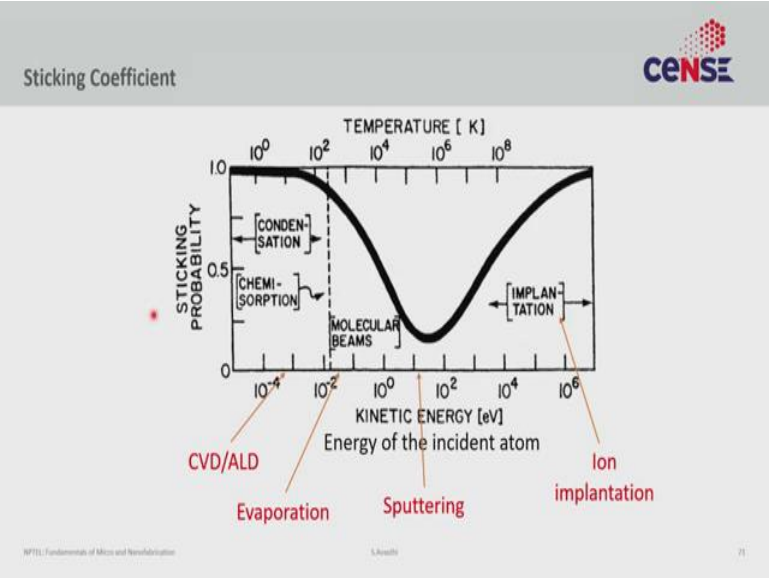


You solve this problem of copper diffusion by using barrier layers, specifically titanium nitride. Its most popular implementation in a commercial device is the damascene process. The details are much more complicated; I will present a simple picture.

You want to make contact with a silicon device (not shown in the figure). So, you cut a hole in the SiO_2 layer and fill it with tungsten Via. Now, you may deposit Cu for making an interconnect, but once you do that, even at the BEOL (400^oC) temperatures, Cu diffuses through SiO_2 to silicon and kill the device. To avoid that, you deposit a thin TiN layer. You select the thickness such that for the thermal budget and time of the remaining process, the copper would not TiN to reach SiO_2 or silicon. This TiN is conductive enough not to increase the series resistance. This TiN is a cladding. Then you pattern copper normally, and also TiN along the way. Then you deposit TiN all around through conformal deposition methods, smartly and of the correct thickness. Then you deposit SiO_2. This cladding prevents this copper from diffusing and contaminating the silicon. This process is the damascene process.

We end the discussion on metallization. We will end this additive processing module with a discussion on the energy-dependent stiction coefficient and a commentary on what deposition methods are appropriate for different applications.

(Refer Slide Time: 26:25)



Till now, we have assumed the stiction coefficient or the sticking probability to be 1. How much it changes, and to what extent, is the subject of this slide. The stiction coefficient is unity under two extreme cases; if the incoming atom or ion is very gentle or low energy or is incident with too high energy.

In CVD, the material comes through diffusion, so practically with 0 impact energy. The incoming species' kinetic energy is minimal; the stiction coefficient is 1; there is almost no backscattering. In implantation, you have ion energy in the range of 10^5 eV. Even there, you have a stiction coefficient of nearly one because there is a tiny probability of something coming back. In ALD, you have chemisorption. The energy is slightly higher in evaporation but low enough that the stiction coefficient is > 0.9. So, we assume whatever comes on the surface sticks.

As you get to a few eV to 10-100 eV, where sputtering happens, the stiction coefficient can be as low as 0.2-0.3. Only 20-25 % of the incoming material stick to the surface, and the rest backscatters. At least in sputtering, we have to account for the stiction coefficient when you model the deposition rates. We can also talk about this in terms of equivalent temperature. CVD and ALD have incoming species at 100-500 K. You have a higher implied temperature in sputtering, so the stiction coefficient becomes low. At very high temperatures, in an implantation system, where the equivalent temperatures are ~ 10^8 K, the stiction coefficient rises again.

(Refer Slide Time: 29:19)

Material	Technique(s)	Comments
Epitaxial silicon	APCVD, LPCVD	900-1100 C
Poly silicon	APCVD or LPCVD	500-650 C
Si_3N_4	LPCVD PECVD	650-800 C for diffusion masking 200-400 C for passivation and low-temperature dielectric
SiO_2	Oxidation APCVD or LPCVD PECVD ALD Sputtering	900-1100C for high-quality gate oxide 200-700 for thick insulator 200-400 C for low-temperature dielectric RT-200 C for low-temperature dielectric RT-500 C for low-temperature dielectric and optical films
Al and Al-alloys	Evaporation Sputtering	RT-300 C for pure films RT-300 C for alloys
W	Sputtering LPCVD	Evaporation is difficult 250-500 C
TiN	Reactive sputtering MOCVD	
Cu	Electroplating Sputtering	Can deposit very thick layers For thinner films
$TiSi_2$	Sputtering + surface reaction	600-700 C for reaction with silicon

You have a typical deposition method for the materials for different applications. There can be exceptions; you can deposit metals using CVD or silicon using evaporation, but that is not common.

For epitaxial silicon, APCVD or LPCVD can give you a relatively clean interface and perfect lattice-matched growth. You require high temperatures, ~ 1100^{o}C. At lower temperatures, you can deposit polysilicon. It is not epitaxial, and you lose on grain size and orientation. I would still recommend APCVD and LPCVD because you have lower impurities with those techniques. For insulators like Si_3N_4, you may use LPCVD or PECVD. The difference between these two is the deposition temperature. For diffusion masking, LPCVD and its high temperatures are okay. For passivation or low-temperature dielectric, you may want to use plasma-enhanced CVD (PECVD).

The highest quality SiO_2 is through native thermal oxidation. But that requires high temperatures; if you want to deposit at lower temperatures, you may use CVD or PECVD. For room temperature oxide, ALD, or sputtering. But these films are only good for low-cost dielectrics or as optical films. They are not necessarily perfect insulators or electronic films. Evaporation is a good option for metal deposition, such as Al, but it doesn't work if you want alloys. You may use sputtering for alloy deposition. You deposit them at lower temperatures because at high temperatures, the metals diffuse.

You can sputter tungsten Via or do LPCVD if conformity is essential. However, the issue with CVD is that it requires a little higher temperatures. For cladding or diffusion barrier TiN, you can use reactive sputtering or MOCVD.

You can sputter copper, but sometimes, you need very thick films. For 1-5 μm copper deposition, evaporation or sputtering are slow and too wasteful. People often use electroplating, which we have discussed briefly before. To get a silicide, you can sputter the metal, for example, Ti, and make it react with silicon to form a silicide. Different silicides require different temperatures. Depending on your thermal budget, you choose an appropriate silicide.

That ends both PVD and the larger module of additive processing. The next module is lithography.